



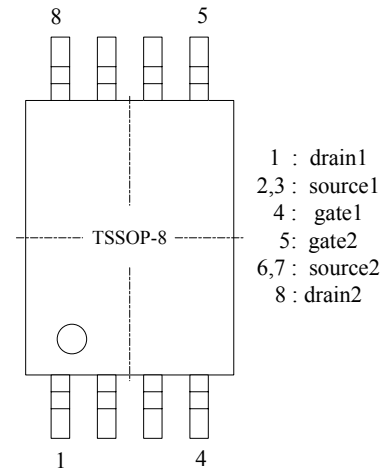
BYD Microelectronics Co., Ltd.

BF9028DNT

20V N-Channel MOSFET

General Description

The BF9028DNT is a dual N-channel MOS Field Effect Transistor, which is applied to electronic systems as a power switch. This device has ESD-protection and low resistance characteristics.



Features

- Can be driven by a 2.3 V power source
- Low on-state resistance

$R_{DS(on)} = 16.0m\Omega$ TYP($V_{GS} = 4.5V$, $I_D = 3.0A$)

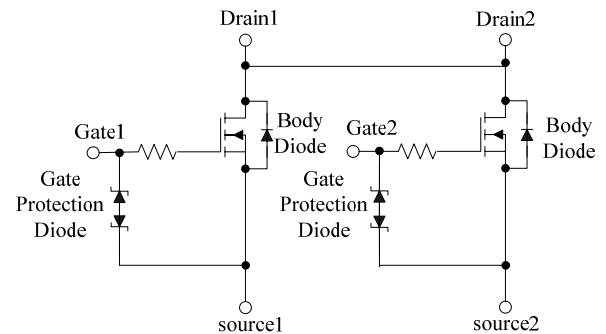
$R_{DS(on)} = 17.5m\Omega$ TYP($V_{GS} = 3.8V$, $I_D = 3.0A$)

$R_{DS(on)} = 22.0m\Omega$ TYP($V_{GS} = 2.5V$, $I_D = 3.0A$)

- Built-in G-S protection diode against ESD
- Lead Pb-free and Halogen-free



EQUIVALENT CIRCUIT



Absolute Maximum Ratings($T_C = 25^\circ C$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage	20	V
I_D	Drain Current(continuous)at $T_C=25^\circ C$	6	A
I_{DM}	Drain Current (pulsed) (Note a)	24	A
V_{GS}	Gate-Source Voltage	± 10	V
P_D	Power Dissipation $T_C = 25^\circ C$	1.5	W
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering Purpose	150	$^\circ C$

Ordering Information

Part Number	Package	Packaging
BF9028DNT	TSSOP-8	3000pcs Tape&Reel

**Electrical Characteristics ($T_c = 25^\circ\text{C}$)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DS}	Drain-source Breakdown Voltage	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}, V_{GS}=0\text{V}$			10	μA
I_{GSS}	Gate-body Leakage Current	$V_{GS}=\pm 12\text{V}, V_{DS}=0\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.5	0.8	1.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS}=4.5\text{V}, I_D=3\text{A}$		16	22	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_D=3\text{A}$		17.5	24	
		$V_{GS}=2.5\text{V}, I_D=3\text{A}$		22	29	
C_{iss}	Input Capacitance	$V_{DS}=15\text{V}, f=1\text{MHz}, V_{GS}=0\text{V}$		800		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=10\text{V}, I_D=3\text{A}, V_{GS}=4\text{V}, R_G=10\Omega$ (Note b,c)		100		ns
t_r	Rise Time			200		ns
$t_{d(off)}$	Turn-off Delay Time			2500		ns
t_f	Fall Time			1200		ns
Q_g	Total Gate Charge	$V_{DS}=16\text{V}, I_D=6\text{A}, V_{GS}=4.5\text{V}$ (Note b,c)		12		nC
Q_{gs}	Gate-source Charge			2.5		nC
Q_{gd}	Gate-Drain Charge			4		nC
$V_{SD(*)}$	Forward On Voltage	$V_{GS}=0\text{V}, I_F=6\text{A}$		0.7		V

Notes

a: Repetitive Rating : Pulse width limited by maximum junction temperature

b: Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

c: Essentially independent of operating temperature

(*)Pulsed:Pulse duration

Caution: These values must not be exceeded under any conditions.**Remark:** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Typical characteristics (25°C unless noted)

Figure 1 Output Characteristics

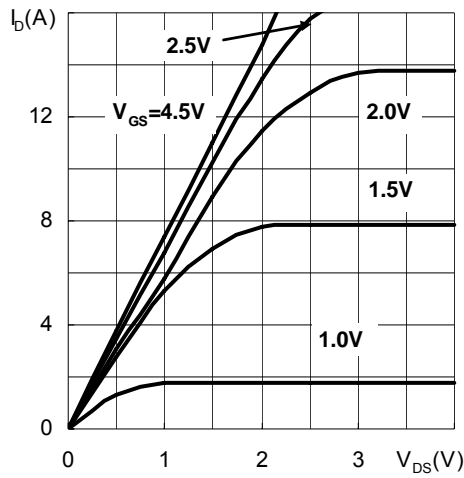


Figure 2 Transfer Characteristics

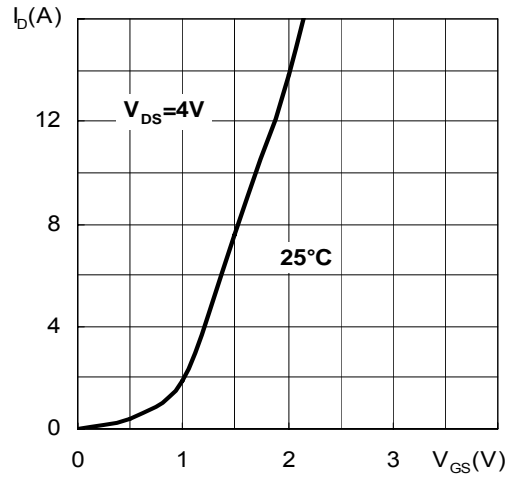


Figure 3 Normalized V_{th} vs. Temperature

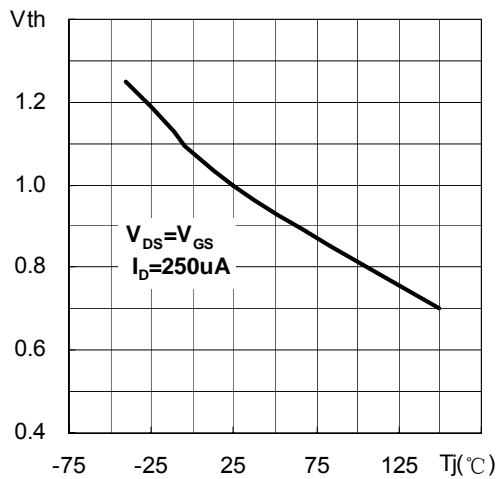


Figure 4 Normalized $B_{V_{DSS}}$ vs. Temperature

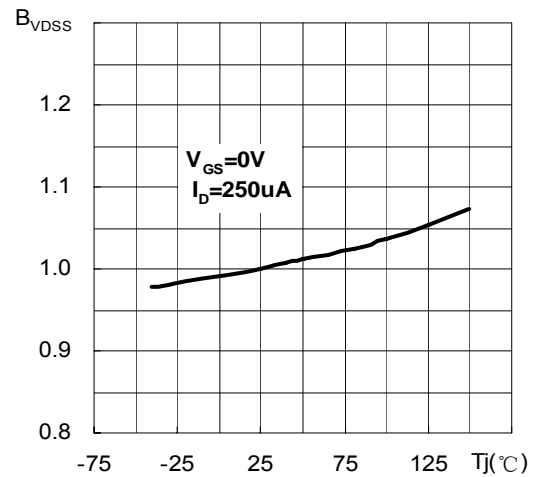


Figure 5 $R_{DS(on)}$ vs. Temperature

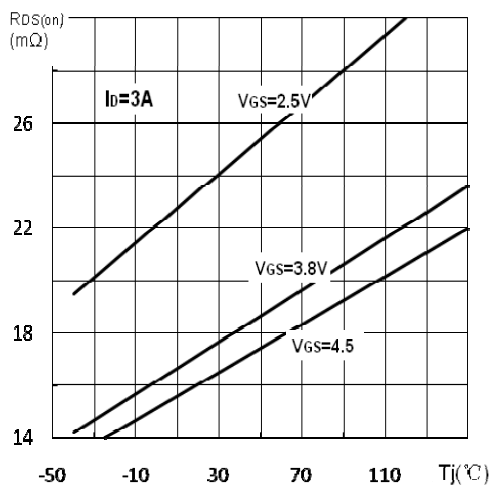


Figure 6 I_{GSS} vs. Environment Temperature

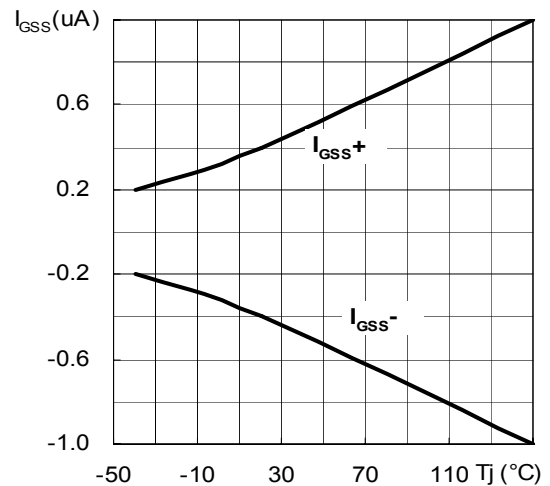


Figure 7 Capacitance

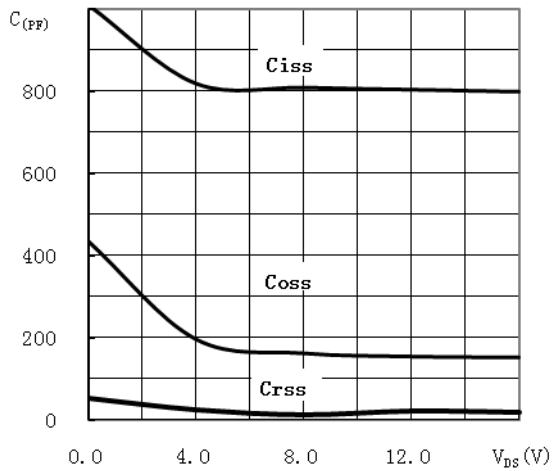


Figure 8 Gate Charge

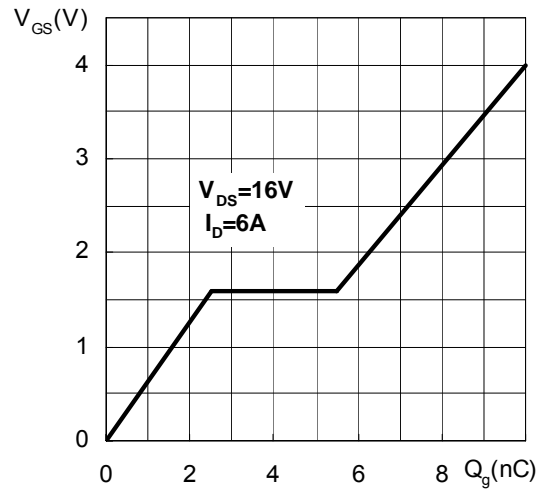


Figure 9 Safe Operating Area

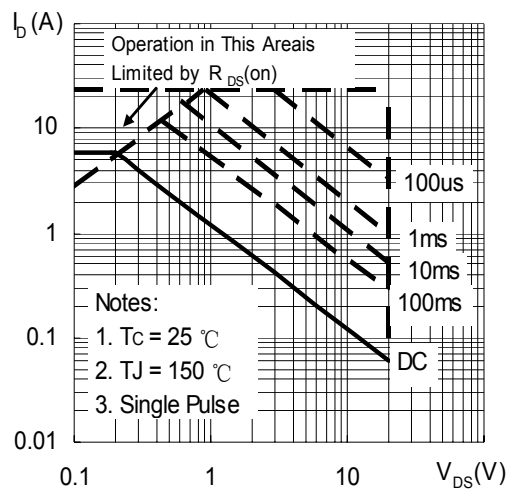


Figure 10 Maximum I_{DSS} vs. Case Temperature

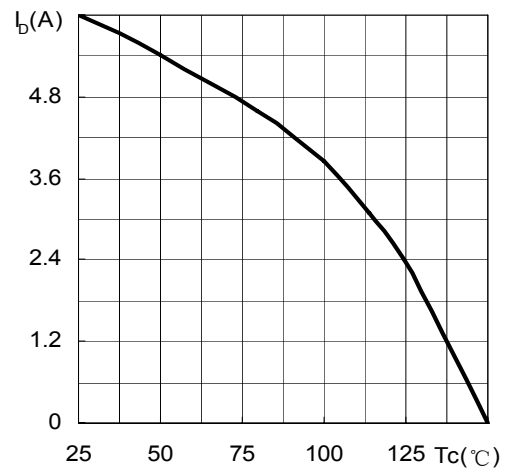


Figure 11 Rdson vs. V_{GS}

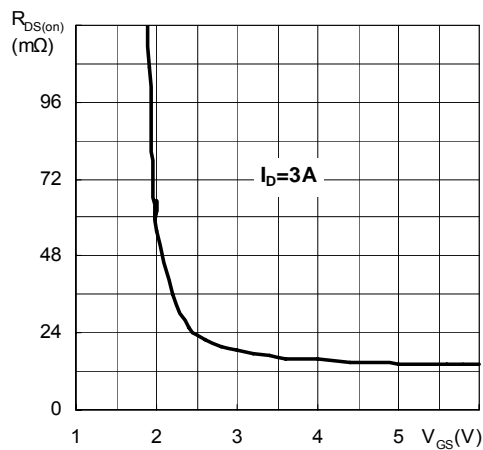


Figure 12 Gate-Current vs. Gate-Source Voltage

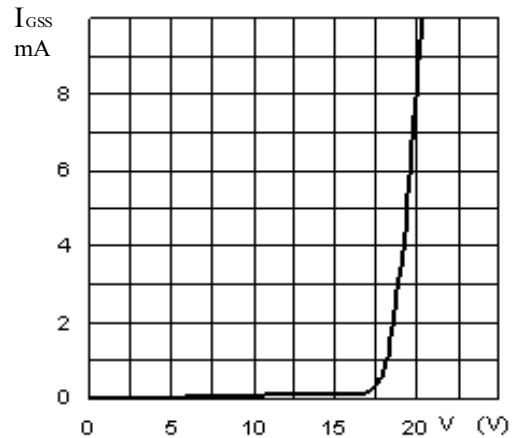
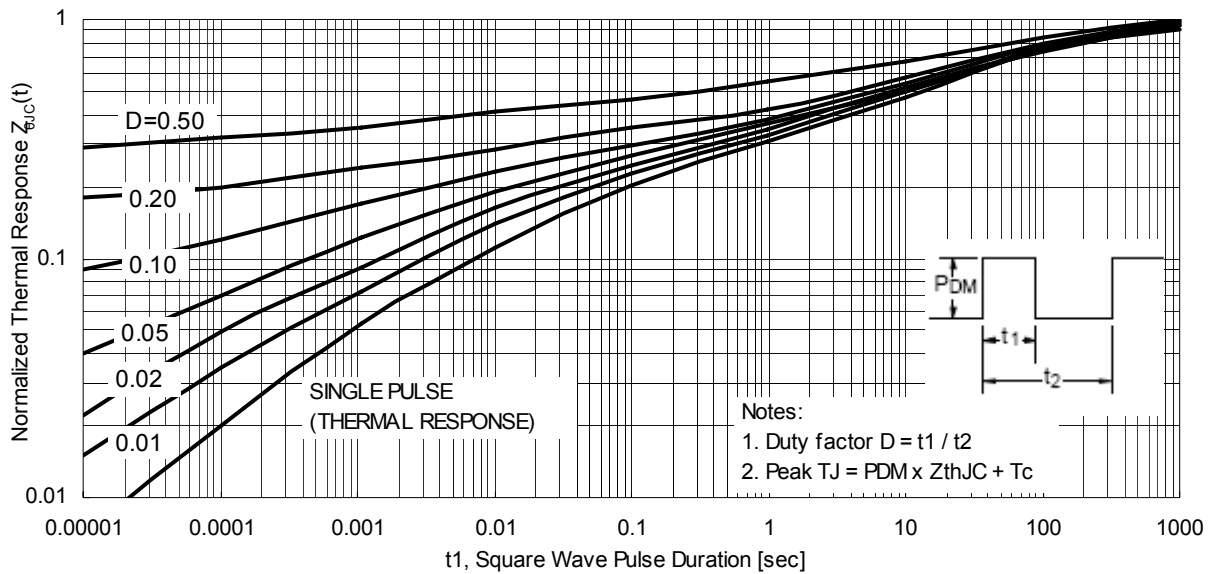
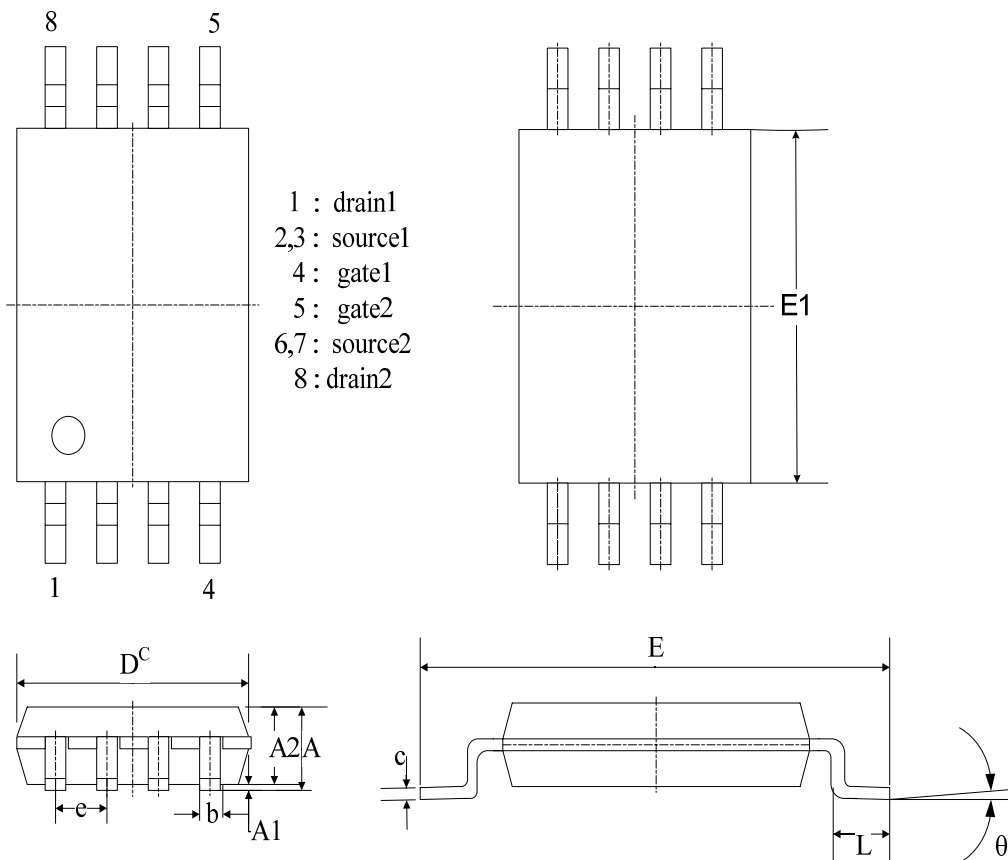


Figure 13 Normalized Maximum Transient Thermal Impedance



Package Drawing:

PACKAGE DRAWING (Unit: mm)

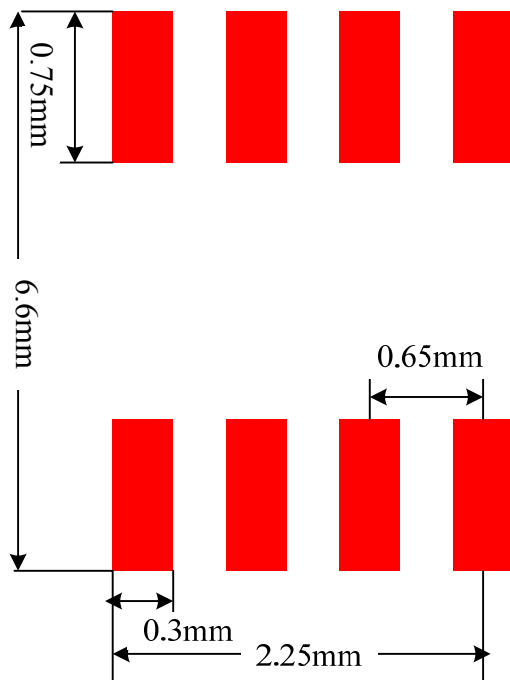


Dimensions

DIM.		A	A1	A2	b	c	D ^c	E	E1	e	L	θ
mm	MIN.	0.820	0.020	0.800	0.170	0.090	2.900	6.200	4.300	0.650 BSC	0.450	0°
	NOM.	—	—	—	—	—	—	6.400	4.400		0.600	4°
	MAX.	1.200	0.150	1.050	0.300	0.200	3.100	6.600	4.500		0.750	8°

Note c. Dimension 'D' does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.

PCB Layout Guide





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