

M5M2168P-55, -70

16384-BIT (4096-WORD BY 4-BIT) STATIC RAM

DESCRIPTION

This is a family of 4096 word by 4-bit static RAMs, fabricated with the high-performance N-channel silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time
M5M2168P-55 55 ns (max)
M5M2168P-70 70 ns (max)
- Low power dissipation
Active 500 mW (typ)
Standby by 40 mW (typ)
- Power down by \bar{S}
- Single 5V power supply
- Fully static operation
Requires neither external clock nor refreshing
- All inputs and output are directly TTL compatible
- Easy memory expansion by chip-select (\bar{S}) input
- Interchangeable with Intel's 2168

APPLICATION

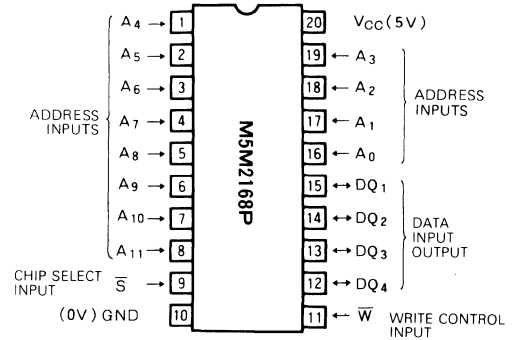
- High-speed memory systems

FUNCTION

A write operation is executed during the \bar{S} low and \bar{W} low overlap time. In this period, address signals must be stable. When \bar{W} is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting \bar{W} to high, and \bar{S} to low if the address signals are stable, the data is available at the DQ terminal.

PIN CONFIGURATION (TOP VIEW)

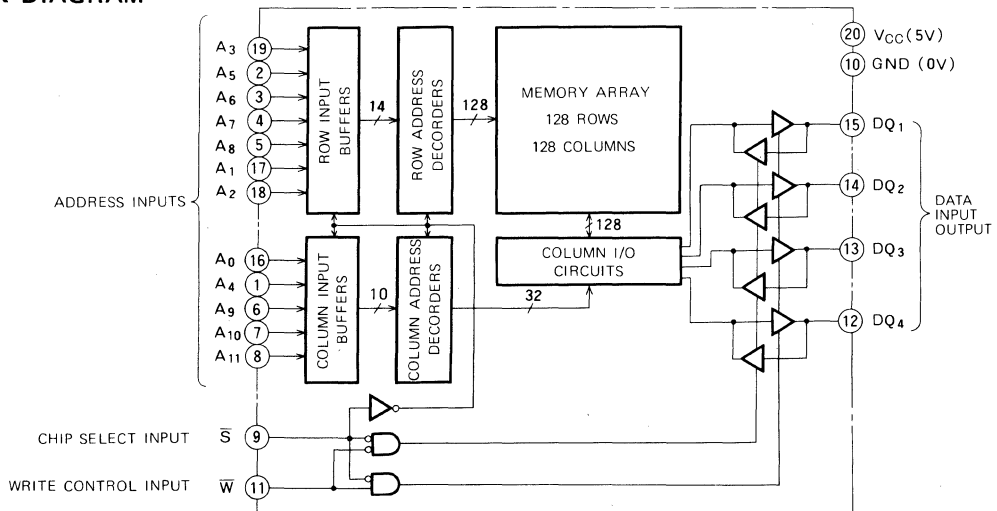


Outline 20 P4

When \bar{S} is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal \bar{S} controls the power-down feature. When \bar{S} goes high, power dissipation is reduced to 1/10 of active power. The access time from \bar{S} is equivalent to the address access time.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	$-3.5 \sim 7$	V
V_I	Input voltage		$-3.5 \sim 7$	V
V_O	Output voltage		$-3.5 \sim 7$	V
P_d	Maximum power dissipation		1	W
T_{opr}	Temperature under bias		$-10 \sim 85$	°C
T_{stg}	Storage temperature		$-65 \sim 150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	-3		0.8	V
V_{IH}	High-level input voltage	2		6	V

Necessary airflow cooling $> 2\text{m/s}$

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2		6	V
V_{IL}	Low-level input voltage		-3		0.8	V
V_{OH}	High-level output voltage	$I_{OH} = -4\text{ mA}$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8\text{ mA}$			0.4	V
I_I	Input current	$V_I = 0 \sim 5.5\text{ V}$			10	μA
$ I_{OZ} $	Off-state output current	$V_I(\bar{S}) = 2\text{ V}$, $V_O = 0 \sim V_{CC}$			50	μA
I_{CC1}	Supply current from V_{CC}	$V_I(\bar{S}) = 0.8\text{ V}$ Output open		$T_a = 25^\circ\text{C}$ $T_a = 0^\circ\text{C}$	100 150	mA
I_{CC2}	Stand by current	$V_I(\bar{S}) = 2\text{ V}$ output open		8	30	mA
I_{PO}	Peak power-on current	$V_{CC} = 0 \sim 4.5\text{ V}$ $V_I(\bar{S}) = \text{Lower of } V_{CC} \text{ or } V_{IH\text{min}}$			30	mA
C_I	Input capacitance	$V_I = \text{GND}$, $V_I = 25\text{ mVrms}$, $f = 1\text{ MHz}$			5	pF
C_O	Output capacitance	$V_O = \text{GND}$, $V_O = 25\text{ mVrms}$, $f = 1\text{ MHz}$			6	pF

Note 1. Current flow into an IC is positive, out is negative.

SWITCHING CHARACTERISTICS (FOR READ CYCLE) ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	M5M2168P-55			M5M2168P-70			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	55			70			ns
$t_a(\text{A})$	Address access time			55			70	ns
$t_a(\text{S})$	Chip select access time			55			70	ns
$t_v(\text{A})$	Data valid time after address	5			5			ns
$t_{en}(\text{S})$	Output enable time after chip selection	20			20			ns
$t_{dis}(\text{S})$	Output disable time after chip deselection	0		20	0		25	ns
t_{PU}	Power-up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			25			30	ns

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TIMING REQUIREMENTS (FOR WRITE CYCLE) ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	M5M2168P-55			M5M2168P-70			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{OW}	Write cycle time	50			60			ns
$t_{su(s)}$	Chip select setup time	45			55			ns
$t_{su(A)_1}$	Address setup time 1 (\overline{W} CONTROL)	0			0			ns
$t_{su(A)_2}$	Address setup time 2 (\overline{S} CONTROL)	0			0			ns
$t_{W(W)}$	Write pulse width	40			50			ns
$t_{rec(W)}$	Write recovery time	0			0			ns
$t_{su(D)}$	Data setup time	20			30			ns
$t_h(D)$	Data hold time	0			0			ns
$t_{dis(W)}$	Output disable time after \overline{W} low	0		25	0		30	ns
$t_{en(W)}$	Output enable time after \overline{W} high	5			5			ns
$t_{su(A-\overline{W}H)}$	Address to \overline{W} high	45			55			ns

CONDITIONS

Input pulse levels 0 to 3V
input rise and falltime 5 ns
Input timing reference level 1.5V
Output timing reference level 0.8~2V
Output load Fig. 1, Fig. 2

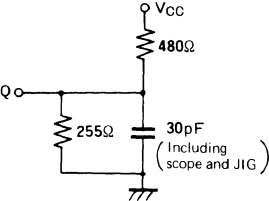


Fig. 1 Output load

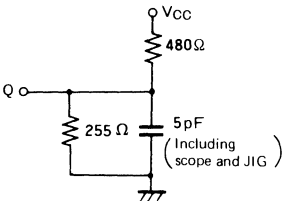
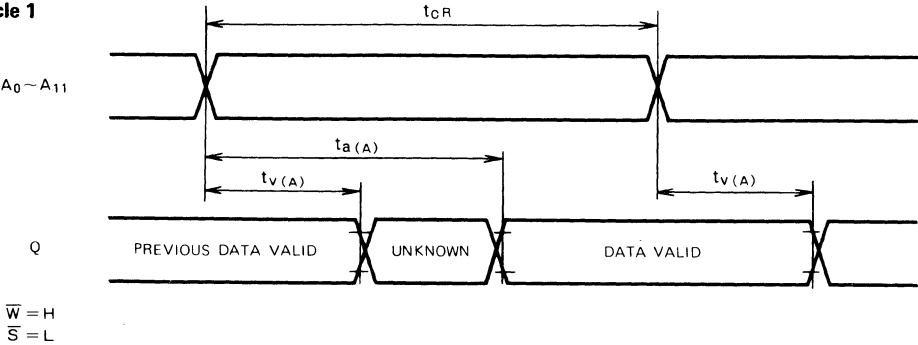


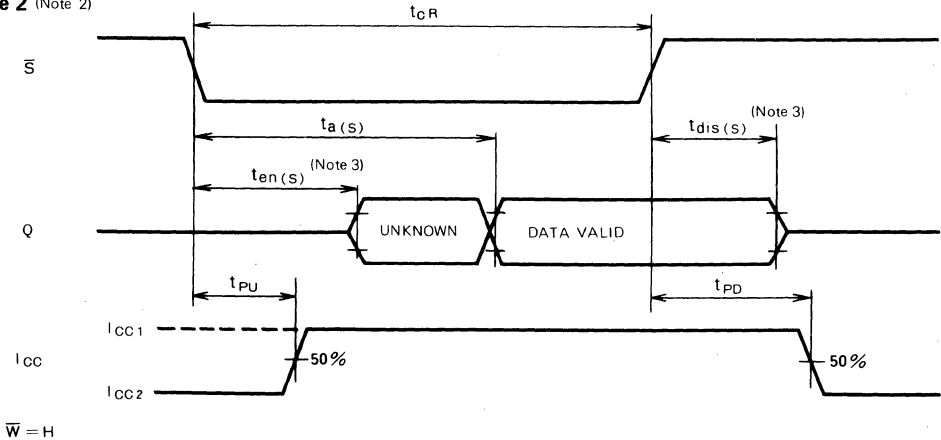
Fig. 2 Output load for ten, tdis

TIMING DIAGRAMS

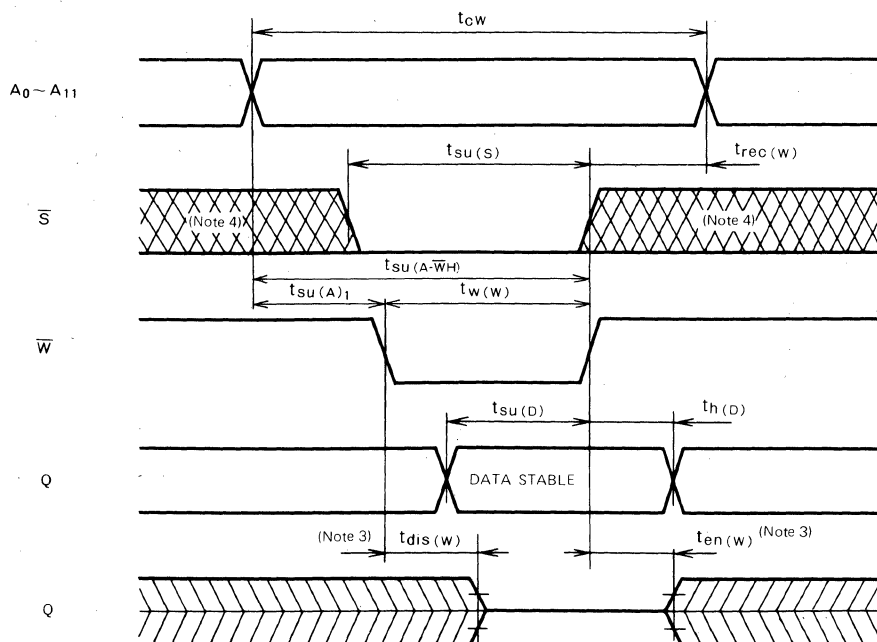
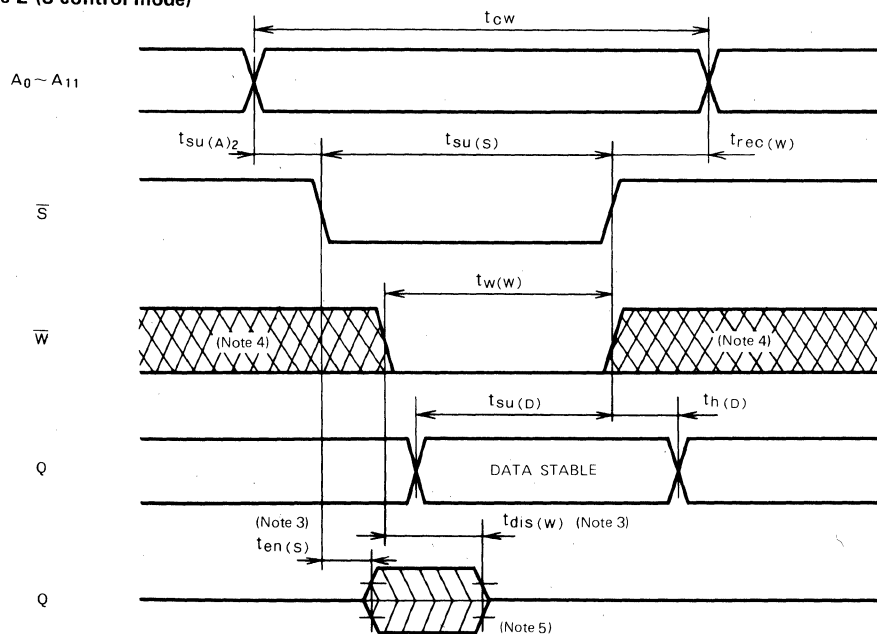
Read cycle 1



Read cycle 2 (Note 2)



Note 2. Addresses valid prior to or coincident with \overline{S} transition low.
3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Figure 2.

16384-BIT (4096-WORD BY 4-BIT) STATIC RAM**TIMING DIAGRAMS****Write cycle 1 (\overline{W} control mode)****Write cycle 2 (\overline{S} control mode)**

Note 4. Hatching indicates the state is don't care.

5. When the falling edge of \overline{W} is simultaneous or prior to the falling edge of \overline{S} , the output is maintained in the high impedance.