

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is low enough for battery back-up application.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M44405CXX-5,-5S	50	13	25	13	90	500
M5M44405CXX-6,-6S	60	15	30	15	110	400
M5M44405CXX-7,-7S	70	20	35	20	130	350

XX=J,TP

- Standard 26 pin SOJ, 26 pin TSOP(II)
 - Single 5V±10% supply
 - Low stand-by power dissipation
 - CMOS Input level ----- 5.5mW (Max) *
 - CMOS Input level ----- 550μW (Max)
 - Low operating power dissipation
 - M5M44405Cxx-5,-5S ----- 687.5mW (Max)
 - M5M44405Cxx-6,-6S ----- 550.0mW (Max)
 - M5M44405Cxx-7,-7S ----- 467.5mW (Max)
 - Self refresh capability *
 - Self refresh current ----- 120μA(max)
 - Extended refresh capability *
 - Extended refresh current ----- 120μA(max)
 - Hyper-page mode (1024-bit random access), Read-modify- write, RAS-only refresh CAS before RAS refresh, Hidden refresh, CBR self refresh(-5S,-6S,-7S) capabilities
 - Early-write mode and OE and W to control output buffer impedance
 - All inputs, output TTL compatible and low capacitance
 - 1024 refresh cycles every 16.4ms (A0~A9)
 - 1024 refresh cycle every 128ms (A0~A9) *
 - 4-bit parallel test mode capability
- * : Applicable to self refresh version (M5M44405CJ,TP-5S,-6S,-7S : option) only

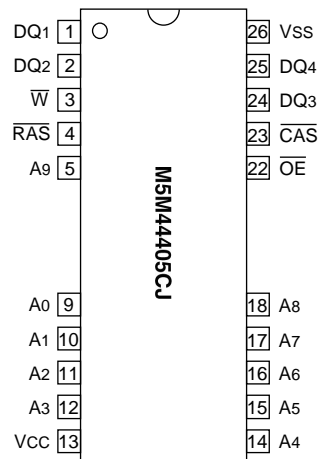
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT, Frame Buffer memory for CRT

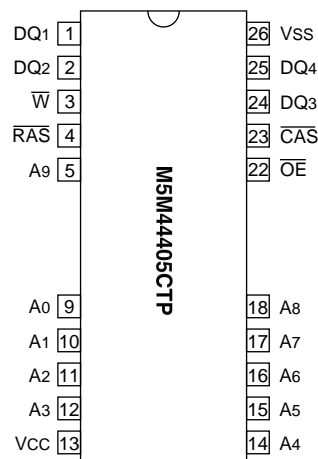
PIN DESCRIPTION

Pin name	Function
A0~A9	Address Inputs
DQ1~DQ4	Data Inputs / Outputs
RAS	Row Address Strobe Input
CAS	Column Address Strobe Input
W	Write Control Input
OE	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 26P0J (300mil SOJ)



Outline 26P3Z-E (300mil TSOP)

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

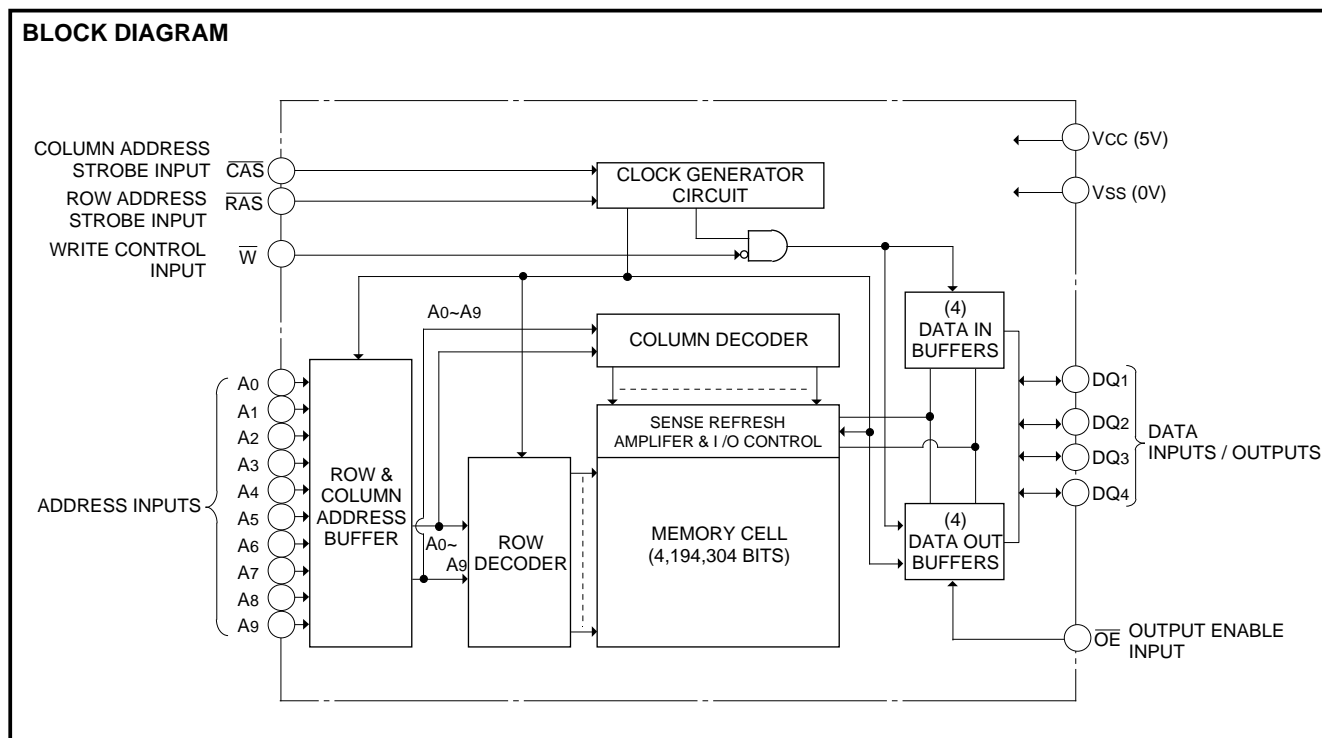
FUNCTION

The M5M44405CJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Hyper-Page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	APD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	NAC	APD	APD	APD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	APD	VLD	YES	
$\overline{\text{RAS}}$ -only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh *	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open



M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1~7	V
V _I	Input voltage		-1~7	V
V _O	Output voltage		-1~7	V
I _O	Output current	Ta=25°C	50	mA
P _d	Power dissipation		1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.0	V
V _{IL}	Low-level input voltage	DQ1~4	-1.0	0.8	V
		others	-2.0	0.8	V

Note 1 : All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}= 5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V _{OH}	High-level output voltage		I _{OH} = -5mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage		I _{OL} = 4.2mA	0		0.4	V
I _{OZ}	Off-state output current		Q floating 0V V _{OUT} 5.5V	-10		10	μA
I _I	Input current		0V V _{IN} +6.5V, Other inputs pins=0V	-10		10	μA
I _{CC1} (AV)	Average supply current from V _{CC} , operating (Note 3,4,5)	M5M44405C-5,-5S	RAS, CAS cycling trc=twc=min. output open			125	mA
		M5M44405C-6,-6S				100	
		M5M44405C-7,-7S				85	
I _{CC2} (AV)	Supply current from V _{CC} , stand-by (Note 6)	M5M44405C	RAS= CAS =V _{IH} , output open RAS= CAS V _{CC} -0.5V output open			2	mA
		M5M44405C(S)				1	
						0.1	
I _{CC3} (AV)	Average supply current from V _{CC} , refreshing (Note 3,5)	M5M44405C-5,-5S	RAS cycling, CAS= V _{IH} trc=min. output open			125	mA
		M5M44405C-6,-6S				100	
		M5M44405C-7,-7S				85	
I _{CC4} (AV)	Average supply current from V _{CC} , Hyper-Page-Mode (Note 3,4,5)	M5M44405C-5,-5S	RAS=V _{IL} , CAS cycling tpc=min. output open			125	mA
		M5M44405C-6,-6S				100	
		M5M44405C-7,-7S				85	
I _{CC6} (AV)	Average supply current from V _{CC} , CAS before RAS refresh mode (Note 3)	M5M44405C-5,-5S	CAS before RAS refresh cycling trc=min. output open			105	mA
		M5M44405C-6,-6S				85	
		M5M44405C-7,-7S				75	
I _{CC8} (AV)	Average supply current from V _{CC} , Extended-Refresh cycle (Note 6)		RAS cycling CAS 0.2V or CAS before RAS refresh cycling RAS 0.2V or V _{CC} -0.2V CAS 0.2V or V _{CC} -0.2V W 0.2V(Except for RAS falling edge) or V _{CC} -0.2V OE 0.2V or V _{CC} -0.2V A0~A9 0.2V or V _{CC} -0.2V, DQ=open trc=125μs, tRAS=tRAS min~1μs			120	μA
I _{CC9} (AV)	Average supply current from V _{CC} , Self-Refresh cycle (Note 6)	M5M44405C(S)	RAS=CAS 0.2V output open			120	μA

Note 2 : Current flowing into an IC is positive, out is negative.

3 : I_{CC1}(AV), I_{CC3} (AV), I_{CC4}(AV) and I_{CC6}(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4 : I_{CC1}(AV) and I_{CC4}(AV) are dependent on output loading. Specified values are obtained with the output open.

5 : Column Address can be changed once or less while RAS=V_{IL} and CAS=V_{IH}.

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (A)	Input capacitance, address inputs	Vi=Vss f=1MHz Vi=25mVrms			5	pF
CI (CLK)	Input capacitance, clock inputs				7	pF
CI / O	Input/Output capacitance, data ports				7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 7,8)		13		15		20	ns
tRAC	Access time from $\overline{\text{RAS}}$ (Note 7,9)		50		60		70	ns
tAA	Column address access time (Note 7,10)		25		30		35	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		28		33		38	ns
toEA	Access time from $\overline{\text{OE}}$ (Note 7)		13		15		20	ns
toHC	Output hold time from $\overline{\text{CAS}}$	5		5		5		ns
toHR	Output hold time from $\overline{\text{RAS}}$ (Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{\text{CAS}}$ low (Note 7)	5		5		5		ns
toEZ	Output disable time after $\overline{\text{OE}}$ high (Note 12)		13		15		20	ns
tWEZ	Output disable time after $\overline{\text{WE}}$ high (Note 12)		13		15		20	ns
toFF	Output disable time after $\overline{\text{CAS}}$ high (Note 12,13)		13		15		20	ns
tREZ	Output disable time after $\overline{\text{RAS}}$ high (Note 12,13)		13		15		20	ns

Note 6 : An initial pause of 200µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles).

Note the $\overline{\text{RAS}}$ may be cycled during the initial pause . And eight initialization cycles are required after prolonged periods (greater than $t_{\text{REF(max)}}$) of $\overline{\text{RAS}}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 2TTL and 100pF.

The reference levels for measuring of output signals are 2.0V(VOH) and 0.8V(VOL).

8 : Assumes that t_{RCD} $t_{\text{RCD(max)}}$ and t_{ASC} $t_{\text{ASC(max)}}$ and t_{CP} $t_{\text{CP(max)}}$.

9 : Assumes that t_{RCD} $t_{\text{RCD(max)}}$ and t_{RAD} $t_{\text{RAD(max)}}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10 : Assumes that t_{RAD} $t_{\text{RAD(max)}}$ and t_{ASC} $t_{\text{ASC(max)}}$.

11 : Assumes that t_{CP} $t_{\text{CP(max)}}$ and t_{ASC} $t_{\text{ASC(max)}}$.

12 : $t_{\text{OEZ(max)}}$, $t_{\text{WEZ(max)}}$, $t_{\text{OFF(max)}}$ and $t_{\text{REZ(max)}}$ defines the time at which the output achieves the high impedance state ($I_{\text{OUT}} \leq \pm 10\mu\text{A}$) and is not reference to $V_{\text{OH(min)}}$ or $V_{\text{OL(max)}}$.

13 : Output is disabled after both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ go to high.

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4		16.4	ms
tREF	Refresh cycle time *		128		128		128	ms
tRP	RAS high pulse width	30		40		50		ns
trCD	Delay time, RAS low to CAS low (Note 16)	18	37	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low	5		5		5		ns
trPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	8		10		13		ns
trAD	Column address delay time from RAS low (Note 17)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note 18)	0	10	0	13	0	13	ns
trAH	Row address hold time after RAS low	8		10		10		ns
tCAH	Column address hold time after CAS low	8		10		10		ns
tdZC	Delay time, data to CAS low (Note 19)	0		0		0		ns
tdZO	Delay time, data to OE low (Note 19)	0		0		0		ns
trDD	Delay time, RAS high to data (Note 20)	13		15		20		ns
tcDD	Delay time, CAS high to data (Note 20)	13		15		20		ns
tODD	Delay time, OE high to data (Note 20)	13		15		20		ns
tT	Transition time (Note 21)	1	50	1	50	1	50	ns

Note 14 : The timing requirements are assumed TT=2ns.

15 : VIH(min) and VIL(max) are reference levels for measuring timing of input signals.

16 : trCD(max) is specified as a reference point only. If trCD is less than trCD(max), access time is tRAC. If trCD is greater than trCD(max), access time is controlled exclusively by tCAC or tAA.

17 : trAD(max) is specified as a reference point only. If trAD trAD(max) and tASC tASC(max), access time is controlled exclusively by tAA.

18 : tASC(max) is specified as a reference point only. If trCD trCD(max) and tASC tASC(max), access time is controlled exclusively by tCAC.

19 : Either tdZC or tdZO must be satisfied.

20 : Either trDD or tcDD or tODD must be satisfied.

21 : tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tRCS	Read Setup time before CAS low	0		0		0		ns
tRCH	Read hold time after CAS high (Note 22)	0		0		0		ns
tRRH	Read hold time after RAS high (Note 22)	0		0		0		ns
tRAL	Column address to RAS hold time	25		30		35		ns
tCAL	Column address to CAS hold time	13		18		23		ns
tORH	RAS hold time after OE low	13		15		20		ns
tOCH	CAS hold time after OE low	13		15		20		ns

Note 22 : Either trCH or trRH must be satisfied for a read cycle.

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
trSH	RAS hold time after CAS low	13		15		20		ns
twCS	Write setup time before CAS low (Note 24)	0		0		0		ns
twCH	Write hold time after CAS low	8		10		13		ns
tcWL	CAS hold time after W low	8		10		13		ns
trWL	RAS hold time after W low	8		10		13		ns
tWP	Write pulse width	8		10		13		ns
tDS	Data setup time before CAS low or W low	0		0		0		ns
tDH	Data hold time after CAS low or W low	8		10		13		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
trWC	Read write/read modify write cycle time (Note 23)	109		133		161		ns
trAS	RAS low pulse width	75	10000	89	10000	107	10000	ns
tCAS	CAS low pulse width	38	10000	44	10000	57	10000	ns
tCSH	CAS hold time after $\overline{\text{RAS}}$ low	75		89		107		ns
trSH	RAS hold time after $\overline{\text{CAS}}$ low	38		44		57		ns
trCS	Read setup time before $\overline{\text{CAS}}$ low	0		0		0		ns
tCWD	Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{W}}$ low (Note 24)	28		32		42		ns
trWD	Delay time, RAS low to $\overline{\text{W}}$ low (Note 24)	65		77		92		ns
tAWD	Delay time, address to $\overline{\text{W}}$ low (Note 24)	40		47		57		ns
toEH	$\overline{\text{OE}}$ hold time after $\overline{\text{W}}$ low	13		15		20		ns

Note 23 : trWC is specified as trWC(min)=tRAC(max)+tODD(min)+trWL(min)+trP(min)+4tT.

24 : twCS, tcWD, trWD and tAWD and, tcpWD are specified as reference points only. If twCS twCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tcWD tcWD(min), trWD trWD(min), tAWD tAWD(min) and tcpWD tcpWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Hyper page Mode Cycle

(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by \overline{OE} or \overline{W}) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time (Note 26)	20		25		30		ns
tHPRWC	Hyper Page Mode read write/read modify write cycle time	57		66		79		ns
tDOH	Output hold time from \overline{CAS} low	5		5		5		ns
tRAS	RAS low pulse width for read or write cycle (Note 27)	65	100000	77	100000	92	100000	ns
tCP	\overline{CAS} high pulse width (Note 28)	8	13	10	16	13	16	ns
tCPRH	RAS hold time after \overline{CAS} precharge	28		33		38		ns
tCPWD	Delay time, \overline{CAS} precharge to \overline{W} low (Note 24)	43		50		60		ns
tCHOL	Hold time to maintain the data Hi-Z until \overline{CAS} access	7		7		7		ns
tOEPE	\overline{OE} Pulse Width (Hi-Z control)	7		7		7		ns
tWPE	\overline{W} Pulse Width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, \overline{CAS} low to \overline{W} low after read	28		32		42		ns
tHAWD	Delay time, Address to \overline{W} low after read	40		47		57		ns
tHPWD	Delay time, \overline{CAS} precharge to \overline{W} low after read	43		50		60		ns
tHCOD	Delay time, \overline{CAS} low to \overline{OE} high after read	13		15		20		ns
tHAOD	Delay time, Address to \overline{OE} high after read	25		30		35		ns
tHPOD	Delay time, \overline{CAS} precharge to \overline{OE} high after read	28		33		38		ns

Note 25 : All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

26 : tHPC(min) is specified in the case of read-only and early write-only in Hyper Page Mode.

27 : tRAS(min) is specified as two cycles of CAS input are performed.

28 : tCP(max) is specified as a reference point only.

CAS before RAS Refresh Cycle (Note 29)

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{\text{CAS}}$ setup time before $\overline{\text{RAS}}$ low	5		5		5		ns
tCHR	CAS hold time after RAS low	10		10		15		ns
tRSR	Read setup time before $\overline{\text{RAS}}$ low	10		10		10		ns
tRHR	Read hold time after $\overline{\text{RAS}}$ low	10		10		15		ns
tCAS	$\overline{\text{CAS}}$ low pulse width	17		17		22		ns

Note 29 : Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

Self Refresh Cycle * (Note 30)

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	CBR self refresh $\overline{\text{RAS}}$ low pulse width	100		100		100		ns
tRPS	CBR self refresh RAS high precharge time	90		110		130		ns
tCHS	CBR self refresh $\overline{\text{CAS}}$ hold time	- 50		- 50		- 50		ns
tRSR	Read setup time before RAS low	10		10		10		ns
tRHR	Read hold time after $\overline{\text{RAS}}$ low	10		10		15		ns

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Test Mode Specification (Note 31)

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ICC1(AV)	Average supply current from Vcc, operating (Note 3,4,5)	RAS, CAS cycling trc=twc=min. output open			145	mA
					115	
					100	
ICC3(AV)	Average supply current from Vcc, refreshing (Note 3,5)	RAS cycling, CAS=VIH trc=min. output open			145	mA
					115	
					100	
ICC4(AV)	Average supply current from Vcc, Hyper-Page-Mode (Note 3,4,5)	RAS=VIL, CAS cycling tpc=min. output open			145	mA
					115	
					100	
ICC6(AV)	Average supply current from Vcc, CAS before RAS refresh mode (Note 3)	CAS before RAS refresh cycling trc=min. output open			120	mA
					100	
					85	

Note 31 : All previously specified electrical characteristics, switing characteristics, and timing requirements are applicable to that of test mode.

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{\text{CAS}}$ (Note 7,8)		18		20		25	ns
tRAC	Access time from RAS (Note 7,9)		55		65		75	ns
tAA	Column address access time (Note 7,10)		30		35		40	ns
tCPA	Access time from $\overline{\text{CAS}}$ precharge (Note 7,11)		33		38		43	ns
tOEA	Access time from $\overline{\text{OE}}$ (Note 7)		18		20		25	ns

TIMING REQUIREMENTS (Ta=0~70°C, Vcc= 5V±10%, Vss=0V, unless otherwise noted, see notes 14,15)

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	95		115		135		ns
tRAS	RAS low pulse width	55	10000	65	10000	75	10000	ns
tCAS	CAS low pulse width	13	10000	15	10000	18	10000	ns
tCSH	CAS hold time after $\overline{\text{RAS}}$ low	45		53		60		ns
tRSH	RAS hold time after $\overline{\text{CAS}}$ low	18		20		25		ns
tRAL	Column address to $\overline{\text{RAS}}$ hold time	30		35		40		ns
tCAL	Column address to $\overline{\text{CAS}}$ hold time	18		23		28		ns
tORH	RAS hold time after $\overline{\text{OE}}$ low	18		20		25		ns
tOCH	CAS hold time after $\overline{\text{OE}}$ low	18		20		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note 23)	114		138		166		ns
tRAS	RAS low pulse width	80	10000	94	10000	112	10000	ns
tCAS	CAS low pulse width	43	10000	49	10000	62	10000	ns
tCSH	CAS hold time after RAS low	80		94		112		ns
tRSH	RAS hold time after CAS low	43		49		62		ns
tCWD	Delay time, CAS low to \overline{W} low (Note 24)	33		37		47		ns
tRWD	Delay time, RAS low to \overline{W} low (Note 24)	70		82		97		ns
tAWD	Delay time, address to \overline{W} low (Note 24)	45		52		62		ns

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Hyper page Mode Cycle

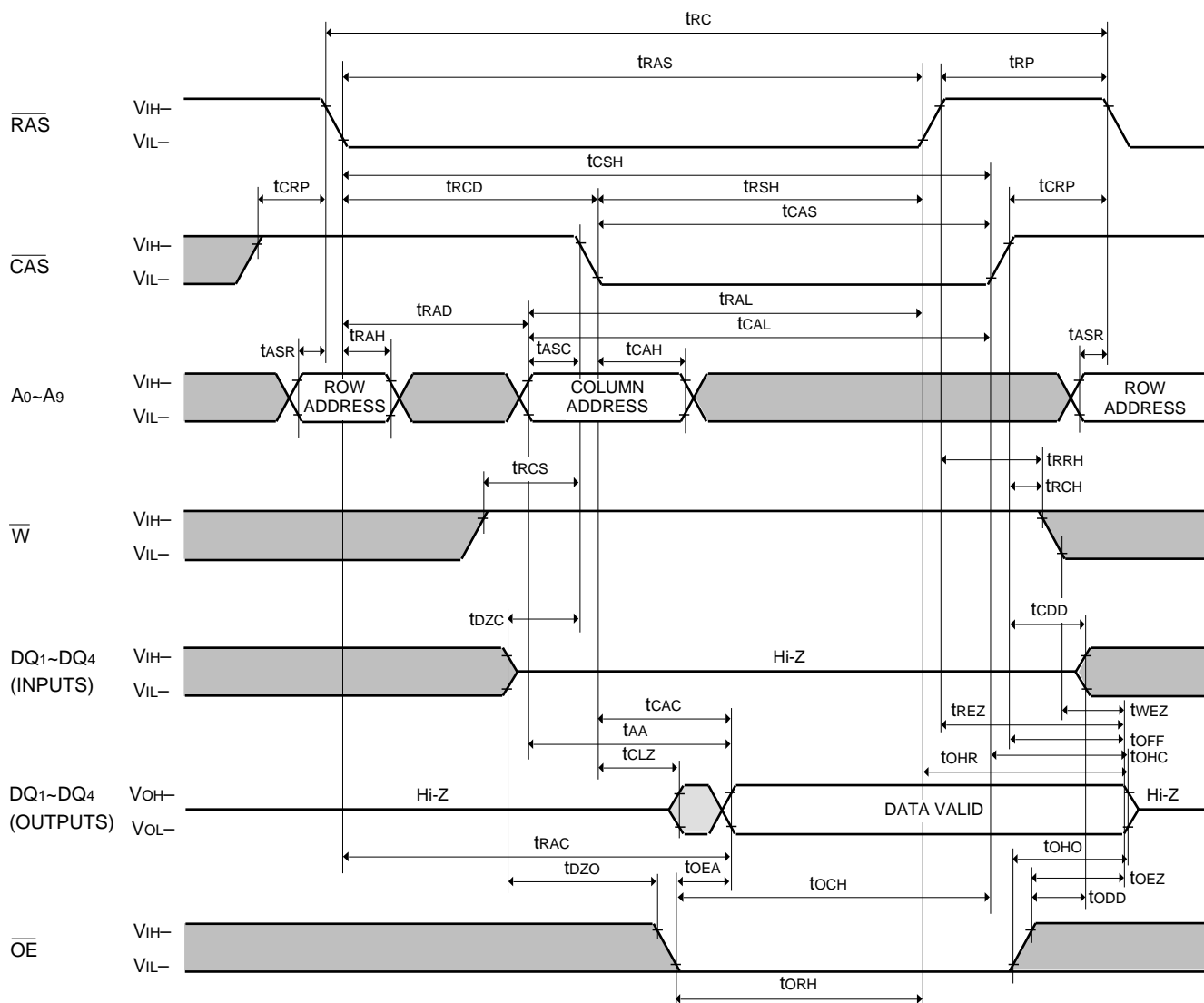
(Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by \overline{OE} or \overline{W}) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time (Note 26)	25		30		35		ns
tHPRWC	Hyper Page Mode read write/read modify write cycle time	62		71		84		ns
tRAS	RAS low pulse width for read or write cycle (Note 27)	70	100000	82	100000	97	100000	ns
tCPRH	RAS hold time after CAS precharge	33		38		43		ns
tCPWD	Delay time, CAS precharge to W low (Note 24)	48		55		65		ns
tHCWD	Delay time, CAS low to W low after read	33		37		47		ns
tHAWD	Delay time, Address to W low after read	45		52		62		ns
tHPWD	Delay time, CAS precharge to W low after read	48		55		65		ns
tHCOD	Delay time, CAS low to OE high after read	18		20		25		ns
tHAOD	Delay time, Address to OE high after read	30		35		40		ns
tHPOD	Delay time, CAS precharge to OE high after read	33		38		43		ns

Test Mode Set Cycle

Symbol	Parameter	Limits						Unit
		M5M44405C-5,-5S		M5M44405C-6,-6S		M5M44405C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	Write setup time before $\overline{\text{RAS}}$ low	10		10		10		ns
tWHR	Write hold time after $\overline{\text{RAS}}$ low	10		10		15		ns

Timing Diagram (Note 32) Read Cycle

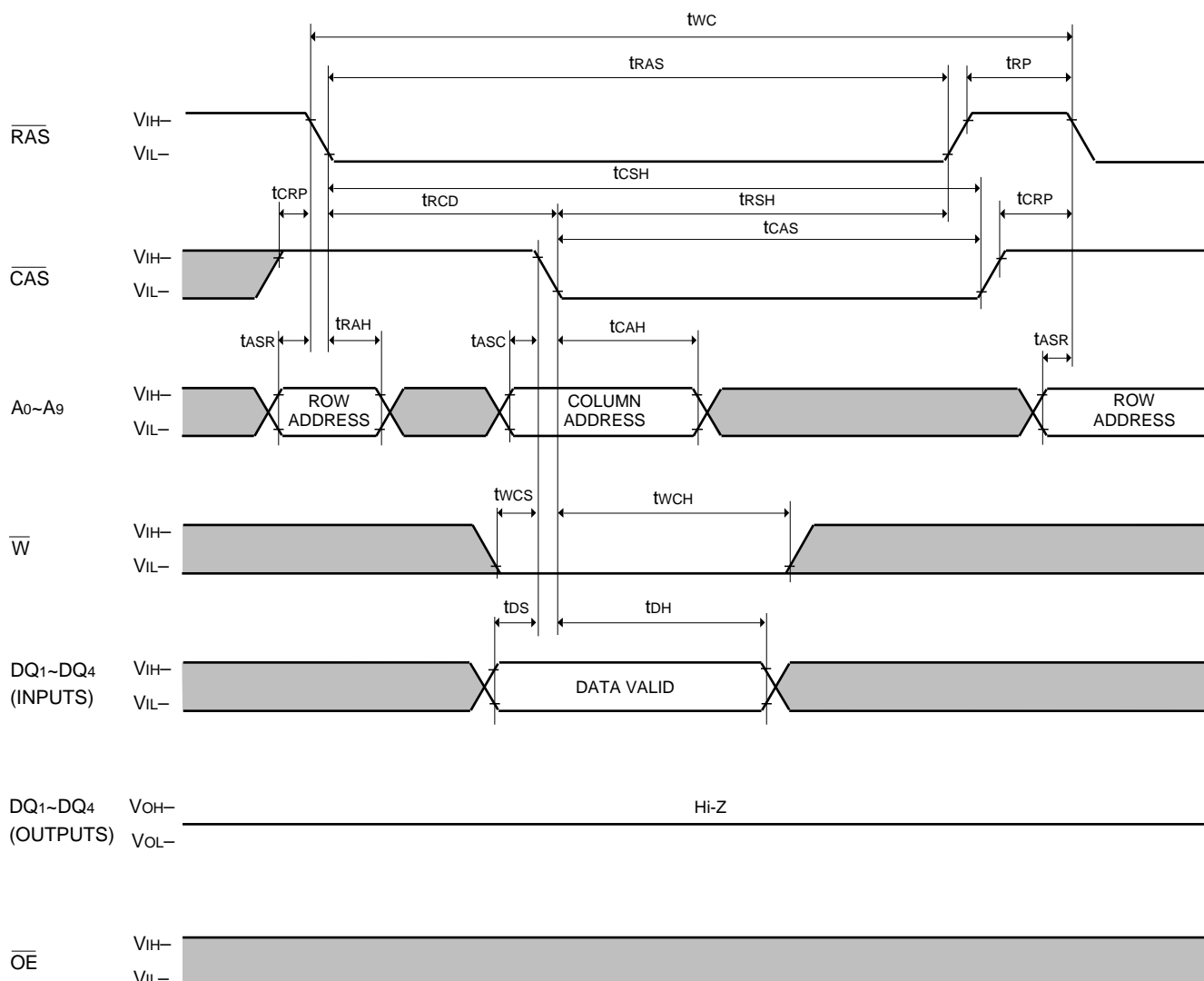


Indicates the invalid output.

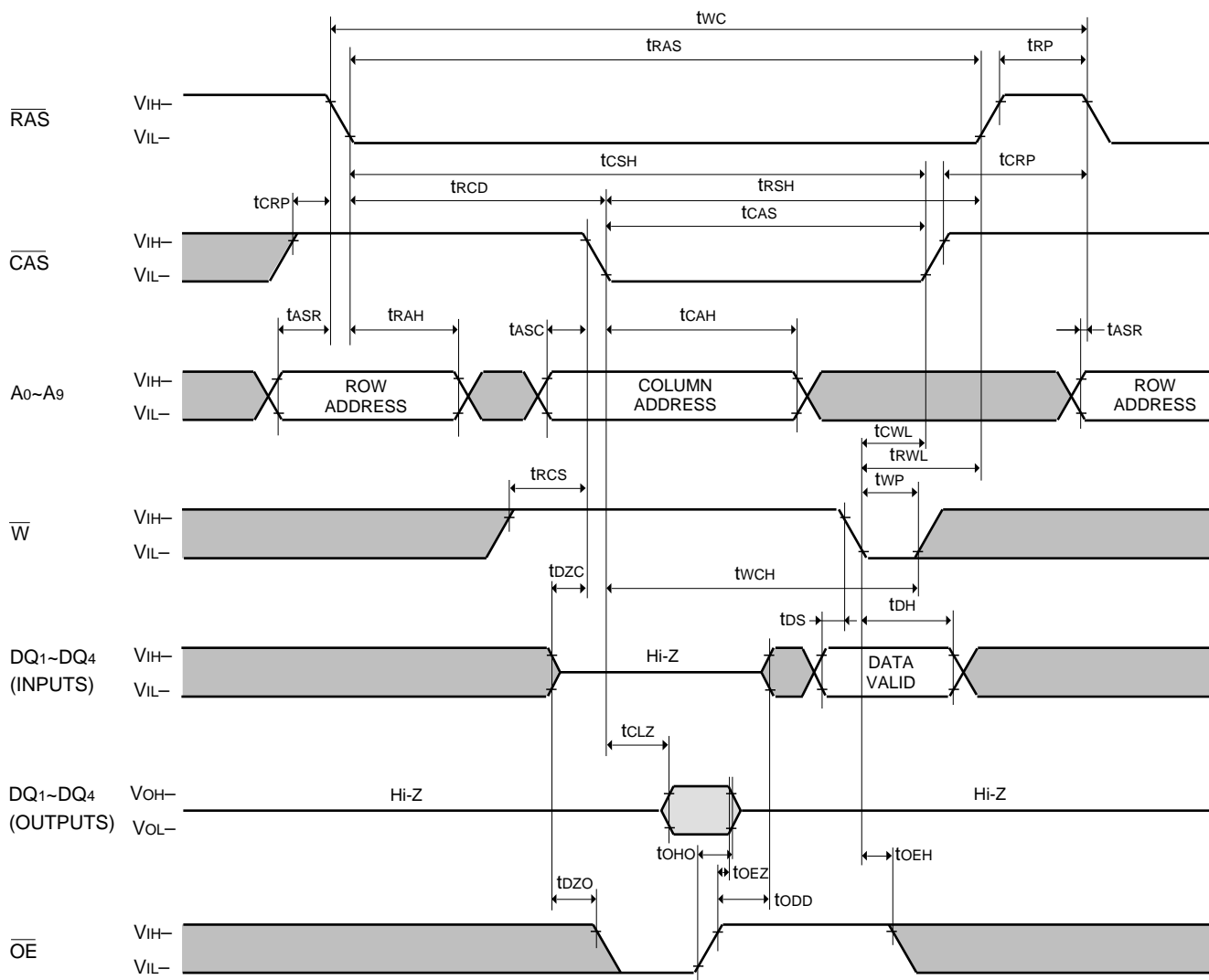
M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Early Write Cycle



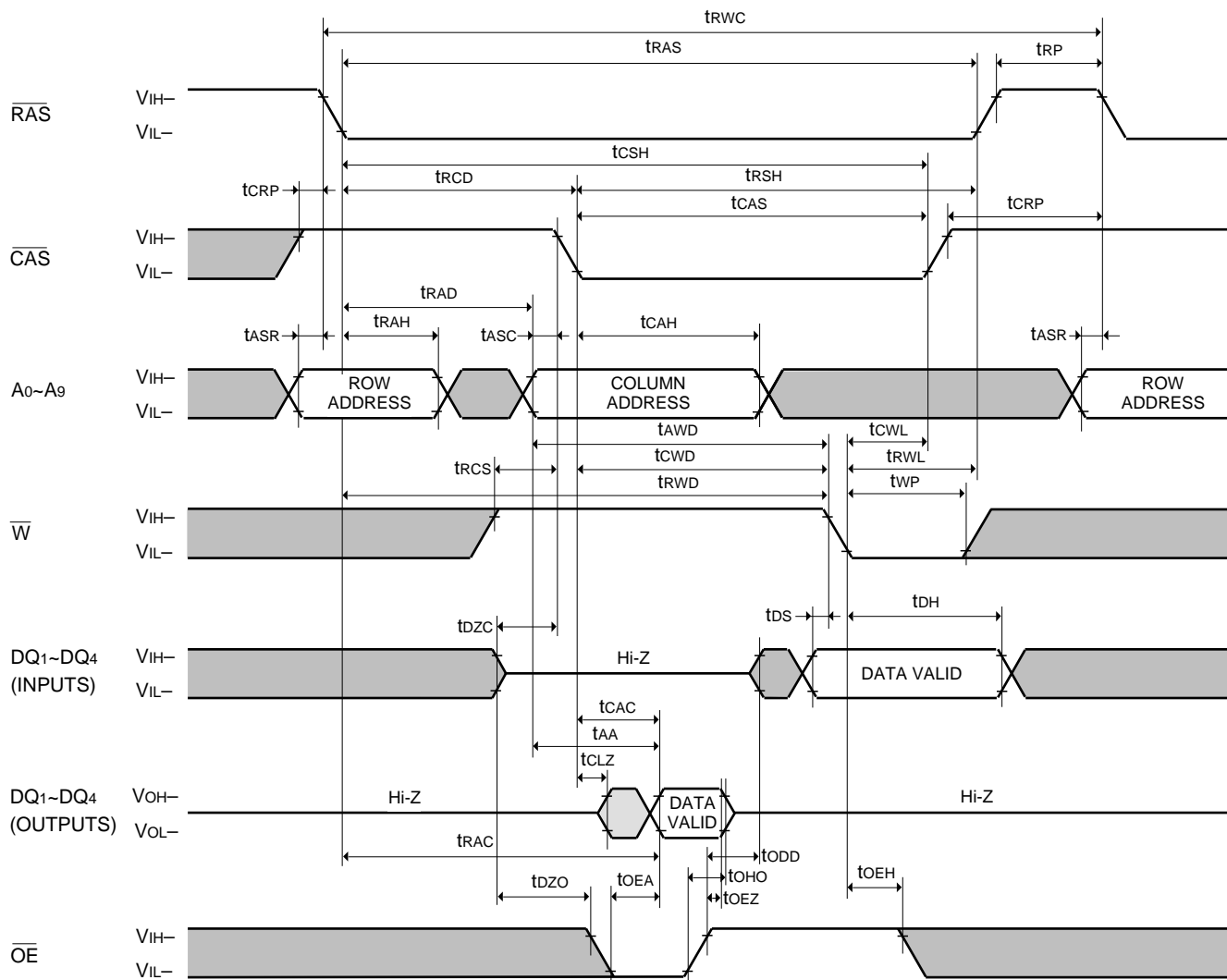
Delayed Write Cycle



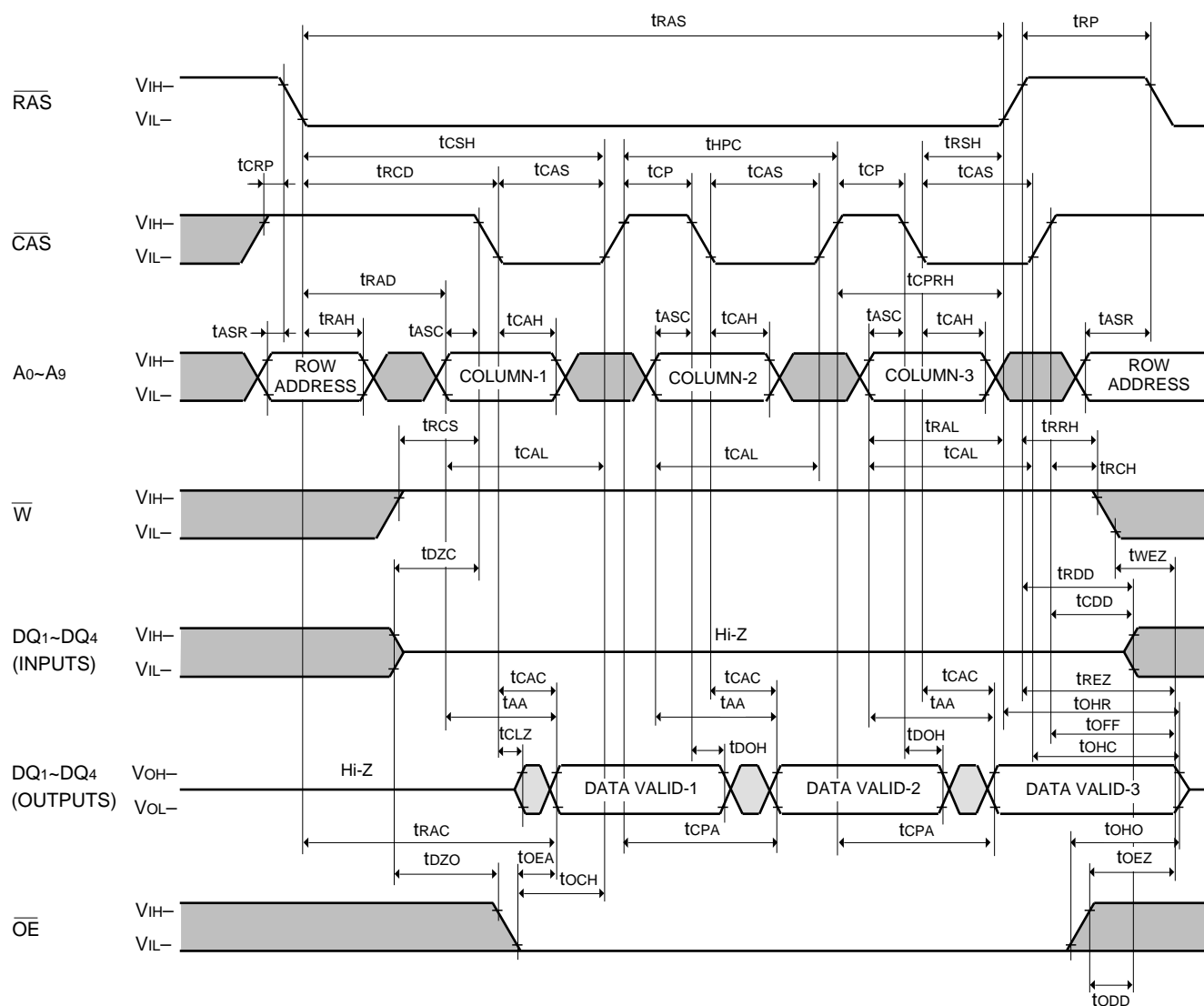
M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Read-Write, Read-Modify-Write Cycle



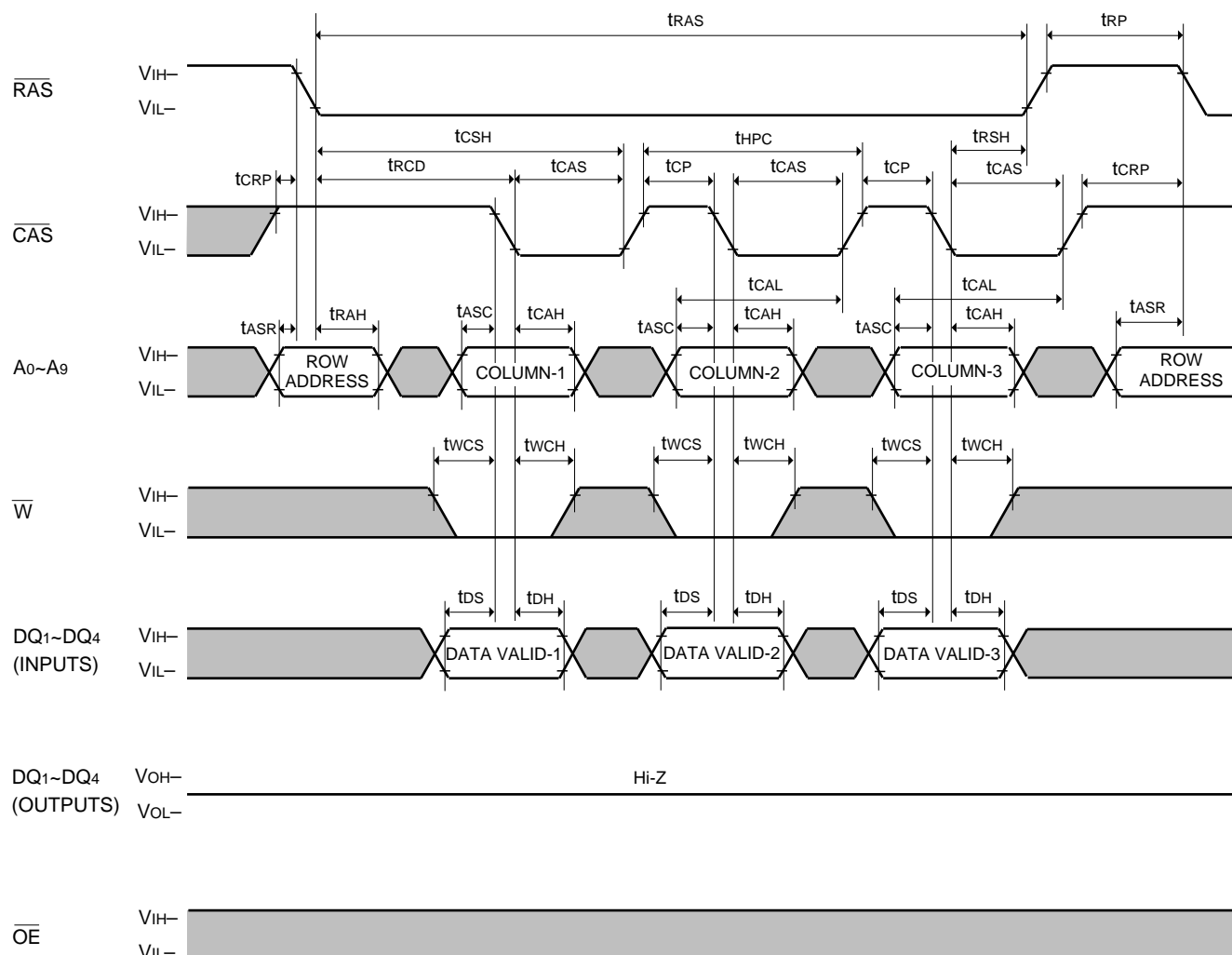
Hyper Page Mode Read Cycle



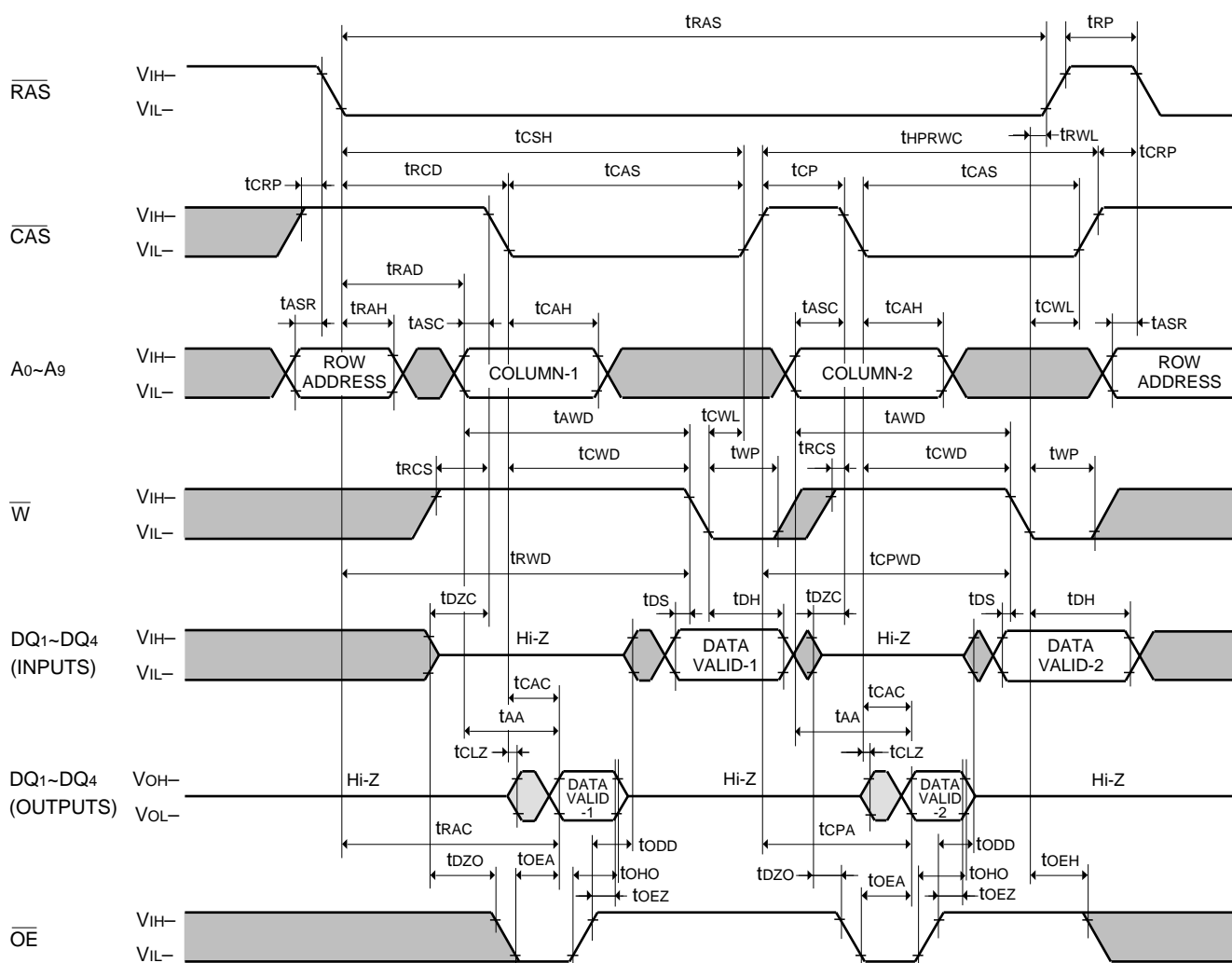
M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

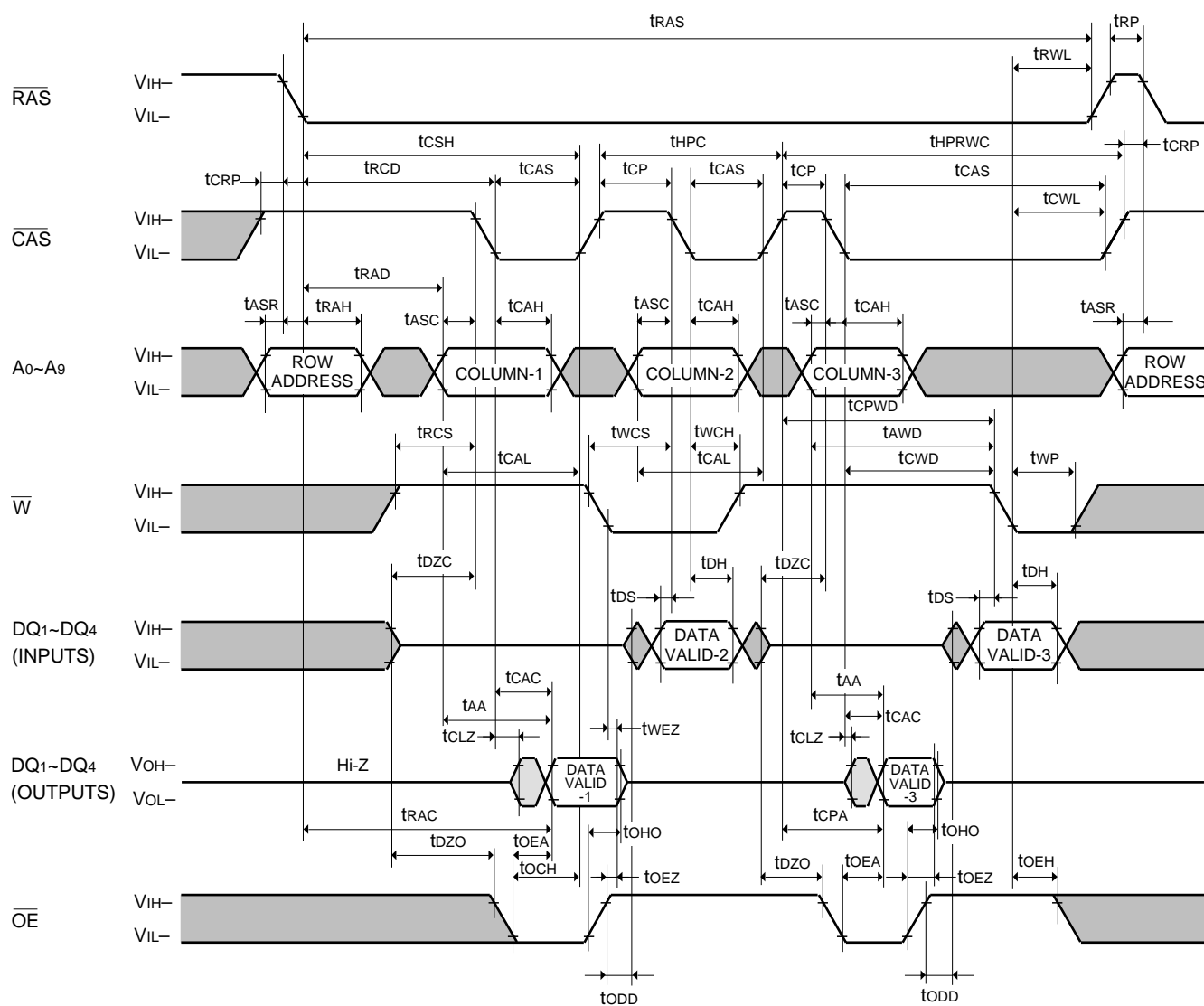
Hyper Page Mode Early Write Cycle



Hyper Page Mode Read-Write, Read-Modify-Write Cycle



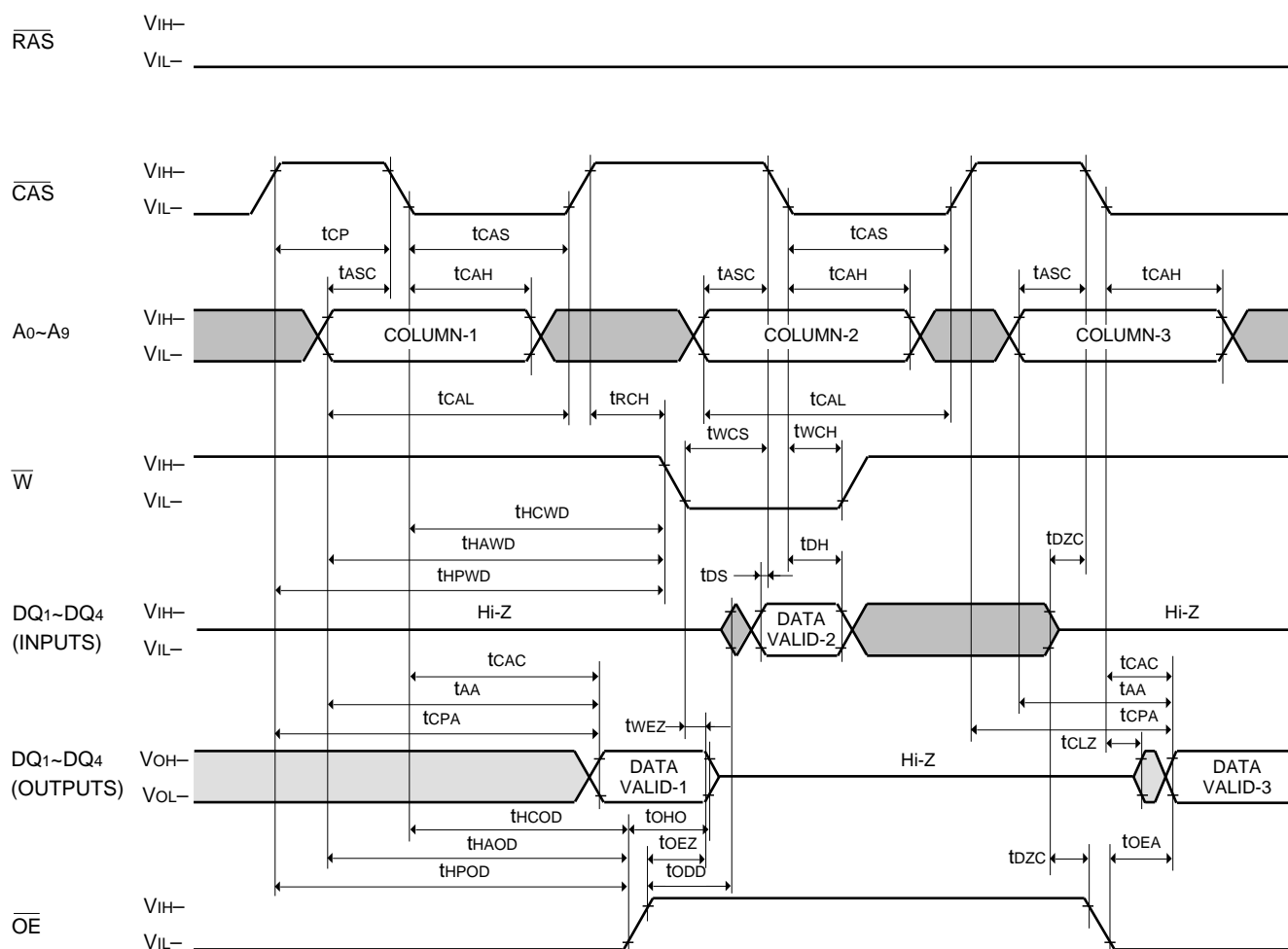
Hyper Page Mode Mix Cycle (1)



M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

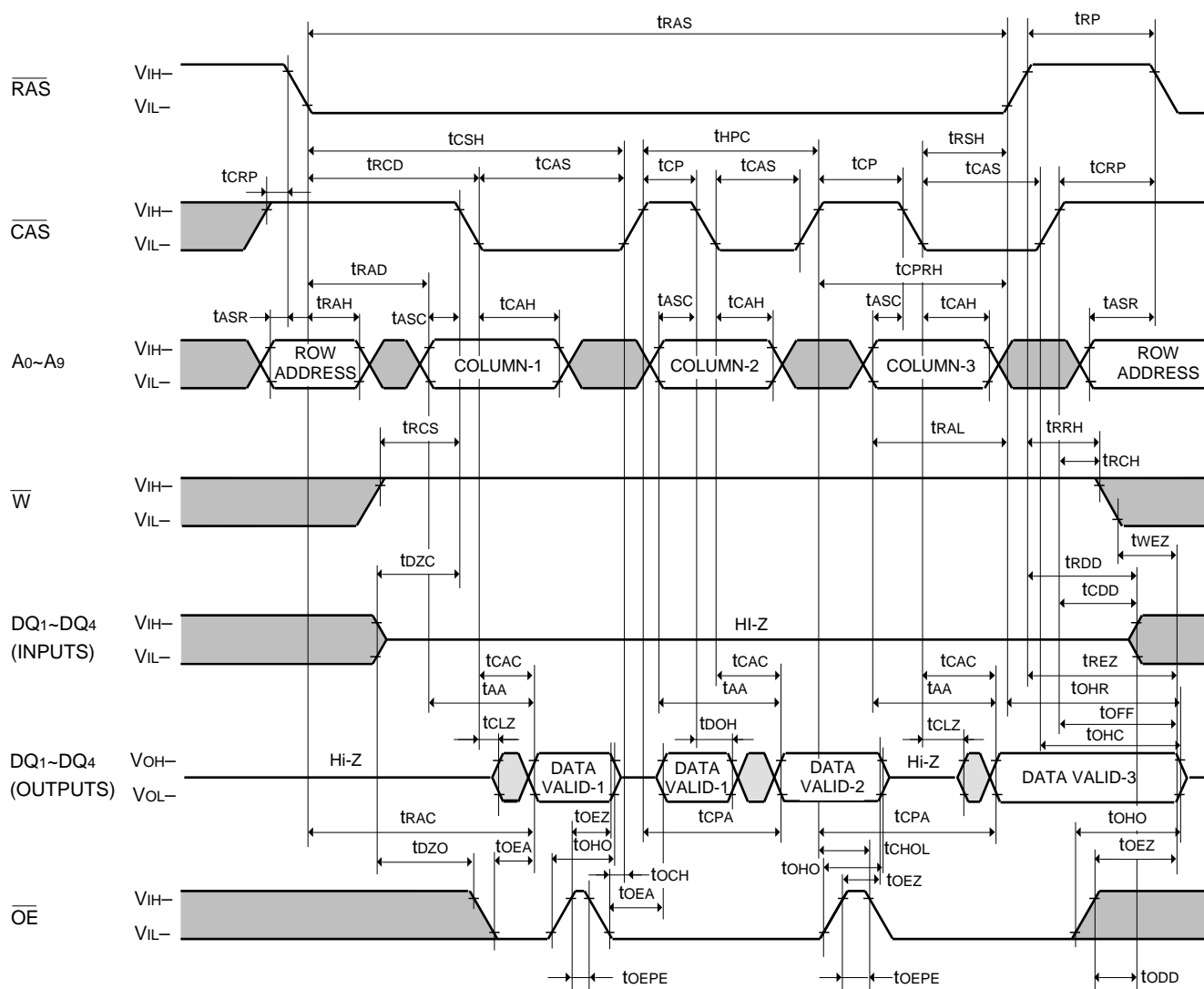
Hyper Page Mode Mix Cycle (2)



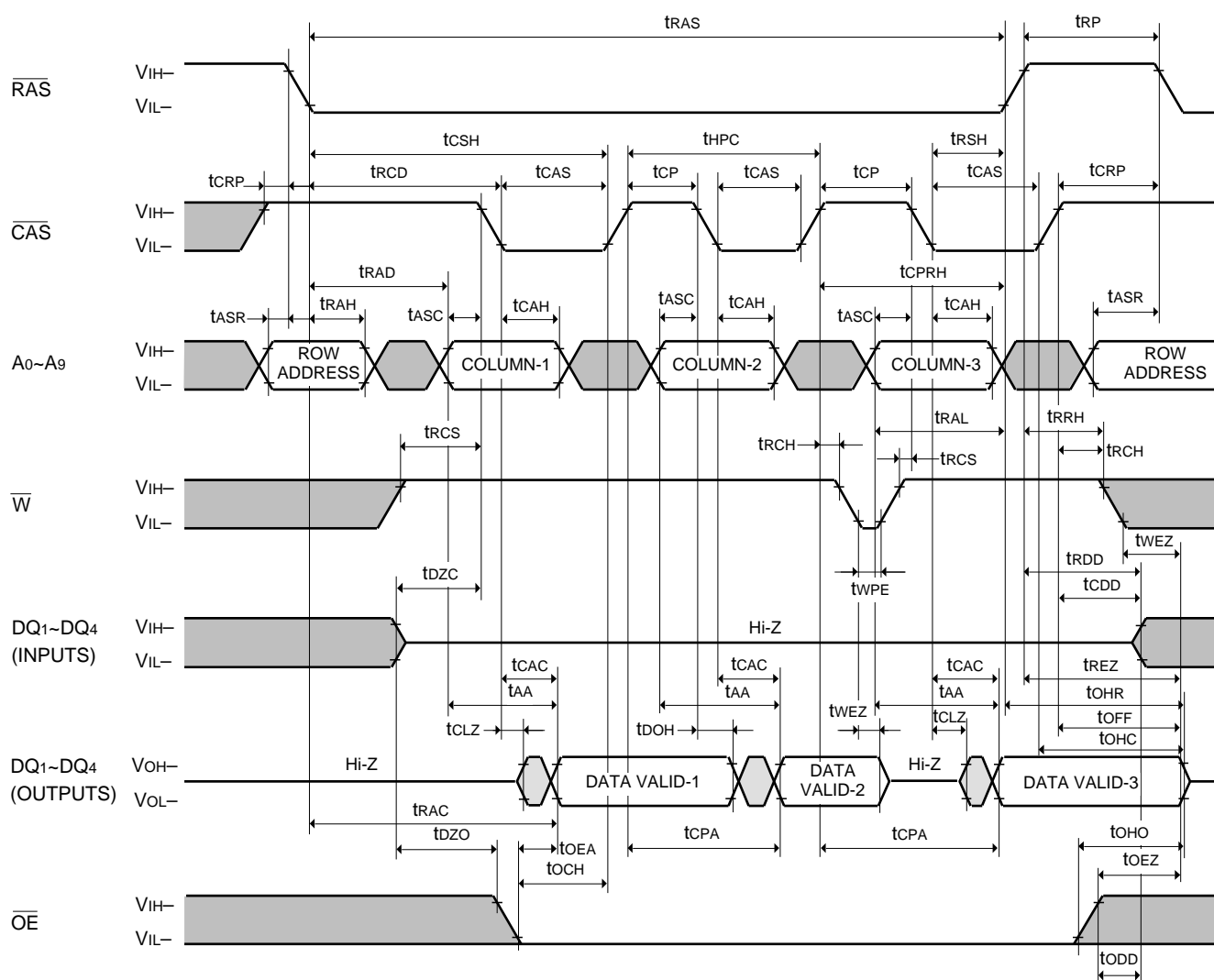
M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

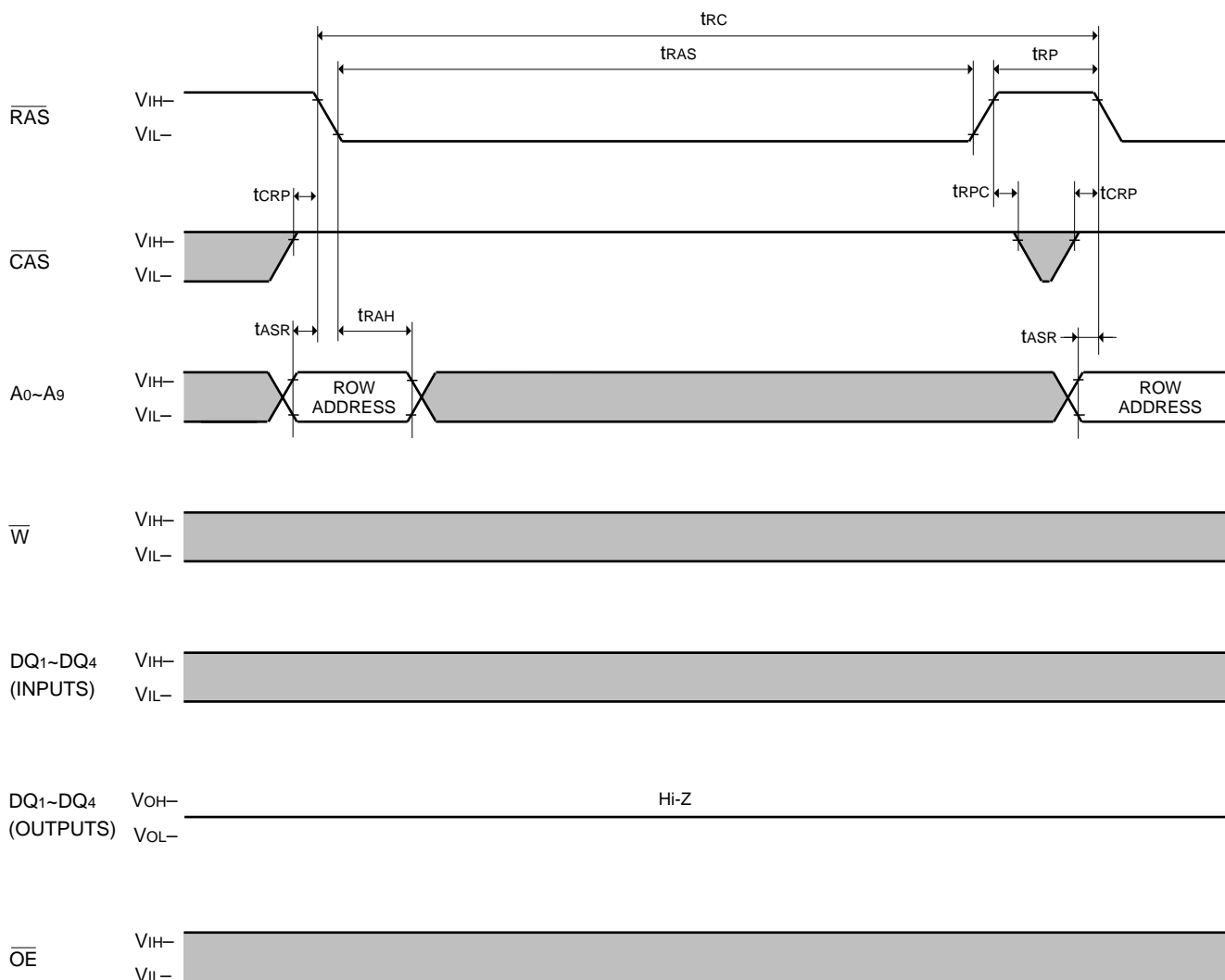
Hyper Page Mode Read Cycle (Hi-Z control by \overline{OE})



Hyper Page Mode Read Cycle (Hi-Z control by \overline{W})



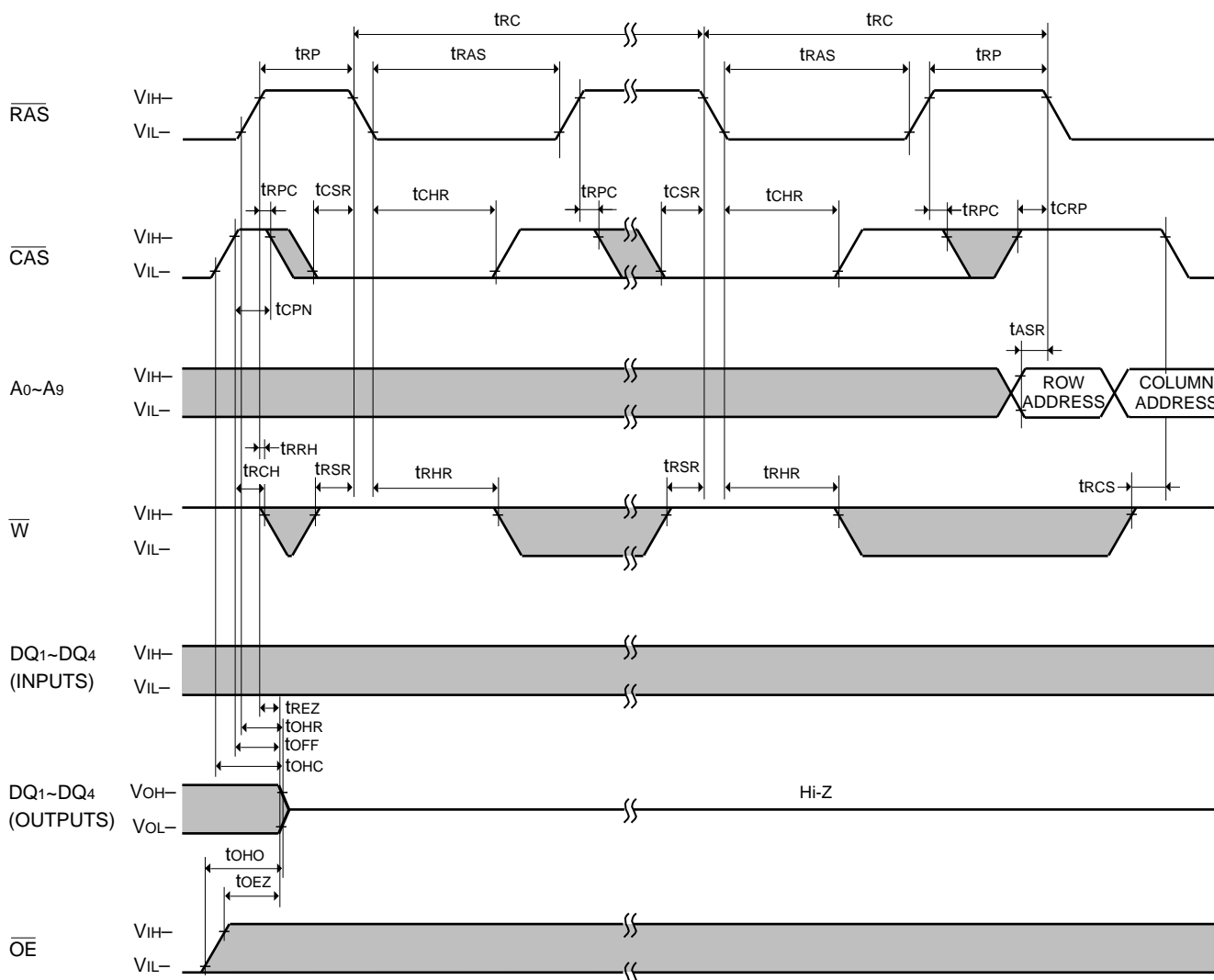
RAS-only Refresh Cycle



M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

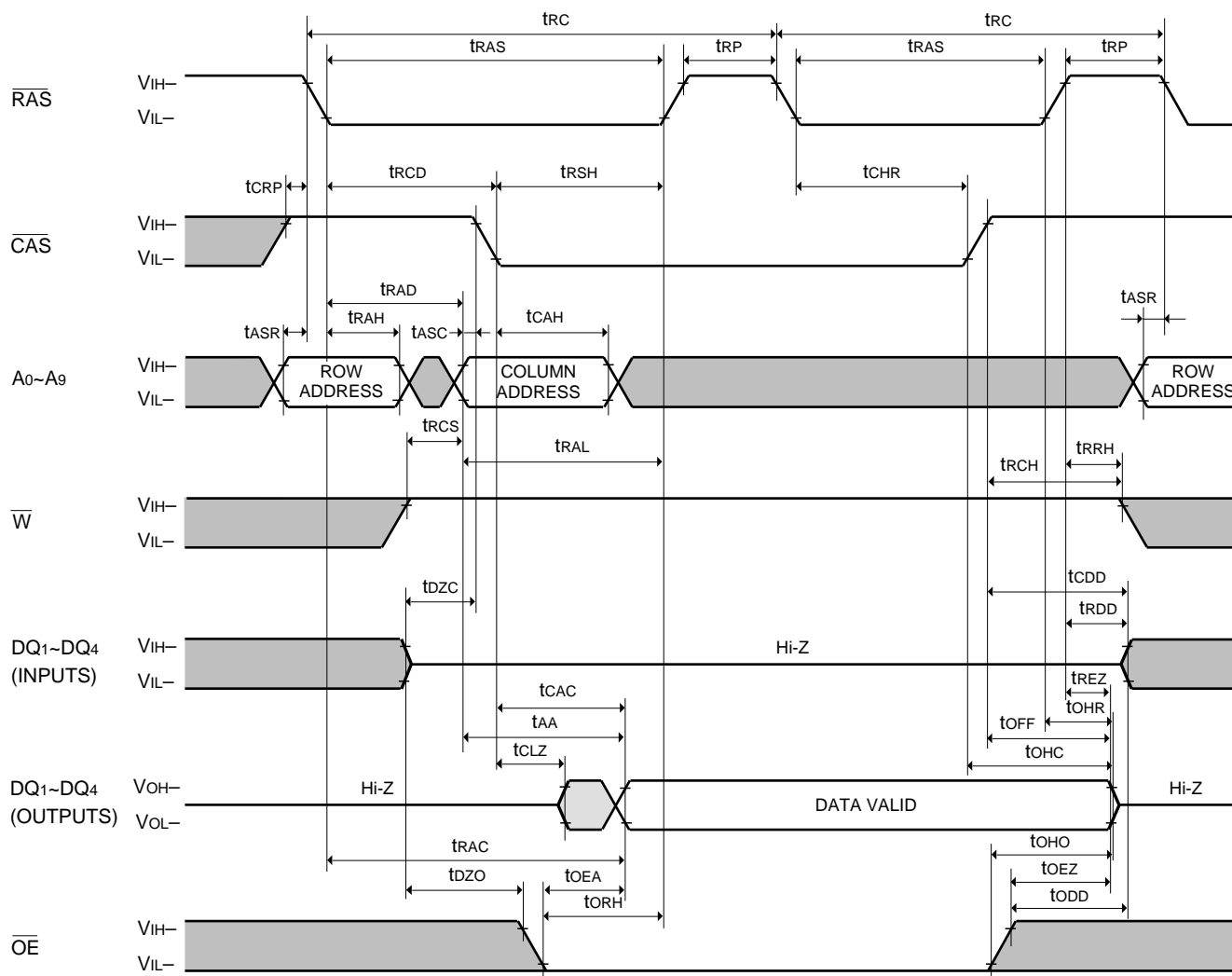
CAS before RAS Refresh Cycle, Extended Refresh Cycle *



M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 33)

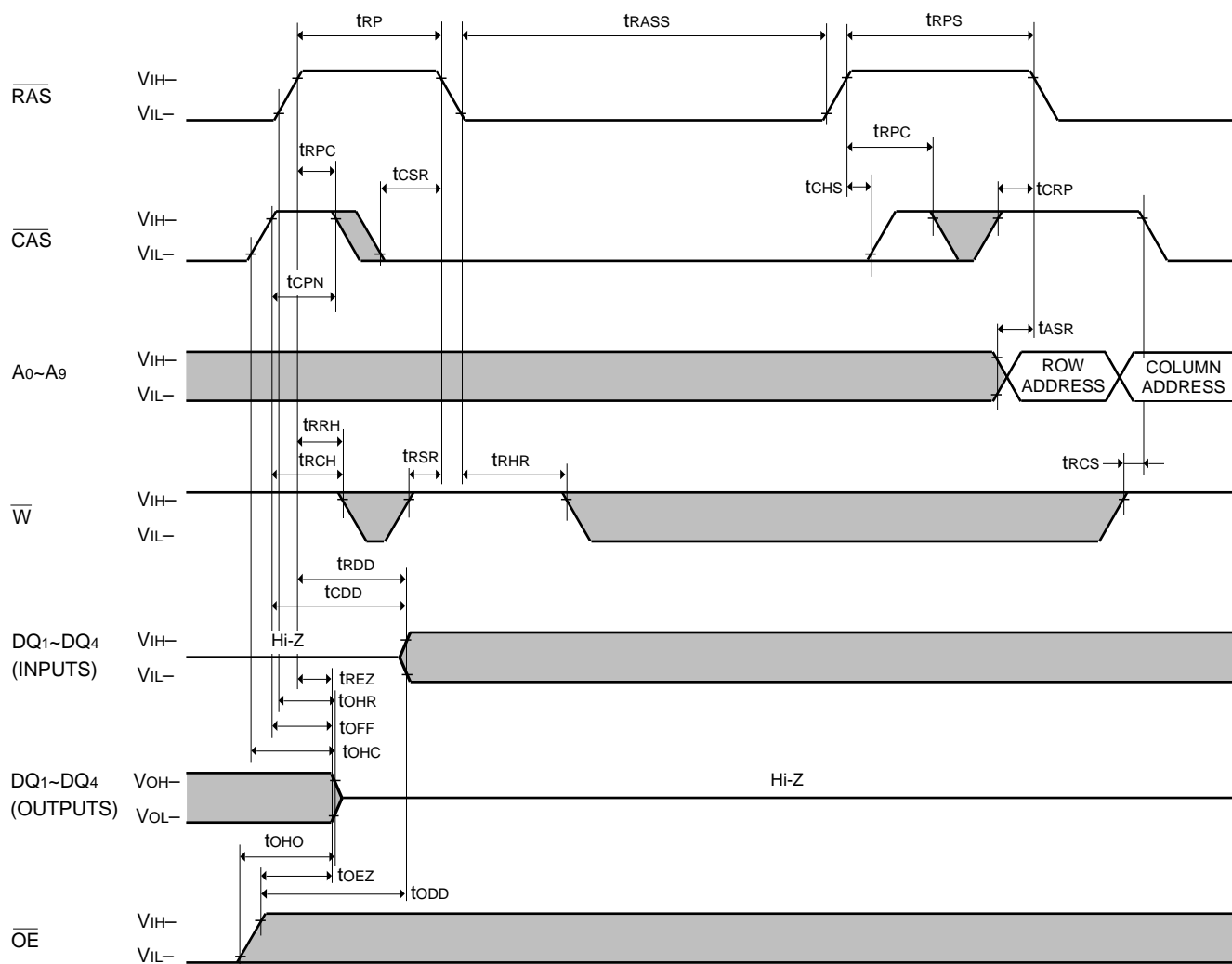


Note 33 : Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

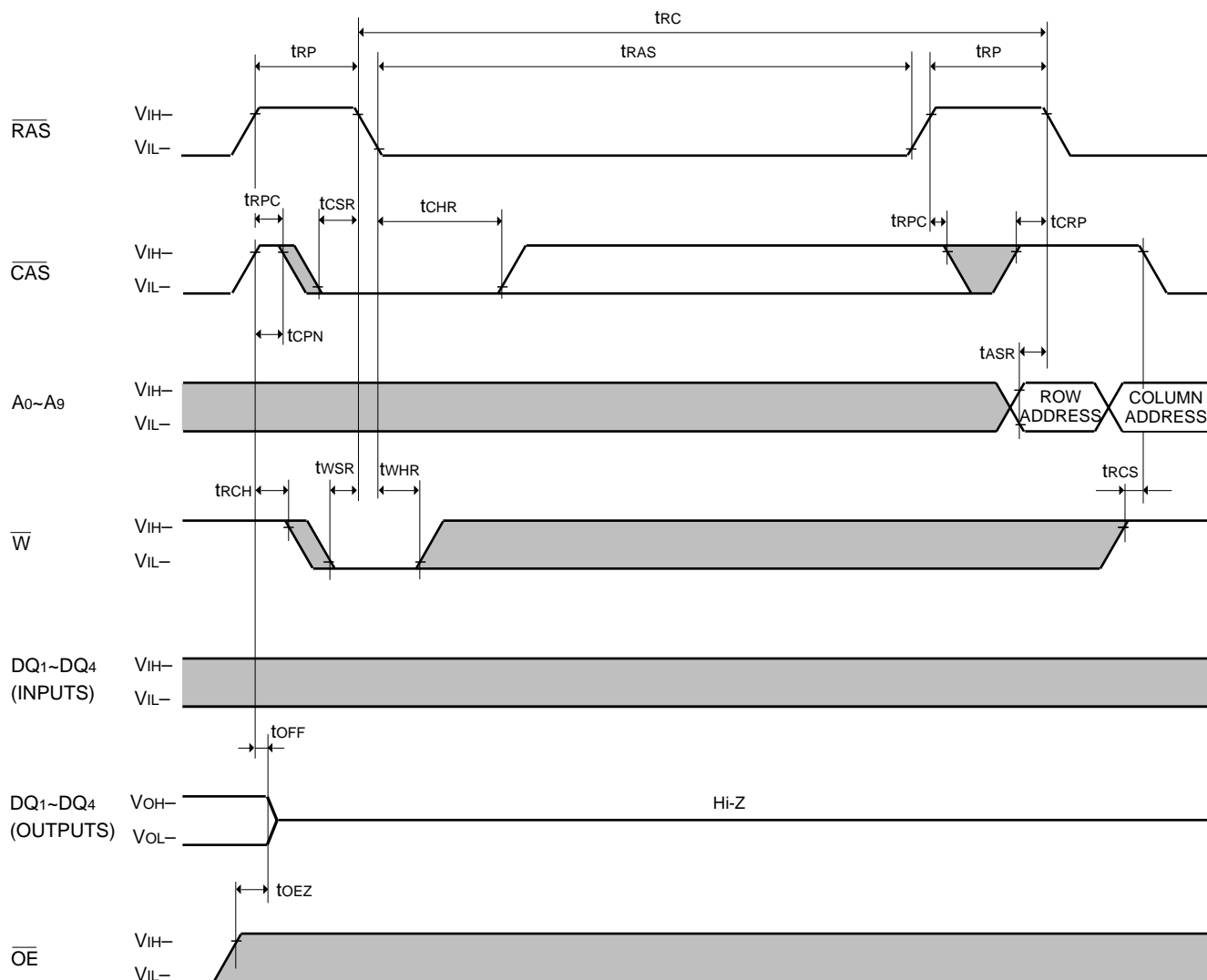
Self Refresh Cycle *(Note 30)



M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Test Mode Set Cycle (Note 34)



Note 34 : The cycle is also available for initialization cycle, but in this case device enters test mode.
 The test mode function is initiated with a \overline{W} and \overline{CAS} before \overline{RAS} cycle(WCBB cycle) as specified above timing diagram.
 The test mode function is terminated by either a \overline{CAS} before \overline{RAS} (CBB) refresh or a \overline{RAS} only refresh cycle.
 During the test mode, the device is internally organized as 4-bits wide (256-kilobytes deep) for each DQ (input/output) port.
 No addressing of A0,A1(column only) is required.
 During a write cycle, data on the each DQ (input) pin is written in parallel into all 4-bits for each DQ port and can be written independently for each DQ port.
 During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4-bits are equal, and a LOW state if any bits differ.
 During the test mode operation, a WCBB cycle is used to perform refresh.

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Note 30 : Self refresh sequence

Two refreshing methods should be used properly depending on the low pulse width(t_{RASS}) of RAS signal during self refresh period.

1. Distributed refresh during Read/Write operation

(A) Timing Diagram

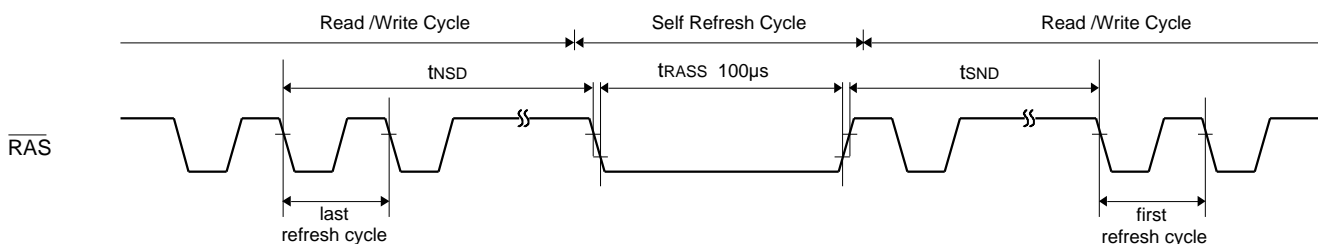
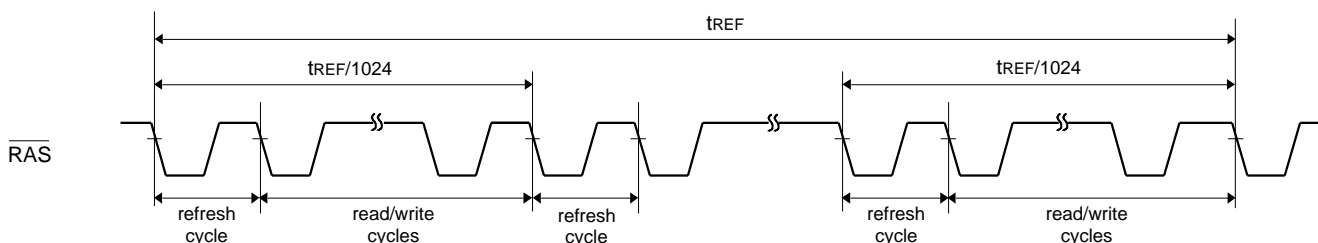


Table 2

Read/Write Cycle	Read/Write → Self Refresh	Self Refresh → Read/Write
CBR distributed refresh	t_{NSD} 125μs	t_{SND} 125μs
RAS only distributed refresh	t_{NSD} 16μs	t_{SND} 16μs

(B) Definition of distributed refresh



Definition of CBR distributed refresh

(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125μs max.) CBR cycles within 128ms.

Definition of RAS only distributed refresh

All combinations of nine row address signals ($A_0 \sim A_9$) are selected during 1024 constant period (16μs max.) RAS only refresh cycles within 16.4ms.

Note:

Hidden refresh may be used instead of CBR refresh.

RAS/CAS refresh may be used instead of RAS only refresh.

1.1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.

The time interval from the falling edge of \overline{RAS} signal in the last CBR refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).

- Switching from self refresh operation to read/write operation.

The time interval from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2)

1.2 RAS only distributed refresh

- Switching from read/write operation to self refresh operation.

The time interval t_{NSD} from the falling edge of \overline{RAS} signal in the last RAS only refresh cycle during read/write operation period to the falling edge of \overline{RAS} signal at the start of self refresh operation should be set within 16μs.

- Switching from self refresh operation to read/write operation.

The time interval t_{SND} from the rising edge of \overline{RAS} signal at the end of self refresh operation to the falling edge of \overline{RAS} signal in the first CBR refresh cycle during read/write operation period should be set within 16μs.

M5M44405CJ,TP-5,-6,-7,-5S,-6S,-7S

EDO (HYPER PAGE MODE) 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

2. Burst refresh during Read/Write operation (A) Timing diagram

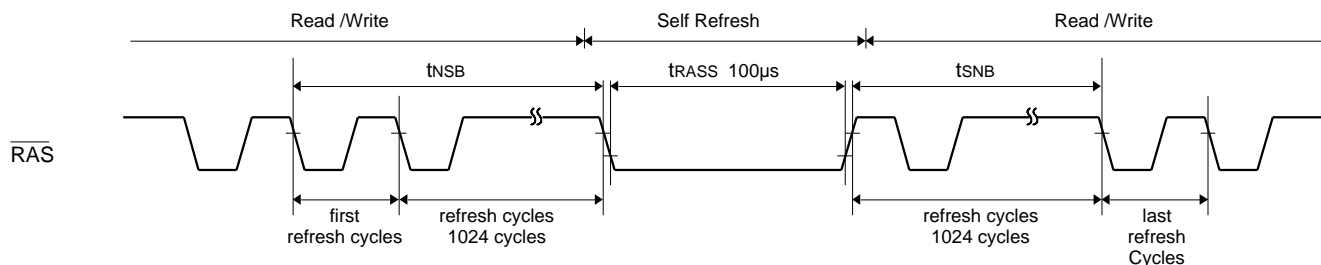
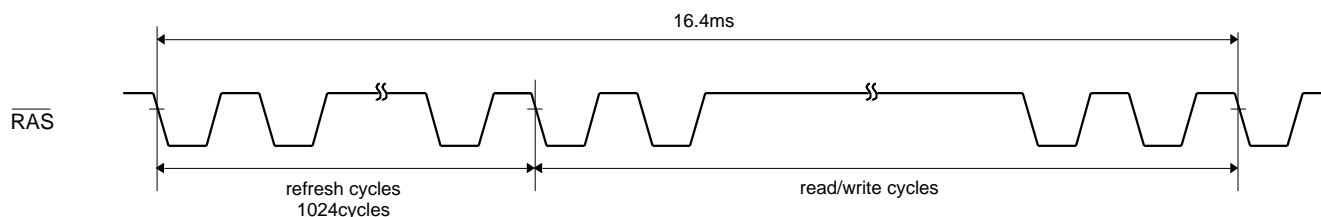


Table 3

Read/Write Cycle	Read/Write → Self Refresh	Self Refresh → Read/Write
CBR burst refresh	tNSB 16.4ms	tSNB 16.4ms
$\overline{\text{RAS}}$ only burst refresh	tNSB+tSNB 16.4ms	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{\text{RAS}}$ only burst refresh

All combination of nine row address signals ($A_0 \sim A_9$) are selected during 1024 continuous $\overline{\text{RAS}}$ only refresh cycles within 16.4ms.

2.1 CBR burst refresh

- Switching from read/write operation to self refresh operation.
The time interval t_{NSB} from the falling edge of $\overline{\text{RAS}}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within 16.4ms.
- Switching from self refresh operation to read/write operation.
The time interval t_{SNB} from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.2 $\overline{\text{RAS}}$ only burst refresh

- Switching from read/write operation to self refresh operation.
The time interval from the falling edge of $\overline{\text{RAS}}$ signal in the first $\overline{\text{RAS}}$ only refresh cycle during read/write operation period to the falling edge of $\overline{\text{RAS}}$ signal at the start of self refresh operation should be set within t_{NSB} (Shown in table 3).
- Switching from self refresh operation to read/write operation.
The time interval from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the last $\overline{\text{RAS}}$ only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).