

M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 4194304-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

| Type Name | RAS access time (max.ns) | CAS access time (max.ns) | Address access time (max.ns) | OE access time (max.ns) | Cycle time (min.ns) | Power dissipa- tion (typ.mW) |
|--------------------|-----------------------------------|-----------------------------------|---------------------------------------|----------------------------------|---------------------------|---------------------------------------|
| M5M417400CXX-5,-5S | 50 | 13 | 25 | 13 | 90 | 655 |
| M5M417400CXX-6,-6S | 60 | 15 | 30 | 15 | 110 | 540 |
| M5M417400CXX-7,-7S | 70 | 20 | 35 | 20 | 130 | 475 |

XX=J, TP

- Standard 26 pin SOJ, 26 pin TSOP
 - Single 5V \pm 10% supply
 - Low stand-by power dissipation
 - 5.5mW(Max)CMOS Input level
 - 2.2mW (Max)*CMOS Input level
 - Low operating power dissipation
 - M5M417400Cxx-5,-5S 800.0mW (Max)
 - M5M417400Cxx-6,-6S 660.0mW (Max)
 - M5M417400Cxx-7,-7S 580.0mW (Max)
 - Self refresh capability *
 - self refresh current 200.0 μ A(Max)
 - Fast-page mode, Read-modify-write, $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh capabilities
 - Early-write mode and $\overline{\text{OE}}$ to control output buffer impedance
 - All inputs, output TTL compatible and low capacitance
 - 2048 refresh cycles every 32ms ($A_0 \sim A_{10}$)
- *Applicable to self refresh version (M5M417400CJ,TP-5S,-6S,-7S :option) only

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

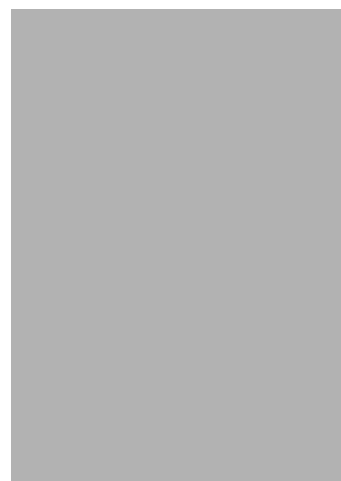
PIN DESCRIPTION

| Pin name | Function |
|-------------------------|-----------------------------|
| $A_0 \sim A_{11}$ | Address inputs |
| $DQ_1 \sim DQ_4$ | Data inputs / outputs |
| RAS | Row address strobe input |
| $\overline{\text{CAS}}$ | Column address strobe input |
| $\overline{\text{W}}$ | Write control input |
| $\overline{\text{OE}}$ | Output enable input |
| V_{CC} | Power supply (+5V) |
| V_{SS} | Ground (0V) |

PIN CONFIGURATION (TOP VIEW)



Outline 26P0D-B (300mil SOJ)



Outline 26P3D-E (300mil TSOP)

NC: NO CONNECTION

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FUNCTION

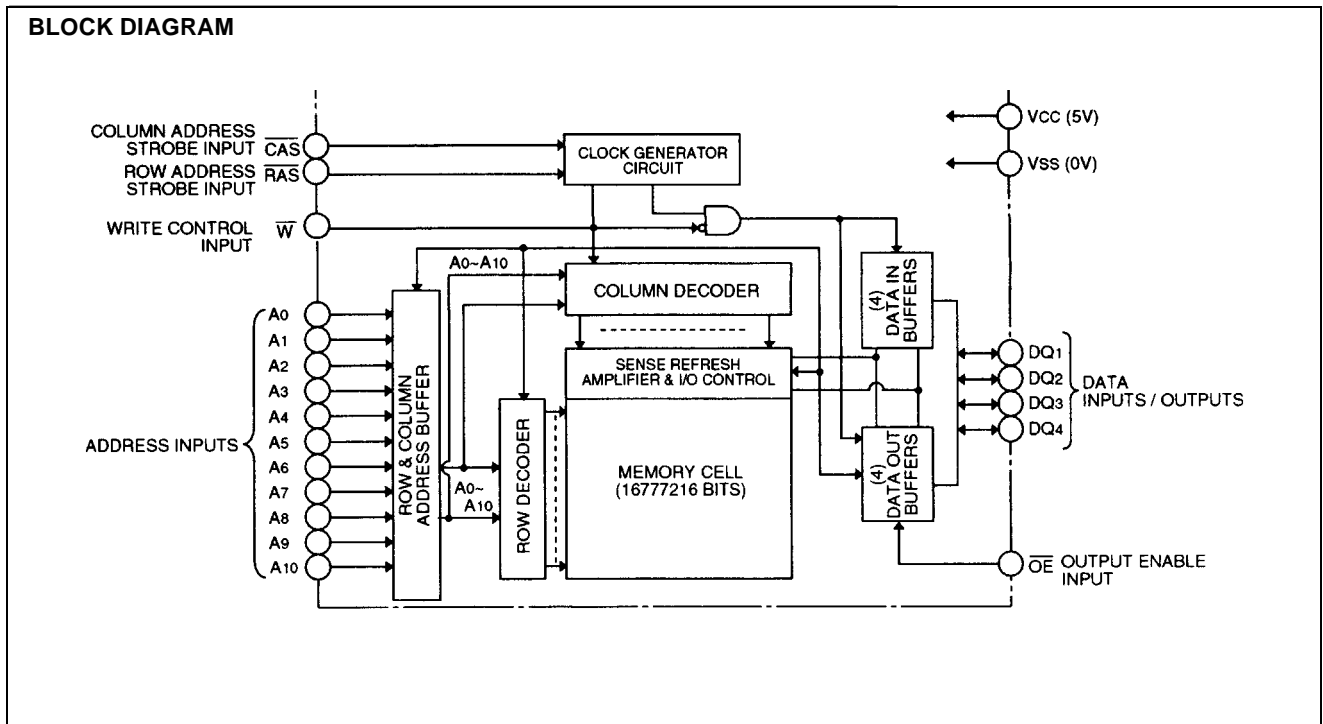
The M5M417400CJ,TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{\text{RAS}}$ -only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

| Operation | Inputs | | | | | | Input/Output | | Refresh | Remark |
|--|--------|-----|-----|-----|-------------|----------------|--------------|--------|---------|--------------------------|
| | RAS | CAS | W | OE | Row address | Column address | Input | Output | | |
| Read | ACT | ACT | NAC | ACT | APD | APD | OPN | VLD | YES | Fast page mode identical |
| Write (Early write) | ACT | ACT | ACT | DNC | APD | APD | VLD | OPN | YES | |
| Write (Delayed write) | ACT | ACT | ACT | DNC | APD | APD | VLD | IVD | YES | |
| Read-modify-write | ACT | ACT | ACT | ACT | APD | APD | VLD | VLD | YES | |
| $\overline{\text{RAS}}$ -only refresh | ACT | NAC | DNC | DNC | APD | DNC | DNC | OPN | YES | |
| Hidden refresh | ACT | ACT | NAC | ACT | APD | DNC | OPN | VLD | YES | |
| Self refresh | ACT | ACT | NAC | DNC | DNC | DNC | DNC | OPN | YES | |
| $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh | ACT | ACT | NAC | DNC | DNC | DNC | DNC | OPN | YES | |
| Stand-by | NAC | DNC | DNC | DNC | DNC | DNC | DNC | OPN | NO | |

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, IVD: invalid, APD: applied, OPN: open

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|-----------|-----------------------|----------------------------|-----------|--------------------|
| V_{CC} | Supply voltage | With respect to V_{SS} | -1 ~ 7 | V |
| V_I | Input voltage | | -1 ~ 7 | V |
| V_O | Output voltage | | -1 ~ 7 | V |
| I_O | Output current | | 50 | mA |
| P_d | Power dissipation | $T_a = 25^{\circ}\text{C}$ | 1000 | mW |
| T_{opr} | Operating temperature | | 0 ~ 70 | $^{\circ}\text{C}$ |
| T_{stg} | Storage temperature | | -65 ~ 150 | $^{\circ}\text{C}$ |

RECOMMENDED OPERATING CONDITIONS

$(T_a = 0 \sim 70^{\circ}\text{C}$, unless otherwise noted) (Note 1)

| Symbol | Parameter | Limits | | | Unit |
|----------|--------------------------------------|--------|-----|-----|------|
| | | Min | Nom | Max | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{SS} | Supply voltage | 0 | 0 | 0 | V |
| V_{IH} | High-level input voltage, all inputs | 2.4 | | 5.5 | V |
| V_{IL} | Low-level input voltage, all inputs | -1.0** | | 0.8 | V |

Note 1: All voltage values are with respect to V_{SS} .

**: $V_{IL(\min)}$ is -2.0V when undershoot width is less than 25ns. (Undershoot width is with respect to V_{SS} .)

ELECTRICAL CHARACTERISTICS

$(T_a = 0 \sim 70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---------------|---|------------------|---|--------|-----|----------|---------------|
| | | | | Min | Typ | Max | |
| V_{OH} | High-level output voltage | | $I_{OH} = -5.0\text{mA}$ | 2.4 | | V_{CC} | V |
| V_{OL} | Low-level output voltage | | $I_{OL} = 4.2\text{mA}$ | 0 | | 0.4 | V |
| I_{OZ} | Off-state output current | | Q floating $0\text{V} \leq V_{OUT} \leq 5.5\text{V}$ | -10 | | 10 | μA |
| I_I | Input current | | $0\text{V} \leq V_{IN} \leq 5.5\text{V}$, Other inputs pins = 0V | -10 | | 10 | μA |
| $I_{CC1(AV)}$ | Average supply current from V_{CC} , operating (Note 3,4) | M5M417400C-5,-5S | $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling | | | 145 | mA |
| | | M5M417400C-6,-6S | $t_{RC} = t_{WC} = \text{min.}$ | | | 120 | |
| | | M5M417400C-7,-7S | output open | | | 105 | |
| I_{CC2} | Supply current from V_{CC} , stand-by (Note 5) | | $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$, output open | | | 2 | mA |
| | | | $\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$ | | | 0.5 | |
| $I_{CC3(AV)}$ | Average supply current from V_{CC} , refreshing (Note 3) | M5M417400C-5,-5S | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ | | | 145 | mA |
| | | M5M417400C-6,-6S | $t_{RC} = \text{min.}$ | | | 120 | |
| | | M5M417400C-7,-7S | output open | | | 105 | |
| $I_{CC4(AV)}$ | Average supply current from V_{CC} , Fast-Page-Mode (Note 3,4) | M5M417400C-5,-5S | $\text{RAS} = V_{IL}$, CAS cycling | | | 80 | mA |
| | | M5M417400C-6,-6S | $t_{PC} = \text{min.}$ | | | 70 | |
| | | M5M417400C-7,-7S | output open | | | 60 | |
| $I_{CC6(AV)}$ | Average supply current from V_{CC} , $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh mode (Note 3) | M5M417400C-5,-5S | $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycling | | | 145 | mA |
| | | M5M417400C-6,-6S | $t_{RC} = \text{min.}$ | | | 120 | |
| | | M5M417400C-7,-7S | output open | | | 105 | |

Note 2: Current flowing into an IC is positive, out is negative.

3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

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CAPACITANCE

(Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|--|--------|-----|-----|------|
| | | | Min | Typ | Max | |
| C _{I(A)} | Input capacitance, address inputs | V _I = V _{SS} f = 1MHz V _I = 25mVrms | | | 5 | pF |
| C _{I(OE)} | Input capacitance, \overline{OE} input | | | | 7 | pF |
| C _{I(\overline{W})} | Input capacitance, write control input | | | | 7 | pF |
| C _{I(\overline{RAS})} | Input capacitance, \overline{RAS} input | | | | 7 | pF |
| C _{I(CAS)} | Input capacitance, CAS input | | | | 7 | pF |
| C _{I/O} | Input/Output capacitance, data ports | | | | 8 | pF |

SWITCHING CHARACTERISTICS

(Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, see notes 5, 12, 13)

| Symbol | Parameter | Limits | | | | | | Unit |
|------------------|--|------------------|-----|------------------|-----|------------------|-----|------|
| | | M5M417400C-5,-5S | | M5M417400C-6,-6S | | M5M417400C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{CAC} | Access time from \overline{CAS} (Note 6, 7) | | 13 | | 15 | | 20 | ns |
| t _{RAC} | Access time from \overline{RAS} (Note 6, 8) | | 50 | | 60 | | 70 | ns |
| t _{AA} | Column address access time (Note 6, 9) | | 25 | | 30 | | 35 | ns |
| t _{CPA} | Access time from \overline{CAS} precharge (Note 6, 10) | | 30 | | 35 | | 40 | ns |
| t _{OEa} | Access time from OE (Note 6) | | 13 | | 15 | | 20 | ns |
| t _{CLZ} | Output low impedance time from \overline{CAS} low (Note 6) | 5 | | 5 | | 5 | | ns |
| t _{OFF} | Output disable time after \overline{CAS} high (Note 11) | 0 | 13 | 0 | 15 | 0 | 15 | ns |
| t _{OEZ} | Output disable time after \overline{OE} high (Note 11) | 0 | 13 | 0 | 15 | 0 | 15 | ns |

Note 5: An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization \overline{RAS} cycles. The initialization cycles should be done either by \overline{RAS} -only refresh cycles or by \overline{CAS} before \overline{RAS} refresh cycles only.

Note the \overline{RAS} may be cycled during the initial pause. And any 8 \overline{RAS} or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of \overline{RAS} inactivity before proper device operation is achieved.

After the initialization cycles, \overline{RAS} should be kept either higher than V_{IH(min)} or lower than V_{IL(max)} except \overline{RAS} transition time.

6: Measured with a load circuit equivalent to 2 TTL loads and 100pF.

7: Assumes that t_{RCD} ≥ t_{RCD(max)} and t_{ASC} ≥ t_{ASC(max)}.

8: Assumes that t_{RCD} ≤ t_{RCD(max)} and t_{RAD} ≤ t_{RAD(max)}. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

9: Assumes that t_{RAD} ≥ t_{RAD(max)} and t_{ASC} ≤ t_{ASC(max)}.

10: Assumes that t_{CP} ≤ t_{CP(max)} and t_{ASC} ≥ t_{ASC(max)}.

11: t_{OFF(max)} and t_{OEZ(max)} defines the time at which the output achieves the high impedance state (I_{OUT} ≤ | ± 10 μ A |) and is not reference to V_{OH(min)} or V_{OL(max)}.

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TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted. See notes 12, 13)

| Symbol | Parameter | Limits | | | | | | Unit |
|------------------|--|------------------|-----|------------------|-----|------------------|-----|------|
| | | M5M417400C-5,-5S | | M5M417400C-6,-6S | | M5M417400C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{REF} | Refresh cycle time | | 32 | | 32 | | 32 | ms |
| t _{RP} | RAS high pulse width | 30 | | 40 | | 50 | | ns |
| t _{RCD} | Delay time, RAS low to CAS low (Note 14) | 18 | 37 | 20 | 45 | 20 | 50 | ns |
| t _{CRP} | Delay time, CAS high to RAS low | 10 | | 10 | | 10 | | ns |
| t _{RPC} | Delay time, RAS high to CAS low | 0 | | 0 | | 0 | | ns |
| t _{CPN} | CAS high pulse width | 10 | | 10 | | 10 | | ns |
| t _{RAD} | Column address delay time from RAS low (Note 15) | 13 | 25 | 15 | 30 | 15 | 35 | ns |
| t _{ASR} | Row address setup time before RAS low | 0 | | 0 | | 0 | | ns |
| t _{ASC} | Column address setup time before CAS low (Note 16) | 0 | 10 | 0 | 10 | 0 | 10 | ns |
| t _{RAH} | Row address hold time after RAS low | 8 | | 10 | | 10 | | ns |
| t _{CAH} | Column address hold time after CAS low | 13 | | 15 | | 15 | | ns |
| t _{DZC} | Delay time, data to CAS low (Note 17) | 0 | | 0 | | 0 | | ns |
| t _{DZO} | Delay time, data to OE low (Note 17) | 0 | | 0 | | 0 | | ns |
| t _{CDD} | Delay time, CAS high to data (Note 18) | 13 | | 15 | | 15 | | ns |
| t _{ODD} | Delay time, OE high to data (Note 18) | 13 | | 15 | | 15 | | ns |
| t _T | Transition time (Note 19) | 1 | 50 | 1 | 50 | 1 | 50 | ns |

Note 12: The timing requirements are assumed t_T = 5ns.

13: V_{IH(min)} and V_{IL(max)} are reference levels for measuring timing of input signals.

14: t_{RCD(max)} is specified as a reference point only. If t_{RCD} is less than t_{RCD(max)}, access time is t_{RAC}. If t_{RCD} is greater than t_{RCD(max)}, access time is controlled exclusively by t_{CAC} or t_{AA}. t_{RCD(min)} is specified as t_{RAD(min)} = t_{RAH(min)} + 2t_H + t_{ASC(min)}.

15: t_{RAD(max)} is specified as a reference point only. If t_{RAD} ≥ t_{RAD(max)} and t_{ASC} ≤ t_{ASC(max)}, access time is controlled exclusively by t_{AA}.

16: t_{ASC(max)} is specified as a reference point only. If t_{RCD} ≥ t_{RCD(max)} and t_{ASC} ≥ t_{ASC(max)}, access time is controlled exclusively by t_{CAC}.

17: Either t_{DZC} or t_{DZO} must be satisfied.

18: Either t_{CDD} or t_{ODD} must be satisfied.

19: t_T is measured between V_{IH(min)} and V_{IL(max)}.

Read and Refresh Cycles

| Symbol | Parameter | Limits | | | | | | Unit |
|------------------|--|------------------|-------|------------------|-------|------------------|-------|------|
| | | M5M417400C-5,-5S | | M5M417400C-6,-6S | | M5M417400C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{RC} | Read cycle time | 90 | | 110 | | 130 | | ns |
| t _{RAS} | RAS low pulse width | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| t _{CAS} | CAS low pulse width | 13 | 10000 | 15 | 10000 | 20 | 10000 | ns |
| t _{CSH} | CAS hold time after RAS low | 50 | | 60 | | 70 | | ns |
| t _{RSH} | RAS hold time after CAS low | 13 | | 15 | | 20 | | ns |
| t _{RCS} | Read setup time after CAS high | 0 | | 0 | | 0 | | ns |
| t _{RCH} | Read hold time after CAS low (Note 20) | 0 | | 0 | | 0 | | ns |
| t _{RRH} | Read hold time after RAS low (Note 20) | 10 | | 10 | | 10 | | ns |
| t _{RAL} | Column address to RAS hold time | 25 | | 30 | | 35 | | ns |
| t _{OCH} | CAS hold time after OE low | 13 | | 15 | | 20 | | ns |
| t _{ORH} | RAS hold time after OE low | 13 | | 15 | | 20 | | ns |

Note 20: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write)

| Symbol | Parameter | Limits | | | | | | Unit |
|------------------|---|------------------|-------|------------------|-------|------------------|-------|------|
| | | M5M417400C-5,-5S | | M5M417400C-6,-6S | | M5M417400C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{WC} | Write cycle time | 90 | | 110 | | 130 | | ns |
| t _{RAS} | RAS low pulse width | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| t _{CAS} | CAS low pulse width | 13 | 10000 | 15 | 10000 | 20 | 10000 | ns |
| t _{CSH} | CAS hold time after RAS low | 50 | | 60 | | 70 | | ns |
| t _{RSH} | RAS hold time after CAS low | 13 | | 15 | | 20 | | ns |
| t _{WCS} | Write setup time before CAS low (Note 22) | 0 | | 0 | | 0 | | ns |
| t _{WCH} | Write hold time after CAS low | 8 | | 10 | | 10 | | ns |
| t _{CWL} | CAS hold time after W low | 13 | | 15 | | 20 | | ns |
| t _{RWL} | RAS hold time after W low | 13 | | 15 | | 20 | | ns |
| t _{WP} | Write pulse width | 8 | | 10 | | 10 | | ns |
| t _{DS} | Data setup time before CAS low or W low | 0 | | 0 | | 0 | | ns |
| t _{DH} | Data hold time after CAS low or W low | 8 | | 10 | | 15 | | ns |
| t _{OEh} | OE hold time after W low | 13 | | 15 | | 20 | | ns |

Read-Write and Read-Modify-Write Cycles

| Symbol | Parameter | Limits | | | | | | Unit |
|-----------------------------|--|------------------|-------|------------------|-------|------------------|-------|------|
| | | M5M417400C-5,-5S | | M5M417400C-6,-6S | | M5M417400C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{RWC} | Read write/read modify write cycle time (Note 21) | 131 | | 155 | | 180 | | ns |
| t _{RAS} | \overline{RAS} low pulse width | 91 | 10000 | 105 | 10000 | 120 | 10000 | ns |
| t _{CAS} | \overline{CAS} low pulse width | 54 | 10000 | 60 | 10000 | 70 | 10000 | ns |
| t _{CSH} | CAS hold time after RAS low | 91 | | 105 | | 120 | | ns |
| t _{RSH} | \overline{RAS} hold time after \overline{CAS} low | 54 | | 60 | | 70 | | ns |
| t _{RCS} | Read setup time before \overline{CAS} low | 0 | | 0 | | 0 | | ns |
| t _{CWD} | Delay time, \overline{CAS} low to \overline{W} low (Note 22) | 36 | | 40 | | 45 | | ns |
| t _{RWD} | Delay time, \overline{RAS} low to \overline{W} low (Note 22) | 73 | | 85 | | 95 | | ns |
| t _{AWD} | Delay time, address to W low (Note 22) | 48 | | 55 | | 60 | | ns |
| t _{CWL} | \overline{CAS} hold time after \overline{W} low | 13 | | 15 | | 20 | | ns |
| t _{RWL} | RAS hold time after W low | 13 | | 15 | | 20 | | ns |
| t _{WP} | Write pulse width | 8 | | 10 | | 10 | | ns |
| t _{DS} | Data setup time before \overline{W} low | 0 | | 0 | | 0 | | ns |
| t _{DH} | Data hold time after \overline{W} low | 8 | | 10 | | 15 | | ns |
| t _{OE_H} | \overline{OE} hold time after \overline{W} low | 13 | | 15 | | 15 | | ns |

Note 21: t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{ODD(min)} + t_{RWL(min)} + t_{RP(min)} + 5t_r$.

Note 22: t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until \overline{CAS} or \overline{OE} goes back to V_{IH}) is indeterminate.

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Fast-Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle)

(Note 23)

| Symbol | Parameter | Limits | | | | | | Unit |
|-------------------|--|------------------|--------|------------------|--------|------------------|--------|------|
| | | M5M417400C-5,-5S | | M5M417400C-6,-6S | | M5M417400C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{PC} | Fast page mode read/write cycle time | 35 | | 40 | | 45 | | ns |
| t _{PRWC} | Fast page mode read write/read modify write cycle time | 76 | | 85 | | 95 | | ns |
| t _{RAS} | RAS low pulse width for read write cycle (Note 24) | 85 | 125000 | 100 | 125000 | 115 | 125000 | ns |
| t _{CP} | CAS high pulse width (Note 25) | 8 | 12 | 10 | 15 | 10 | 15 | ns |
| t _{CPRH} | RAS hold time after CAS precharge | 30 | | 35 | | 40 | | ns |
| t _{CPWD} | Delay time, CAS precharge to W low (Note 22) | 53 | | 60 | | 65 | | ns |

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: $t_{RAS(min)}$ is specified as two cycles of CAS input are performed.

25: $t_{CP(max)}$ is specified as a reference point only.

CAS before RAS Refresh Cycle

(Note 26)

| Symbol | Parameter | Limits | | | | | | Unit |
|------------------|--------------------------------|------------------|-----|------------------|-----|------------------|-----|------|
| | | M5M417400C-5,-5S | | M5M417400C-6,-6S | | M5M417400C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{CSR} | CAS setup time before RAS low | 10 | | 10 | | 10 | | ns |
| t _{CHR} | CAS hold time after RAS low | 10 | | 10 | | 15 | | ns |
| t _{RSR} | Read setup time before RAS low | 10 | | 10 | | 10 | | ns |
| t _{RHR} | Read hold time after RAS low | 10 | | 10 | | 15 | | ns |

Note 26: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -5S/-6S/-7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS

($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted) (Note 2)

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---------------|---|-----------------------|--|--------|-----|-----|---------|
| | | | | Min | Typ | Max | |
| $I_{CC8(AV)}$ | Average supply current from VCC Slow-Refresh cycle (Note 5) | M5M417400C (S) | CAS before RAS refresh cycling or RAS cycling & $\overline{CAS} \leq 0.2V$ $OE \ \& \ WE \leq 0.2V$ or $\overline{OE} \ \& \ \overline{WE} \geq V_{CC} - 0.2V$ $A_0 \sim A_{10} \leq 0.2V$ or $A_0 \sim A_{10} \geq V_{CC} - 0.2V$ $t_{REF} = 128ms$ (2048 cycles) output = OPEN $t_{RAS} = t_{RASmin.} \sim 1\mu s$ | | | 500 | μA |
| $I_{CC9(AV)}$ | Average supply current from VCC Slow-Refresh cycle (Note 5) | M5M417400C (S) | $\overline{RAS} = \overline{CAS} \leq 0.2V$ output = OPEN | | | 200 | μA |

M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

TIMING REQUIREMENTS

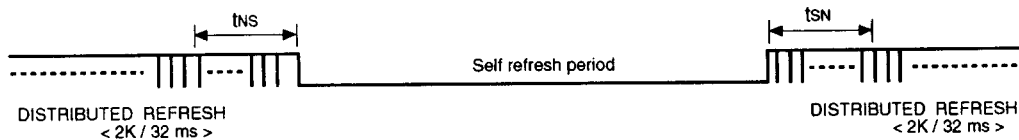
(Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, see notes 12, 13)

| Symbol | Parameter | Limits | | | | | | Unit |
|-------------------|--|---------------|-----|---------------|-----|---------------|-----|------|
| | | M5M417400C-5S | | M5M417400C-6S | | M5M417400C-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{RASS} | Self Refresh $\overline{\text{RAS}}$ low pulse width | 100 | | 100 | | 100 | | μs |
| t _{RPS} | Self Refresh RAS high precharge time | 90 | | 110 | | 130 | | ns |
| t _{CHS} | Self Refresh $\overline{\text{RAS}}$ hold time | -50 | | -50 | | -50 | | ns |
| t _{RSR} | Read setup time before $\overline{\text{RAS}}$ low | 10 | | 10 | | 10 | | ns |
| t _{RHR} | Read hold time after $\overline{\text{RAS}}$ low | 10 | | 10 | | 15 | | ns |

SELF REFRESH ENTRY & EXIT CONDITIONS

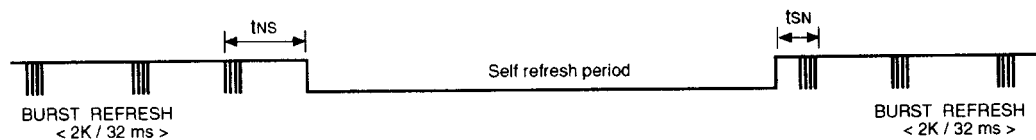
1. In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} ≤ 32ms and t_{SN} ≤ 32ms.



2. In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of t_{NS} + t_{SN} ≤ 32ms.



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

TEST Mode SET Cycle

| Symbol | Parameter | Limits | | | | | | Unit |
|------------------|---|------------------|-----|------------------|-----|------------------|-----|------|
| | | M5M417400C-5,-5S | | M5M417400C-6,-6S | | M5M417400C-7,-7S | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _{WSR} | W setup time before RAS low | 10 | | 10 | | 10 | | ns |
| t _{WHR} | \overline{W} hold time after \overline{RAS} low | 10 | | 10 | | 15 | | ns |

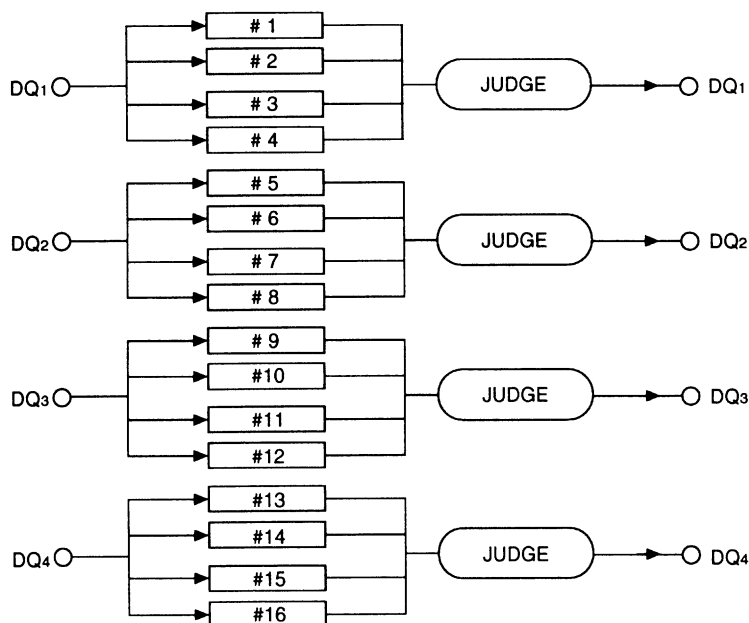
Note 27: The test mode function is initiated by a W and CAS before RAS cycle (WCBR cycle) as specified in timing diagram.

The test mode function is terminated by either a \overline{CAS} before \overline{RAS} refresh cycle (CBR refresh cycle) or a \overline{RAS} only refresh cycle.

During the test mode, the device is internally organized as 16-bits wide (1M bytes depth). No addressing of CA_0 and CA_1 is required.

During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ pin is written into 4-bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 4-bits, respectively. High state indicates that they are same. Low state indicates that they are not same.

During the test mode operation, only WCBR cycle can be used to perform refresh.

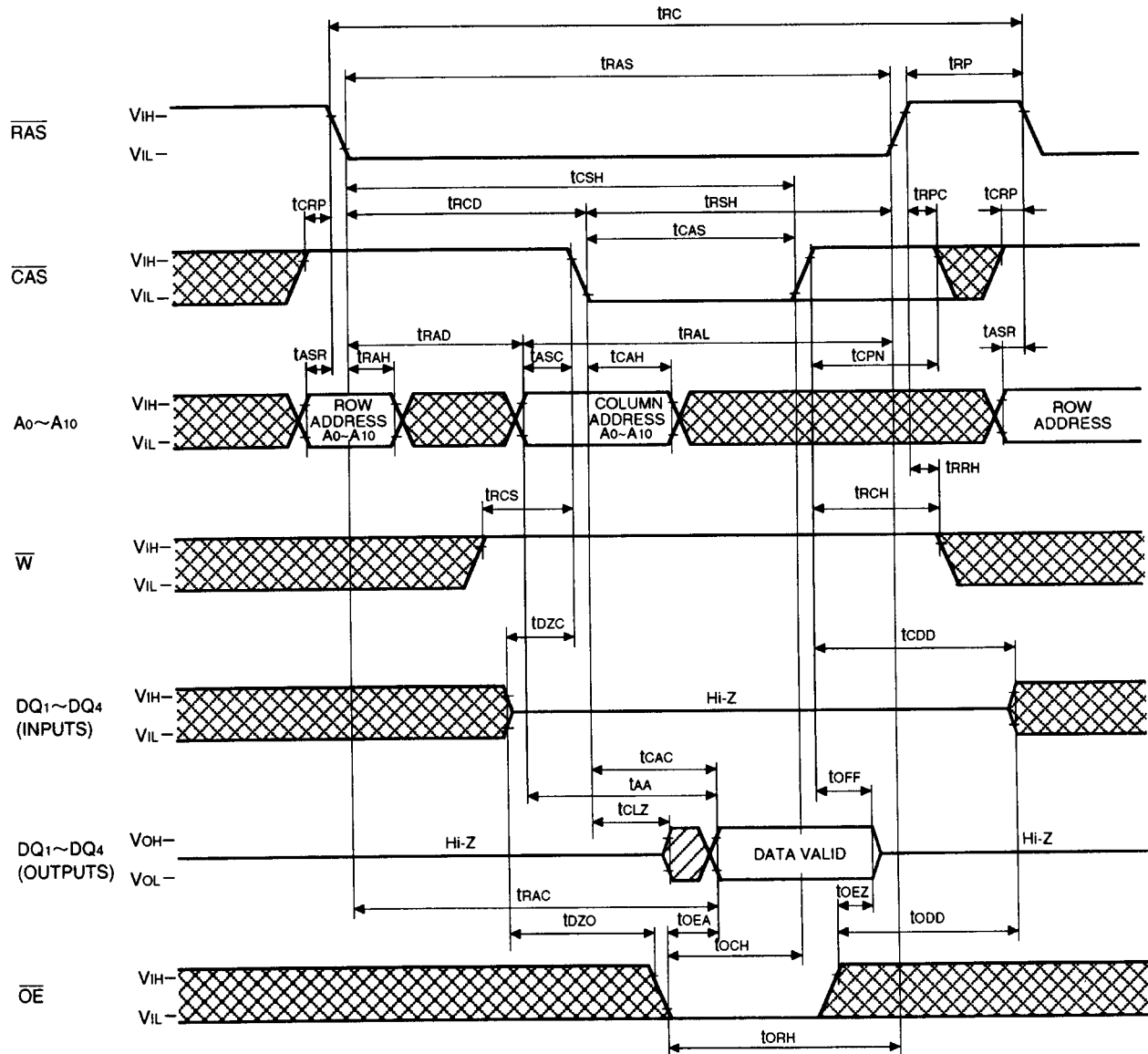


M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

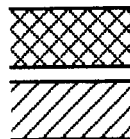
FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

Timing Diagrams Read Cycle

(Note 28)



Note 28



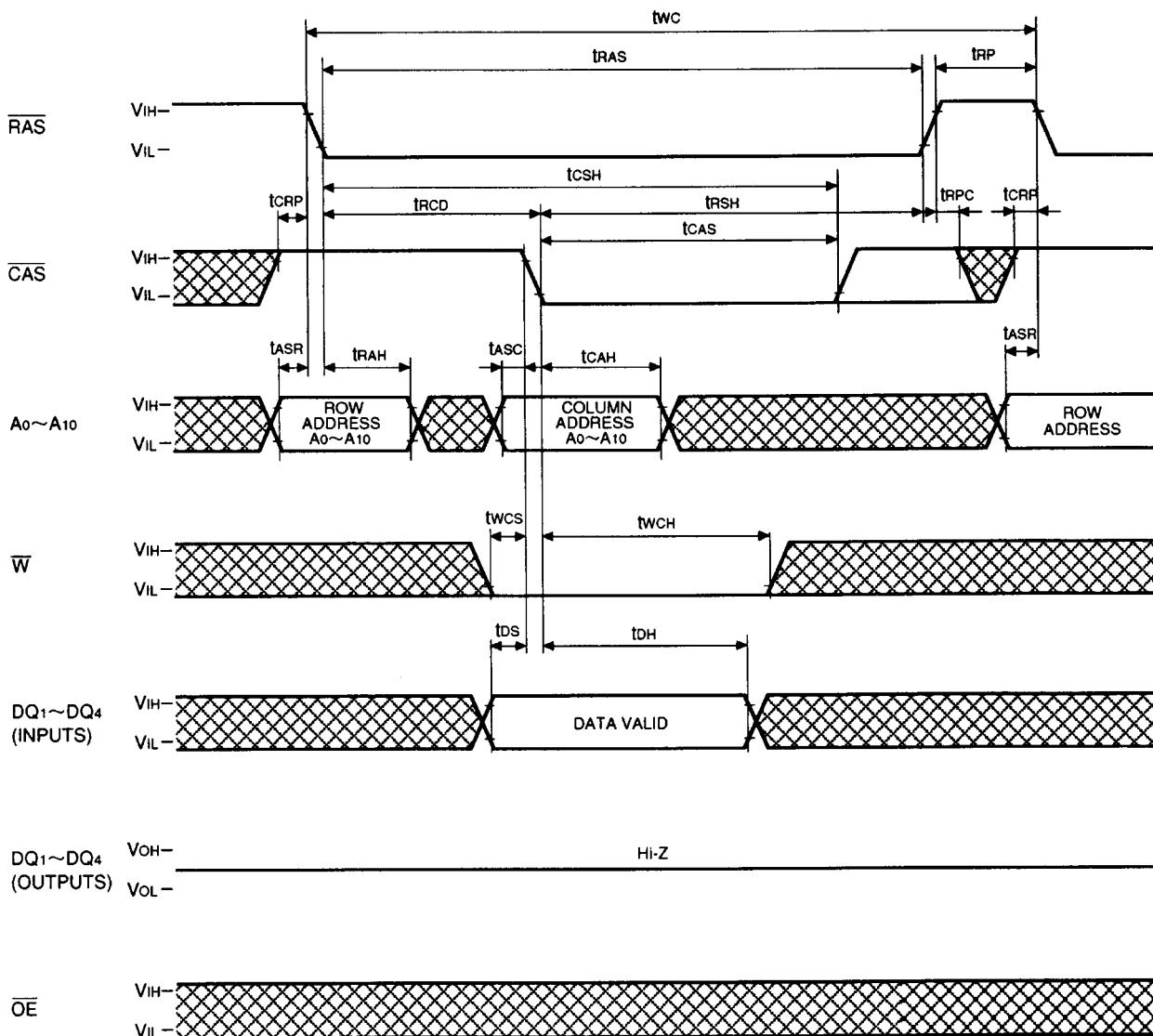
Indicates the don't care input.
 $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$ or $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$

Indicates the invalid output.

M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

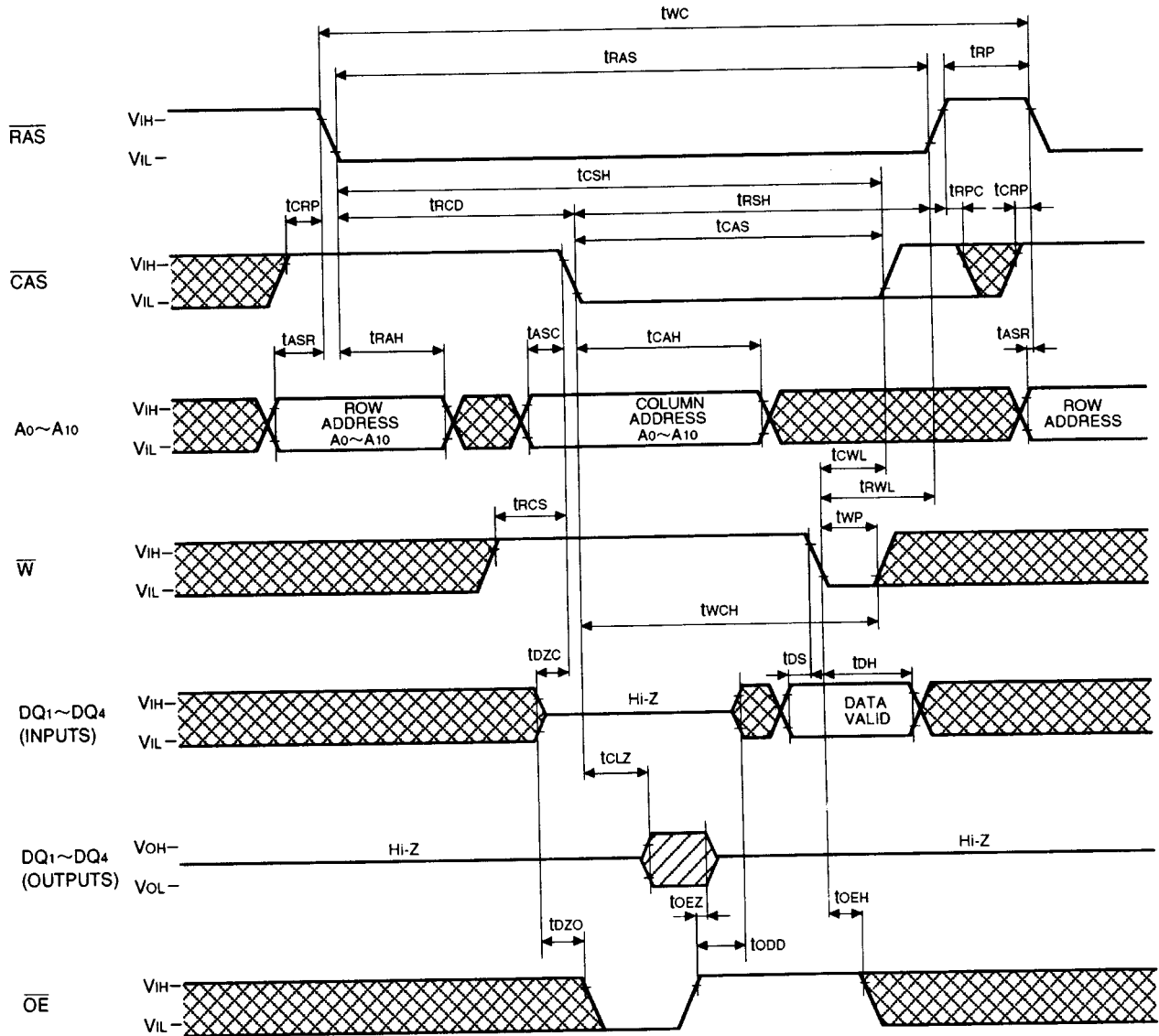
Write Cycle (Early Write)



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

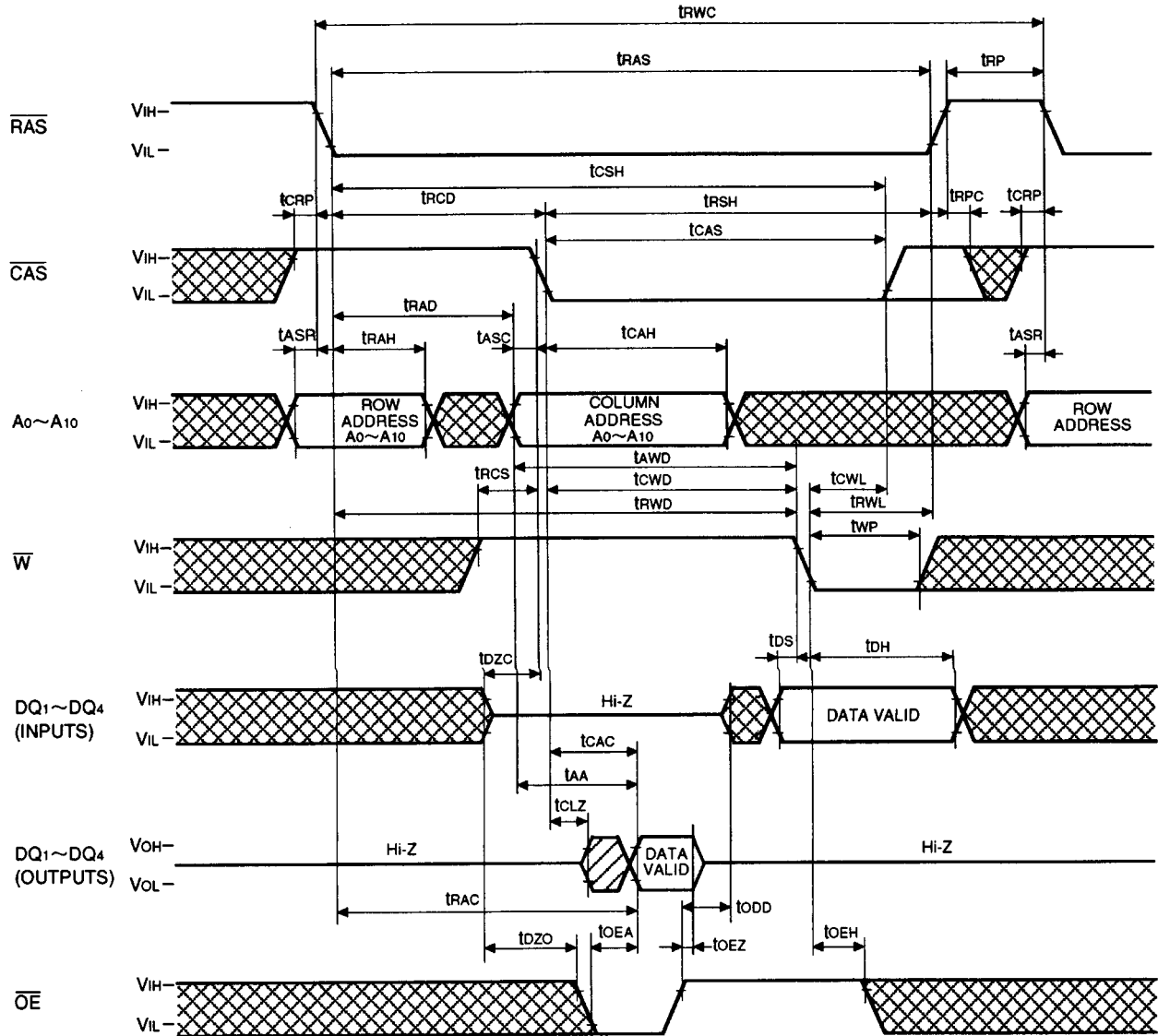
Write Cycle (Delayed Write)



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

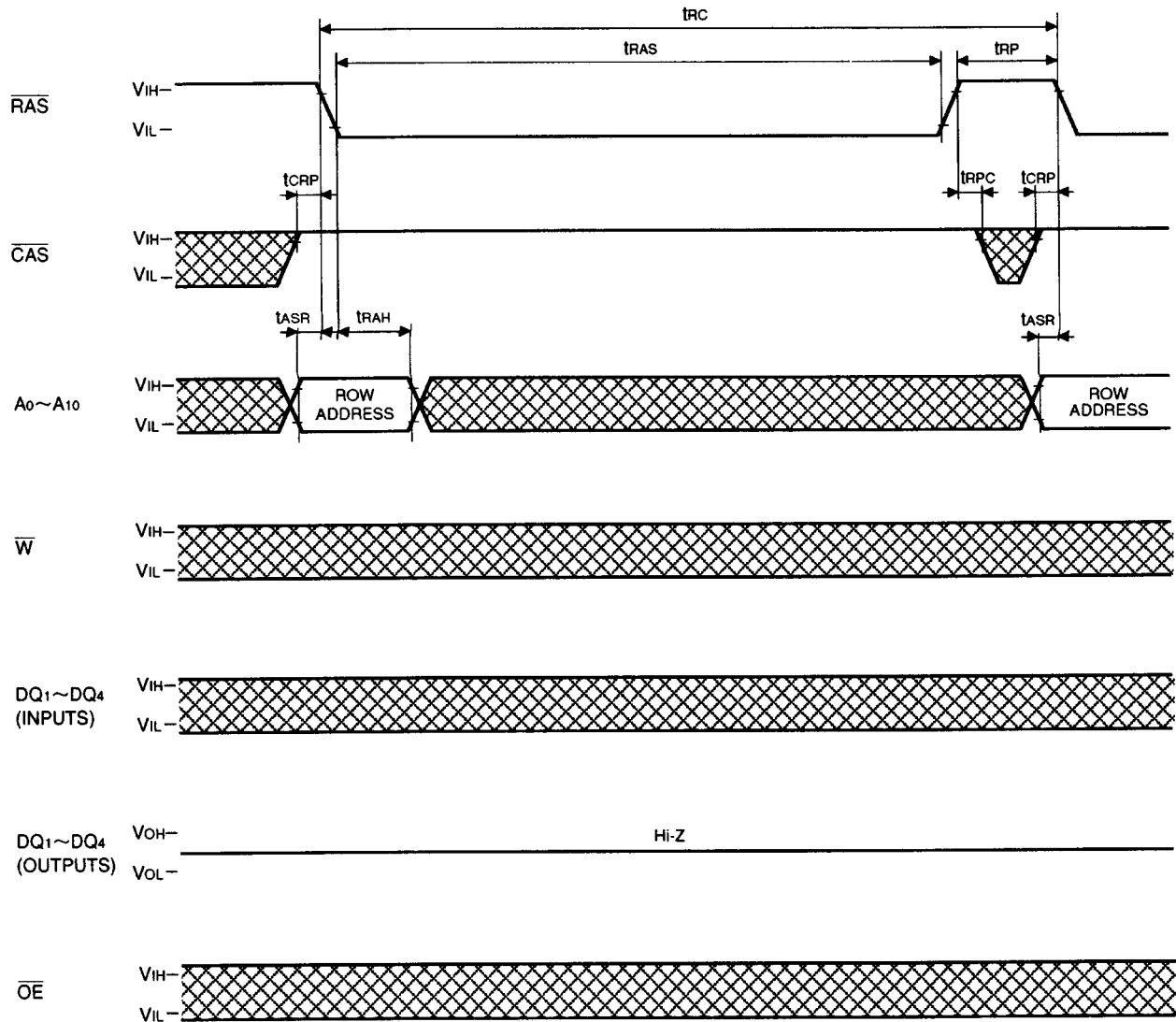
Read-Write, Read-Modify-Write Cycle



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

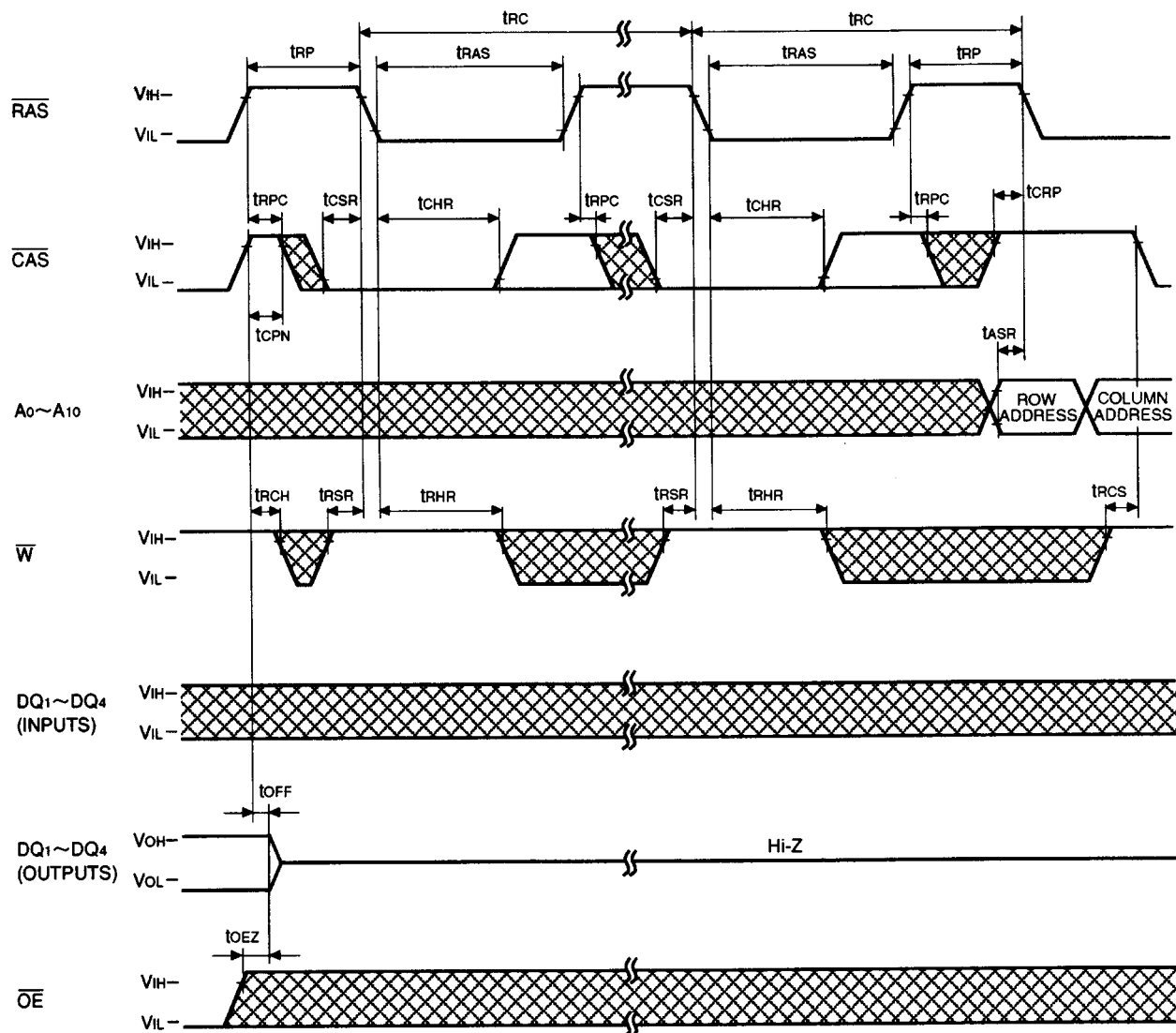
$\overline{\text{RAS}}$ -only Refresh Cycle



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle, Slow Refresh Cycle

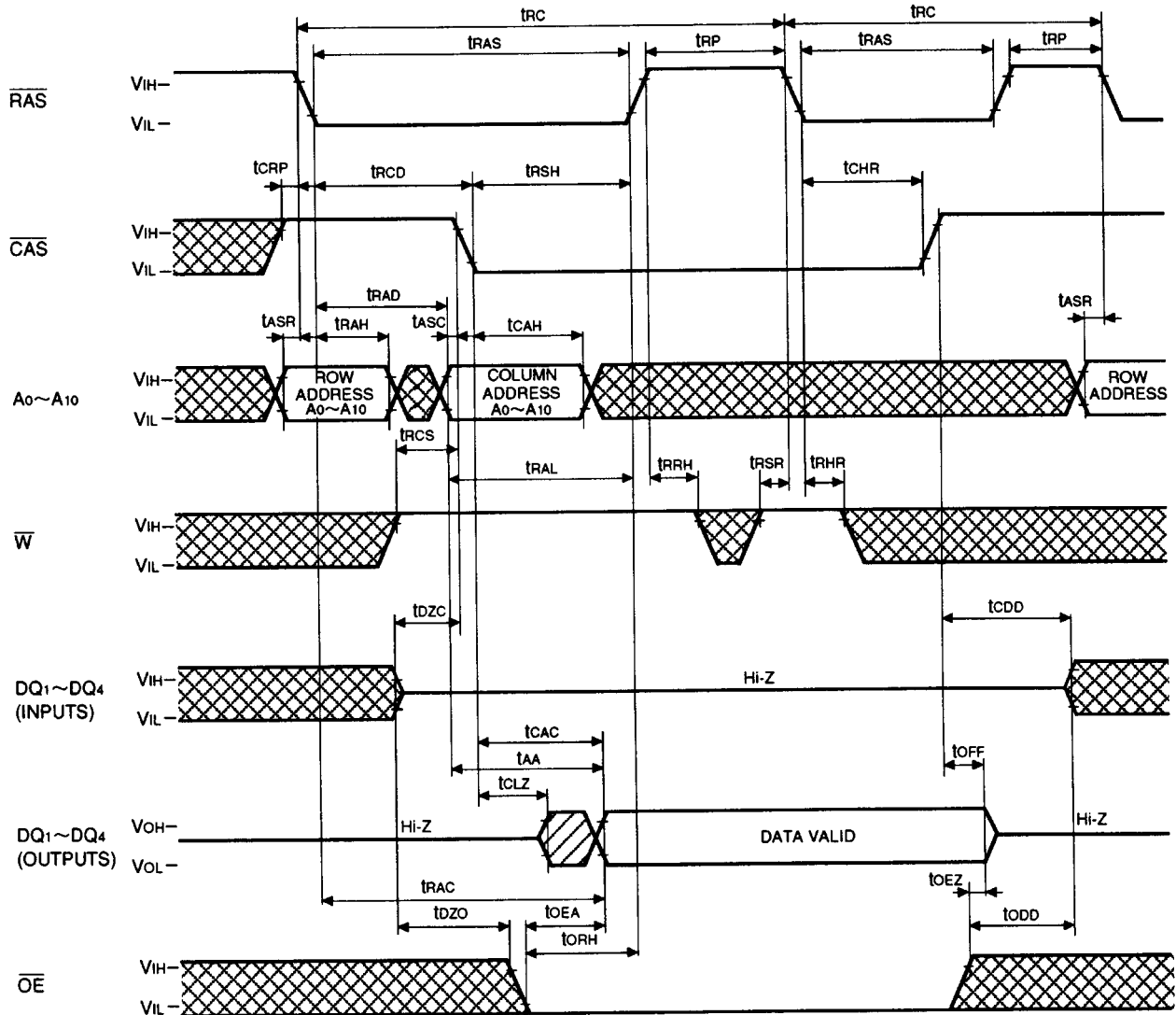


M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

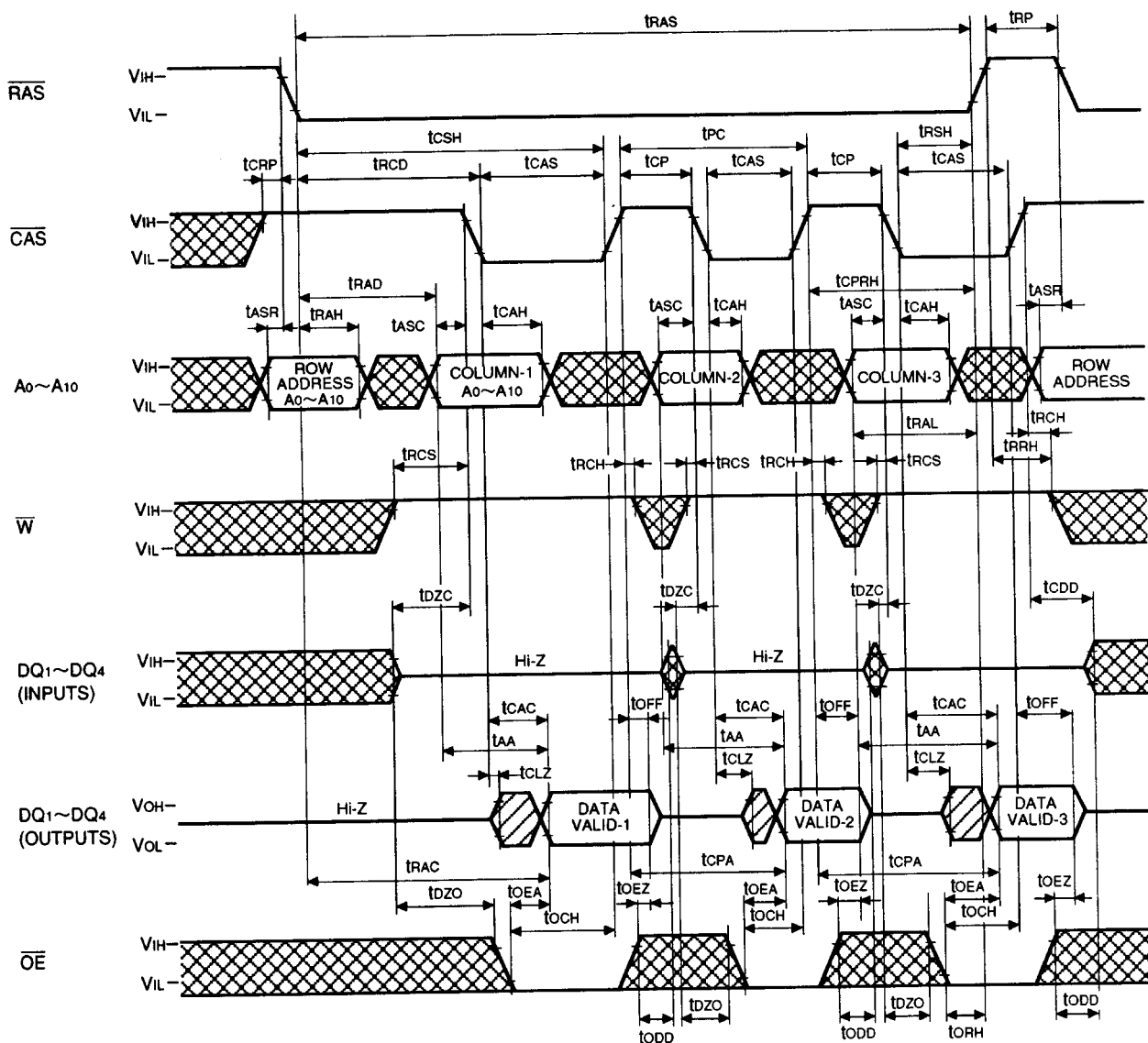
Hidden Refresh Cycle (Read)

(Note 29)



Note 29: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.
And in any cycle, t_{RSR} & t_{RHR} should be satisfied not to enter TEST MODE.

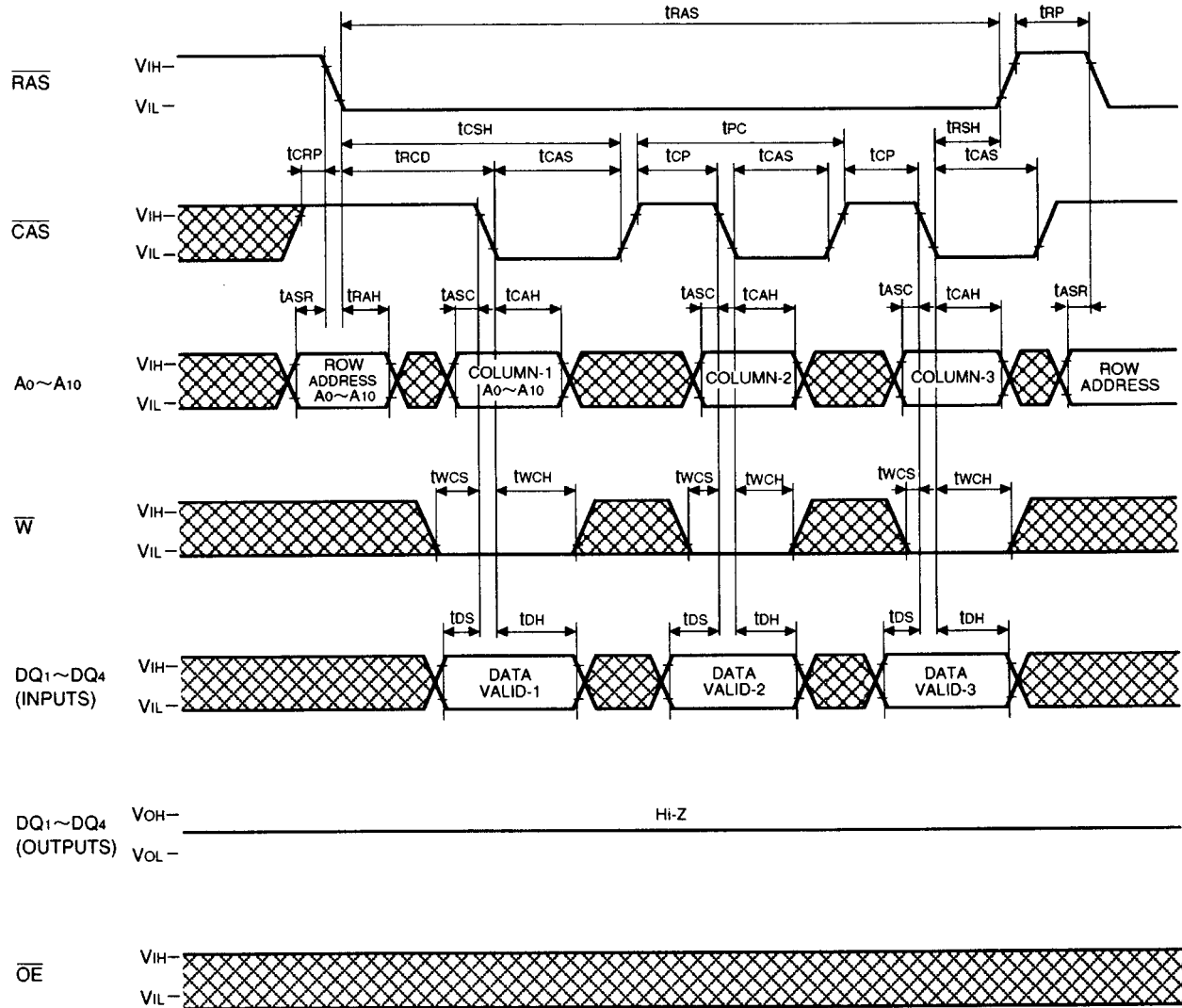
Fast Page Mode Read Cycle



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

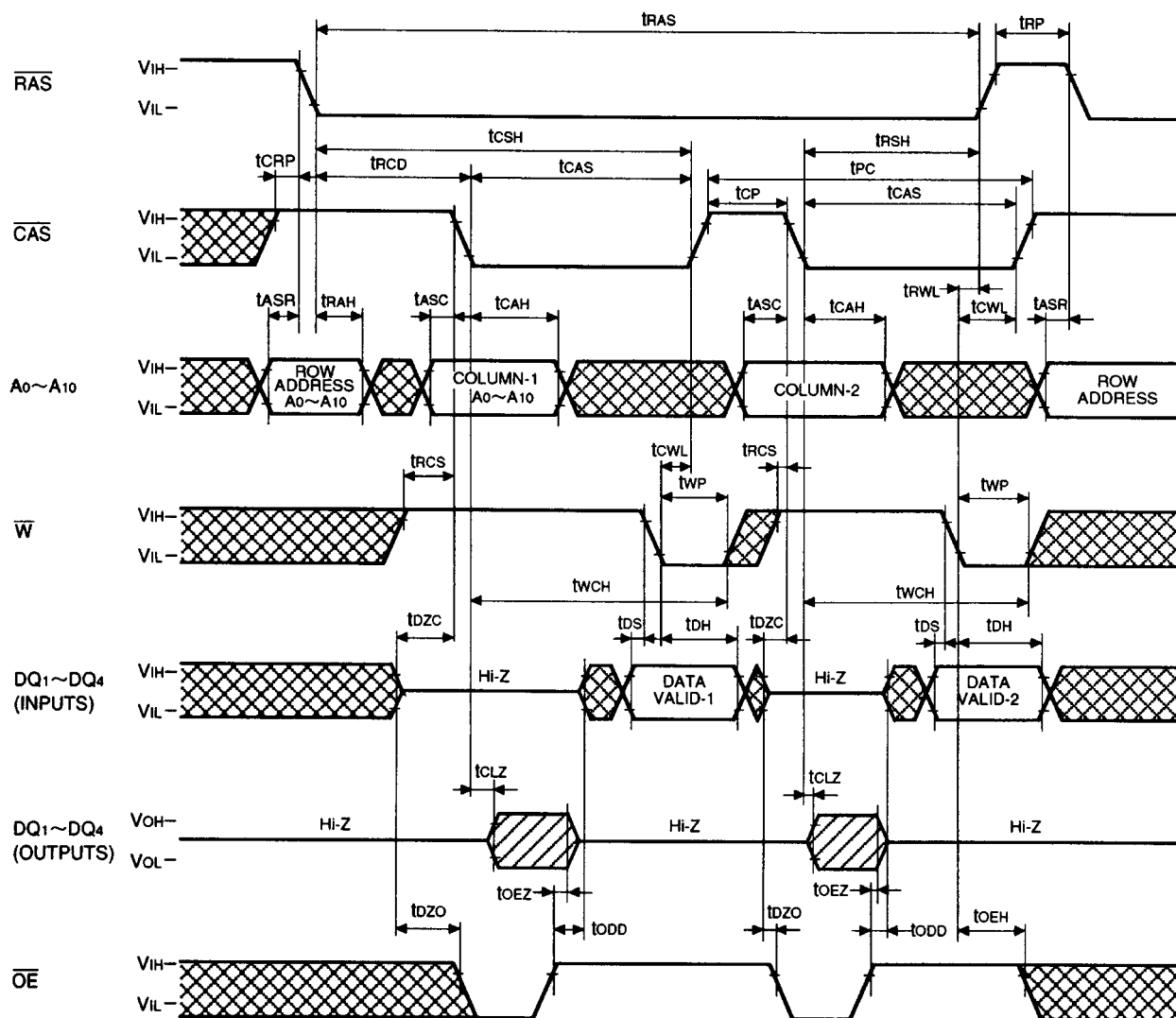
Fast Page Mode Write Cycle (Early Write)



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

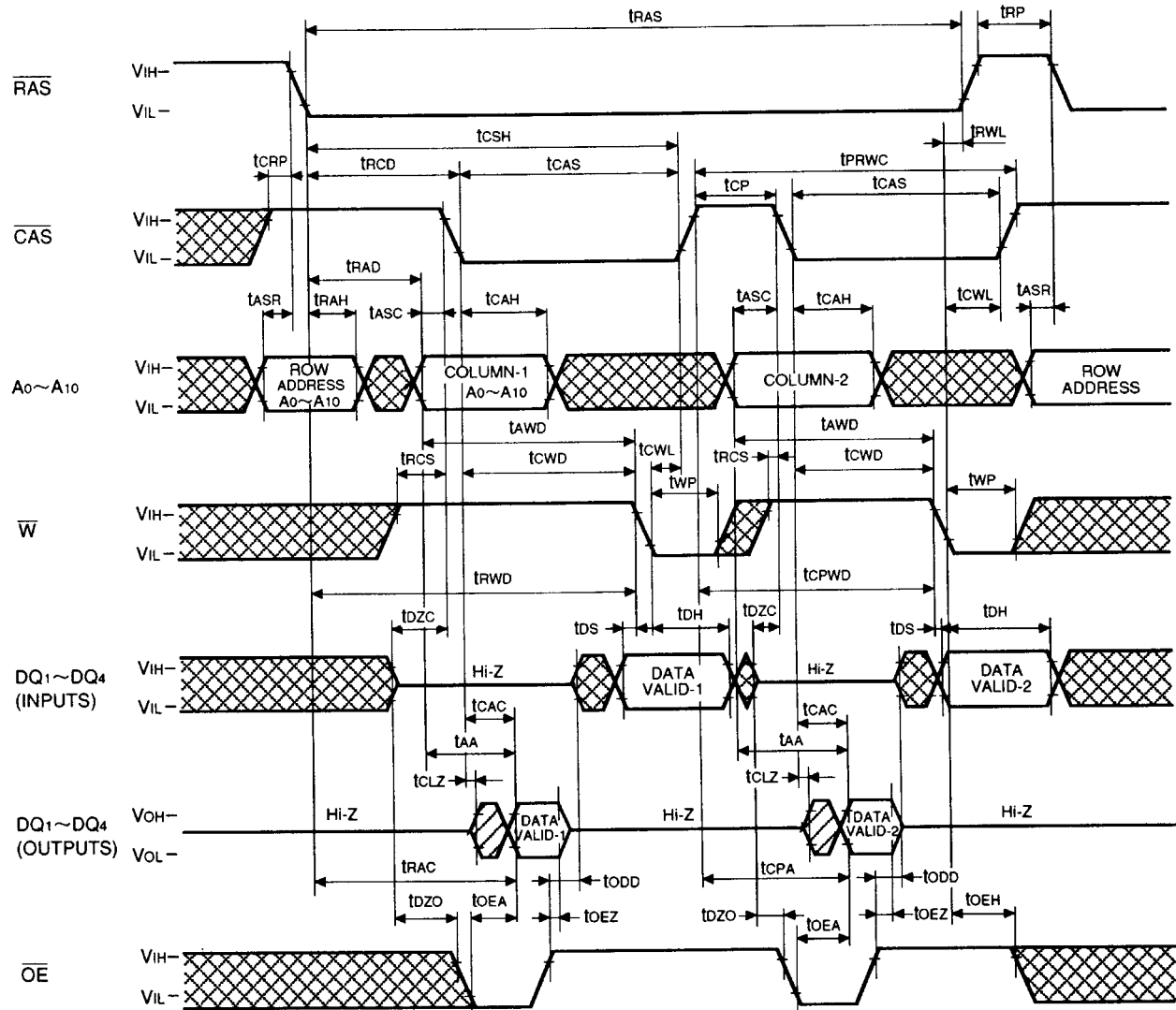
Fast-Page Mode Write Cycle (Delayed Write)



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

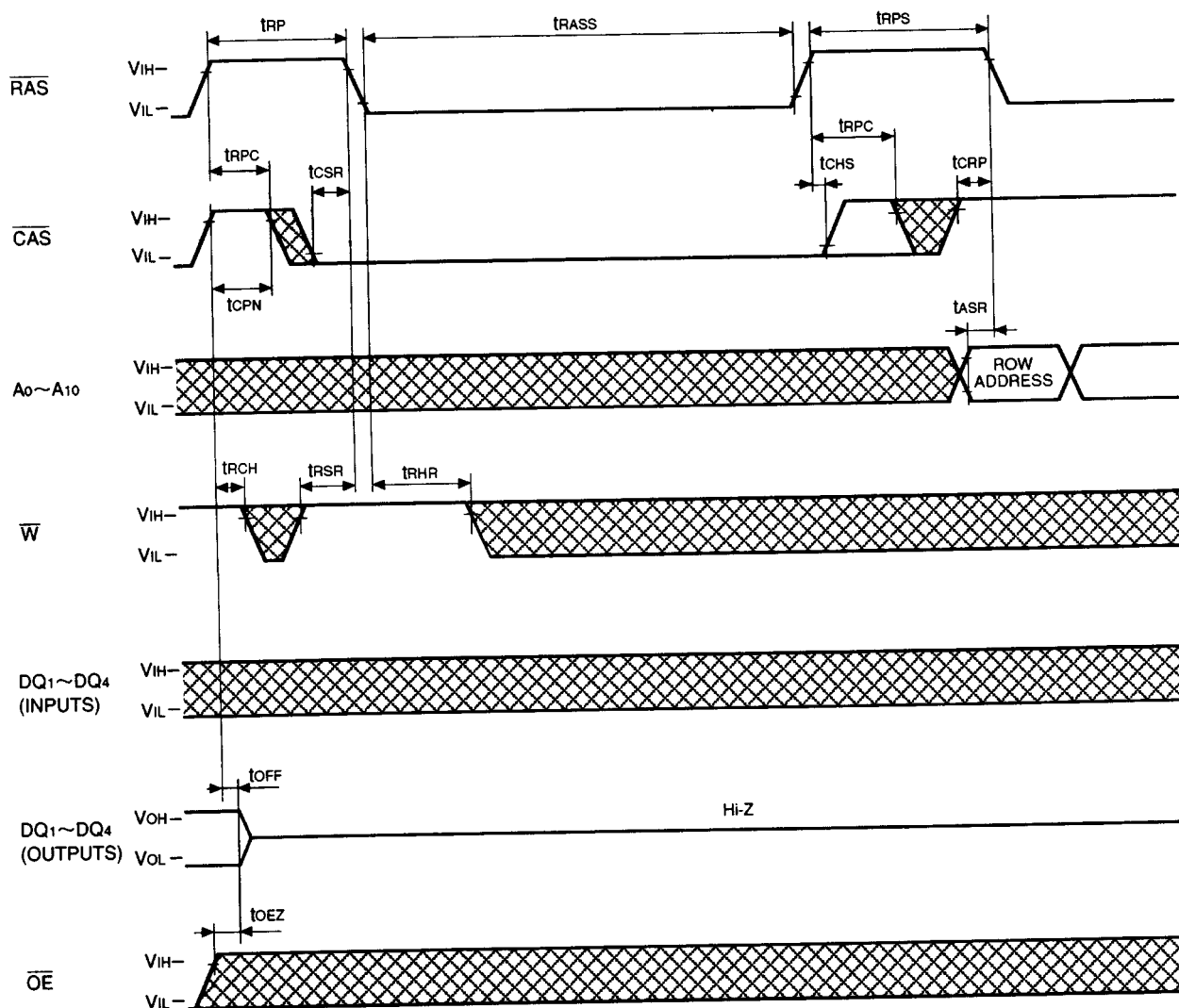
Fast Page Mode Read-Write, Read-Modify-Write Cycle



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 16777216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

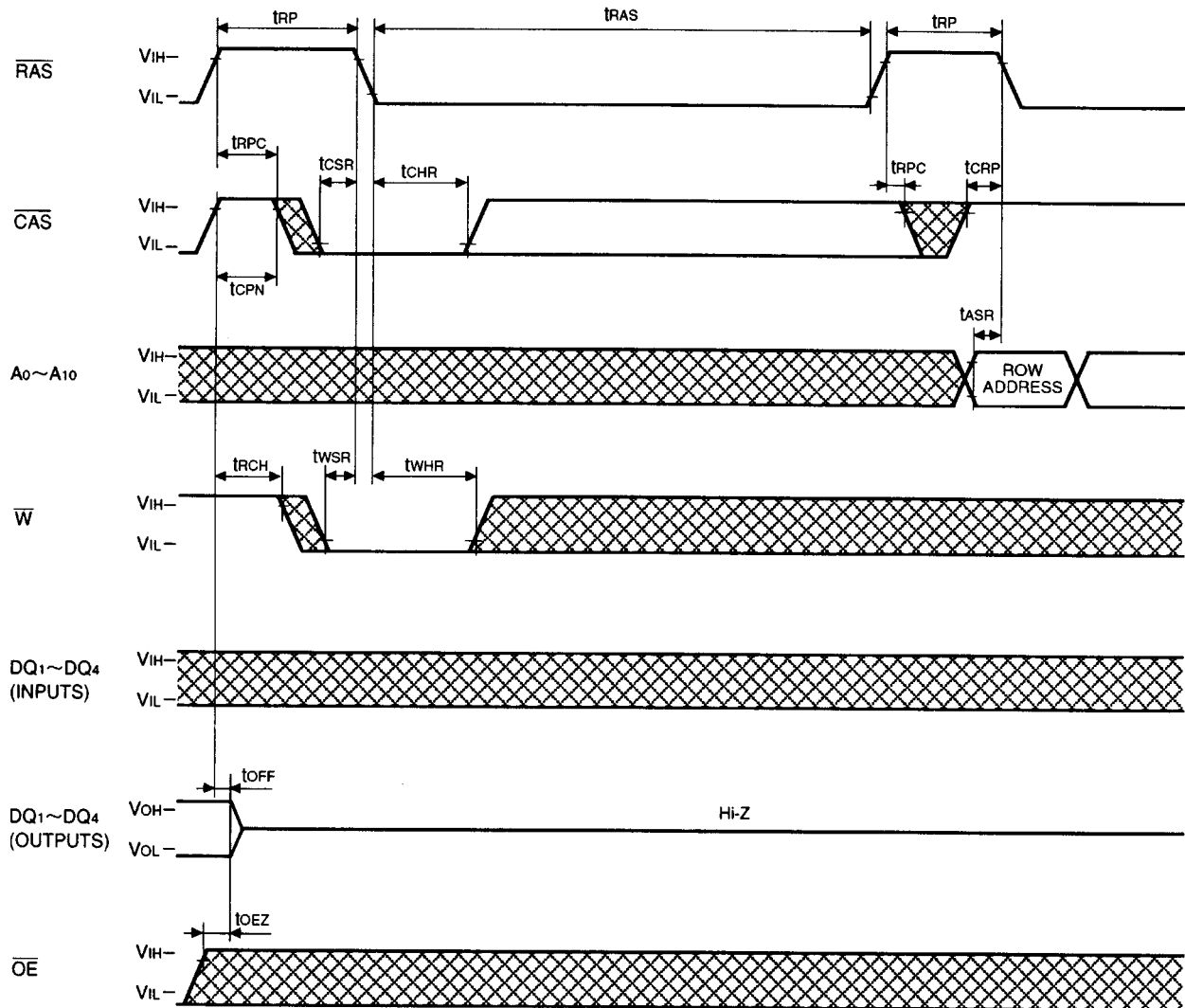
Self Refresh Cycle



M5M417400CJ,TP-5,-6,-7,-5S,-6S,-7S

FAST PAGE MODE 1677216-BIT (4194304-WORD BY 4-BIT) DYNAMIC RAM

TEST Mode SET Cycle



Note 30: This cycle can be used for initialized cycle after power-up, however entried into Test Mode.