M5M44400AWJ,J,L,TP,RT-6,-7,-8,-6L,-7L,-8L

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

The M5M44400ATP, RT are packaged in a 26-pin very thin and small outline package which is a high reliability and high density surface mount device. Two types of devices are available. M5M44400ATP (normal lead bend type package), M5M44400ART (reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

Stand-by current is small enough for battery back-up application (L version).

FEATURES

Type name	$\overline{RAS}$ access time (max ns)	$\overline{CAS}$ access time (max ns)	Address access time (max ns)	$\overline{OE}$ access time (max ns)	Cycle time (min ns)	Power dissipation (typ mW)
M5M44400AXX-6, -6L	60	15	30	15	120	400
M5M44400AXX-7, -7L	70	20	35	20	140	350
M5M44400AXX-8, -8L	80	20	40	20	160	300

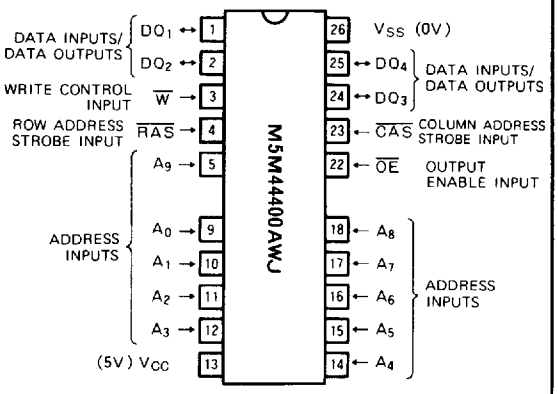
XX=WJ, J, L, TP, RT

- Standard 26 pin SOJ, 20 pin ZIP, 26 pin TSOP
- Single 5V ± 10% supply
- Low stand-by power dissipation
  - M5M44400AWJ, J, L, TP, RT ····· 5.5mW (max)
  - M5M44400AWJ, J, L (L) ····· 1.10mW (max)
  - M5M44400ATP, RT (L) ····· 1.65mW (max)
- Low operating power dissipation
  - M5M44400Axx-6, -6L ····· 550.0mW (max)
  - M5M44400Axx-7, -7L ····· 467.5mW (max)
  - M5M44400Axx-8, -8L ····· 412.5mW (max)
- Fast-page mode (1024-bit random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early write operation and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms /128ms (L) ($A_0 \sim A_9$)
- 16-bit parallel test mode capability

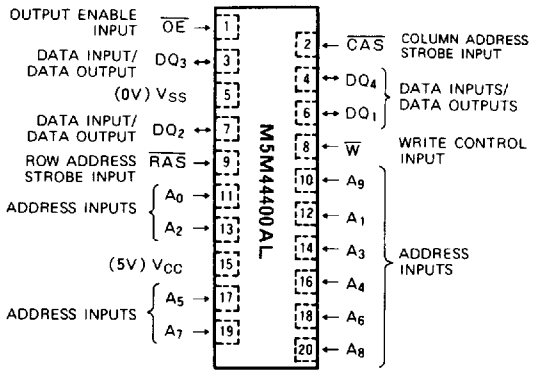
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



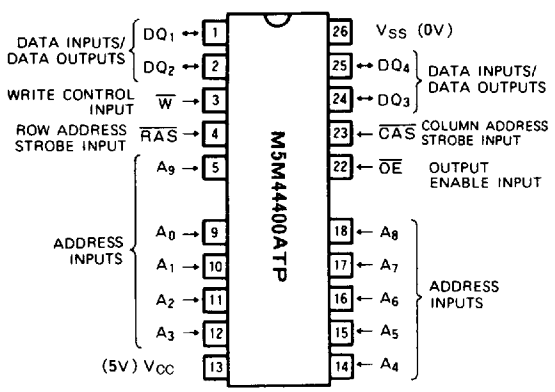
Outline 26P0Z (WJ:350 mil SOJ)
26P0J (J:300mil SOJ)



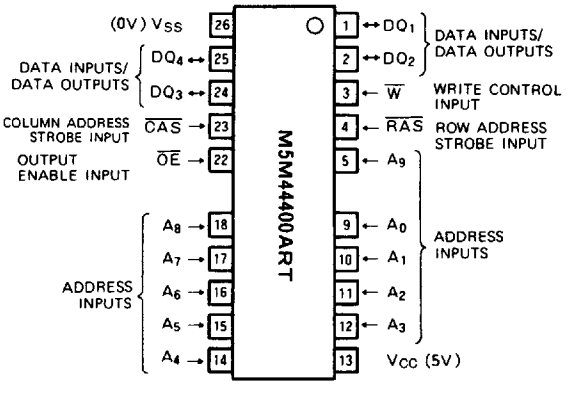
Outline 20P5L-B (ZIP)

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

PIN CONFIGURATION (TOP VIEW)



Outline 26P3Z-E (TSOP)



Outline 26P3Z-F (TSOP)

FUNCTION

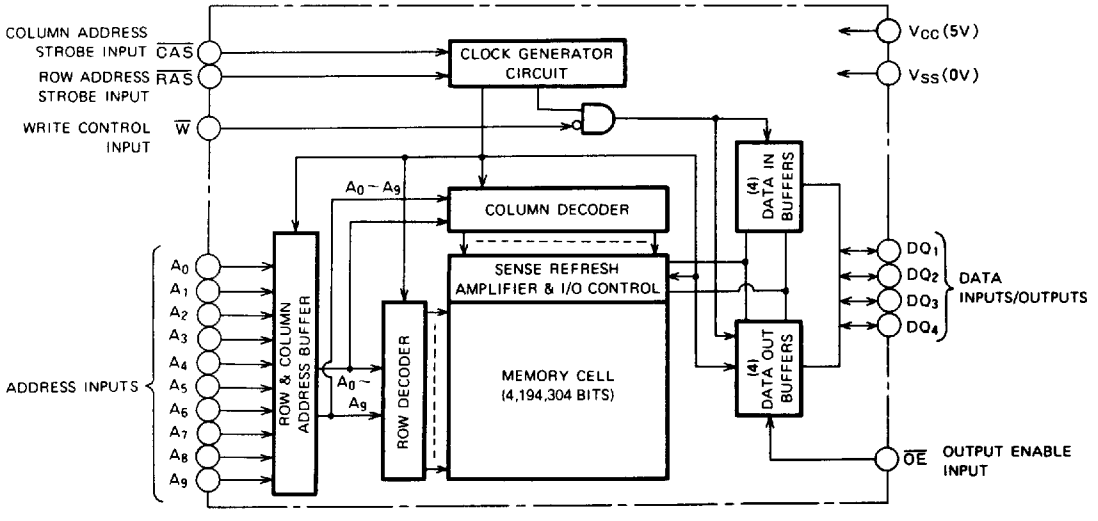
The M5M44400AWJ, J, L, TP, RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT active NAC nonactive, DNC don't care, VLD valid, IVD invalid, APD applied, OPN open

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	T_a=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage, all inputs		2.4		6.5	V
V_{IL}	Low level input voltage	DQ_1~DQ_4	−1.0		0.8	V
		Others	−2.0		0.8	V

Note 1 All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output Voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5, Other input pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M44400A-6, -6L	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min output open			100	mA
		M5M44400A-7, -7L				85	
		M5M44400A-8, -8L				75	
$I_{CC2(AV)}$	Supply current from V_{CC} stand-by (Note 5)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
		M5M44400AWJ, J, L(L)	$\overline{RAS}$=$\overline{CAS}$≧V_{CC}−0.5V, output open			0.2	
		M5M44400ATP, RT(L)				0.3	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M44400A-6, -6L	$\overline{RAS}$ cycling $\overline{CAS}$=V_{IH} t_{RC}=min. output open			100	mA
		M5M44400A-7, -7L				85	
		M5M44400A-8, -8L				75	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note3, 4)	M5M44400A-6, -6L	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cyclin t_{PC}=min. output open			100	mA
		M5M44400A-7, -7L				85	
		M5M44400A-8, -8L				75	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44400A-6, -6L	$\overline{CAS}$ before $\overline{RAS}$ refresh cyling t_{RC}=min output open			85	mA
		M5M44400A-7, -7L				75	
		M5M44400A-8, -8L				65	
$I_{CC8(AV)}$	Average supply current from V_{CC} Battery back-up (Note 5)	M5M44400AWJ, J, L(L)	$\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling W≦0.2V (Except for RAS falling edge) or ≧V_{CC}−0.2V A_0~A_{10}≦0.2V or ≧V_{CC}−0.2V D≦0.2V or ≧V_{CC}−0.2V Q=open t_{RC}=125μs t_{RAS}=t_{RASmin}~1μs			0.2	mA
		M5M44400ATP, RT(L)				0.3	

Note 2 Current flowing into an IC is positive, out is negative

3 $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate Maximum current is measured at the fastest cycle rate

4 $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading Specified values are obtained with the output open

CAPACITANCE (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M44400AWJ, J, TP, RT	V_I=V_{SS} f=1MHz V_I=25mVrms			5	pF
		M5M44400AL				6	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input					7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input					7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					7	pF
$C_{I/O}$	Input/Output capacitance, data ports					7	pF

SWITCHING CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		15		20		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		60		70		80	ns
t_{AA}	Column Address access time	(Note 6, 9)		30		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		35		40		45	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		15		20		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 11)	0	15	0	20	0	20	ns

Note 5 An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh)
Note the $\overline{RAS}$ may be cycled during the initial pause And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4/128ms (L)) of $\overline{RAS}$ inactivity before proper device operation is achieved

6 Measured with a load circuit equivalent to 2TTL loads and 100pF

7 Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

8 Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$ If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown

9 Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$

10 Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

11 $t_{OFF(max)}$ and $t_{OEZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq |\pm 10\mu A|$) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(T_a=0～70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Notes 12 13)

Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time	M5M44400A		16.4		16.4		16.4	ms
		M5M44400A (L)		128		128		128	ns
t_{RP}	$\overline{RAS}$ high pulse width		50		60		70		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	45	20	50	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 15)	15	30	15	35	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		15		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low	(Note 17)	0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low	(Note 17)	0		0		0		ns
t_{CDD}	Delay time $\overline{CAS}$ high to data	(Note 18)	15		20		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data	(Note 18)	15		20		20		ns
t_T	Transition time	(Note 19)	1	50	1	50	1	50	ns

Note 12 The timing requirements are assumed t_T = 5ns

13 $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals

14 $t_{RCD(max)}$ is specified as a reference point only If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA} $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$

15 $t_{RAD(max)}$ is specified as a reference point only If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$ access time is controlled exclusively by t_{AA}

16 $t_{ASC(max)}$ is specified as a reference point only If $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}

17 Either t_{DZC} or t_{DZO} must be satisfied

18 Either t_{CDD} or t_{ODD} must be satisfied

19 t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		120		140		160		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 20)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 20)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time		30		35		40		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low		15		20		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low		15		20		20		ns

Note 20 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		120		140		160		ns
t_{RAS}	$\overline{RAS}$ low pulse width		60	10000	70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		15	10000	20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		60		70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		15		20		20		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 22)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		10		15		15		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		20		ns
t_{WP}	Write pulse width		10		15		15		ns
t_{DS}	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		10		15		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		20		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 21)	160		185		205		ns
t_{RAS}	$\overline{RAS}$ low pulse width		95	10000	115	10000	125	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		50	10000	65	10000	65	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		95		115		125		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		50		65		65		ns
t_{RCS}	Read setup time befor $\overline{CAS}$ low		0		0		0		ns
t_{CWD}	Delay time, $\overline{CAS}$ lnw to W low	(Note 22)	35		40		40		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	80		90		100		ns
t_{AWD}	Delay time address to $\overline{W}$ low	(Note 22)	50		55		60		ns
t_{CWL}	$\overline{CAS}$ hold time after $\overline{W}$ iow		15		20		20		ns
t_{RWL}	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		20		ns
t_{WP}	Write pulse width		10		15		15		ns
t_{DS}	Data setup time before $\overline{W}$ low		0		0		0		ns
t_{DH}	Data hold time after $\overline{W}$ low		10		15		15		ns
t_{OEH}	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		20		ns

Note 21 t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{O\ D(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$

22 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and t_{CPWD} are specified as reference points only If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$, $t_{AWD} \geqq t_{AWD(min)}$ and $t_{CPWD} \geqq t_{CPWD(min)}$ (for fast page mode cycle only), the cycle is a read modify-write cycle and the DQ will contain the data read from the selected address If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate

Fast Page Mode Cycle (Read, Write, Read-Write and Read-Modify-Write Cycles) (Note 23)

Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		40		45		50		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		75		95		100		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 24)	100	100000	115	100000	135	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 25)	10	15	10	20	10	20	ns
t_{CPPH}	RAS hold time after $\overline{CAS}$ precharge		35		40		45		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 22)	35		40		45		ns

Note 23 All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle

24 $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed

25 $t_{CP(max)}$ is specified as a reference point only

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		15		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	25		30		30		ns

Note 26 Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode

TEST MODE SPECIFICATION (Note 27)

ELECTRICAL CHARACTERISTICS (T_a=0~70℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	M5M44400A-6, -6L	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}=t_{WC}$=min output open			115	mA
		M5M44400A-7, -7L				100	
		M5M44400A-8, -8L				85	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	M5M44400A-6, -6L	$\overline{RAS}$ cycling, $\overline{CAS}=V_{IH}$ t_{RC}=min output open			115	mA
		M5M44400A-7, -7L				100	
		M5M44400A-8, -8L				85	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4)	M5M44400A-6, -6L	$\overline{RAS}=V_{IL}$, $\overline{CAS}$ cycling t_{PC}=min output open			115	mA
		M5M44400A-7, -7L				100	
		M5M44400A-8, -8L				85	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44400A-6, -6L	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min output open			100	mA
		M5M44400A-7, -7L				85	
		M5M44400A-8, -8L				75	

Note 27 All previously specified electrical characteristics, switching characteristics and timing requirements are applicable to that of test mode

SWITCHING GHARACTERISTICS (T_a=0~70℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		20		25		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		65		75		85	ns
t_{AA}	Column address access time	(Note 6, 9)		35		40		45	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		40		45		50	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 6)		20		25		25	ns

TIMING REQUIREMENTS (T_a=0~70℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Notes 12, 13)

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	125		145		165		ns
t_{RAS}	$\overline{RAS}$ low pulse width	65	10000	75	10000	85	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	25	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	65		75		85		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	20		25		25		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	35		40		45		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	20		25		25		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	20		25		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read write/read modify write cycle time	(Note 21)	165		190		210		ns
t_{RAS}	$\overline{RAS}$ low pulse width		100	10000	120	10000	130	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		55	10000	70	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		100		120		130		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		55		70		70		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note 22)	40		45		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note 22)	85		95		105		ns
t_{AWD}	Delay time address to $\overline{W}$ low	(Note 22)	55		60		65		ns

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 22)

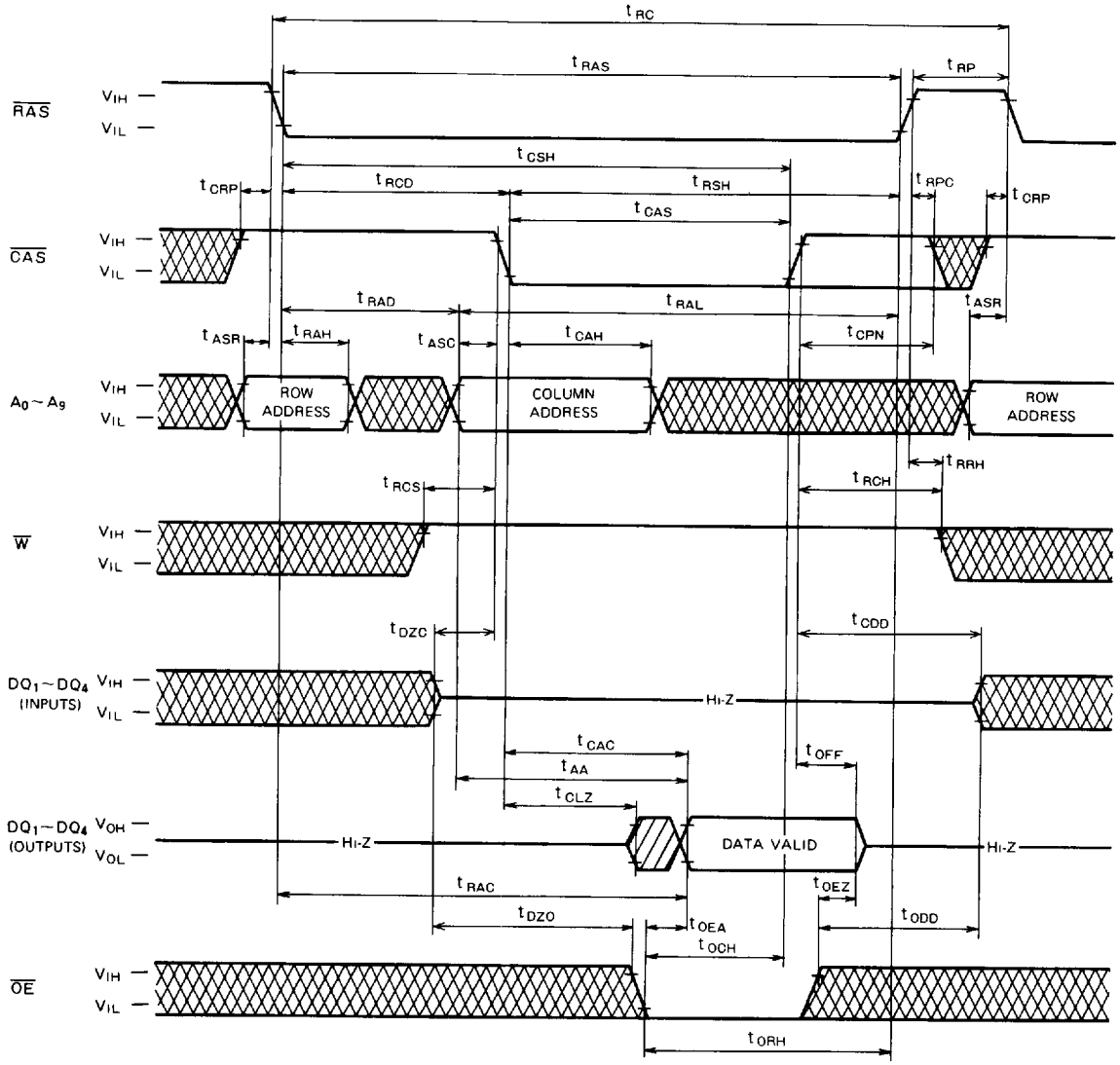
Symbol	Parameter		Limits						Unit
			M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
			Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time		45		50		55		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time		80		100		105		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	(Note 24)	110	100000	125	100000	145	100000	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		40		45		50		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 22)	40		45		50		ns

Test Mode Set Cycle

Symbol	Parameter	Limits						Unit
		M5M44400A-6, -6L		M5M44400A-7, -7L		M5M44400A-8, -8L		
		Min	Max	Min	Max	Min	Max	
t_{WSR}	Write setup time before $\overline{RAS}$ low	10		10		10		ns
t_{WHR}	Write hold time after $\overline{RAS}$ low	10		15		15		ns

Timing Diagrams (Note 28)

Read Cycle

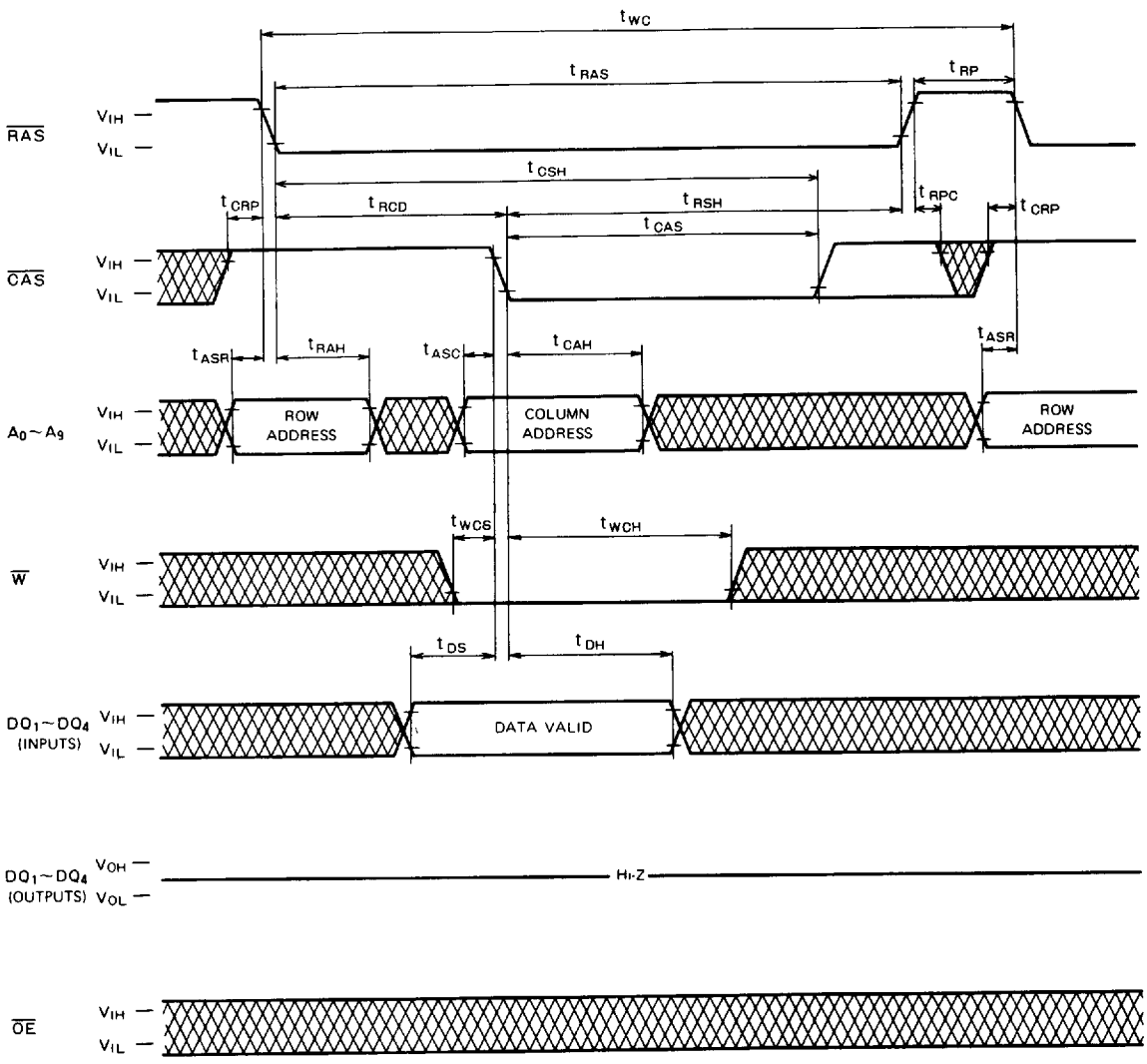


Note 28

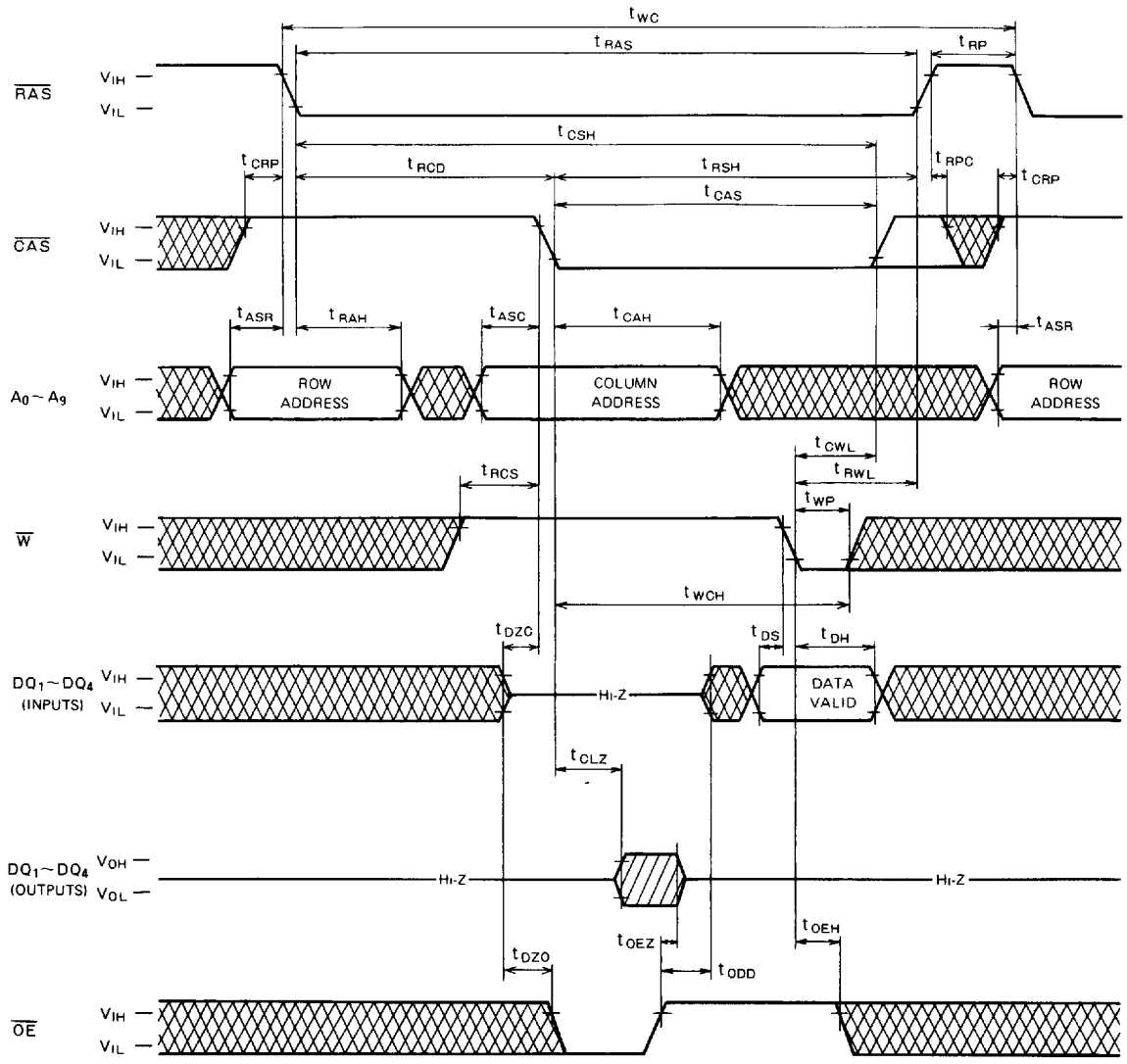
Indicates the don't care input
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

Indicates the invalid output

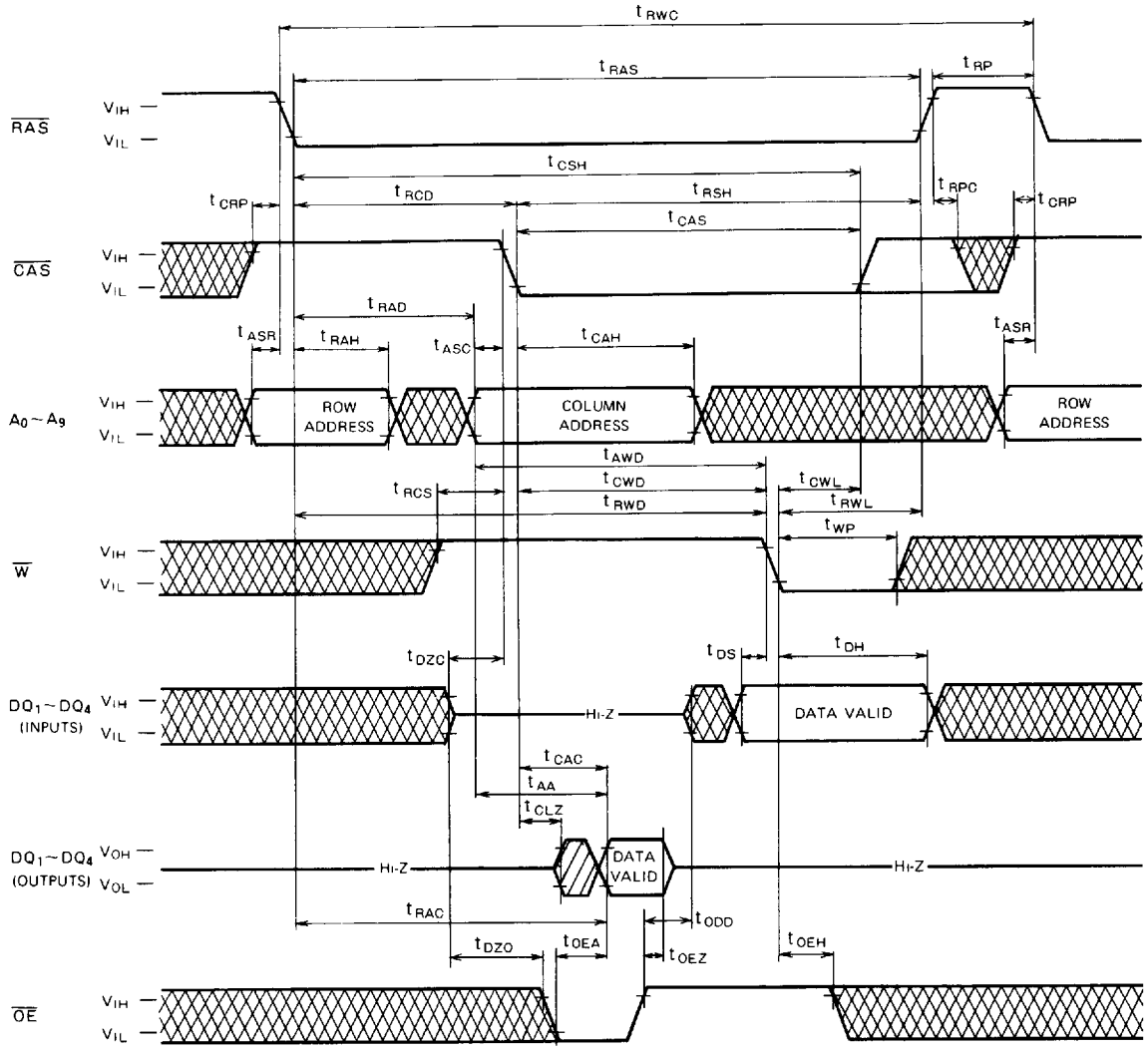
Write Cycle (Early write)



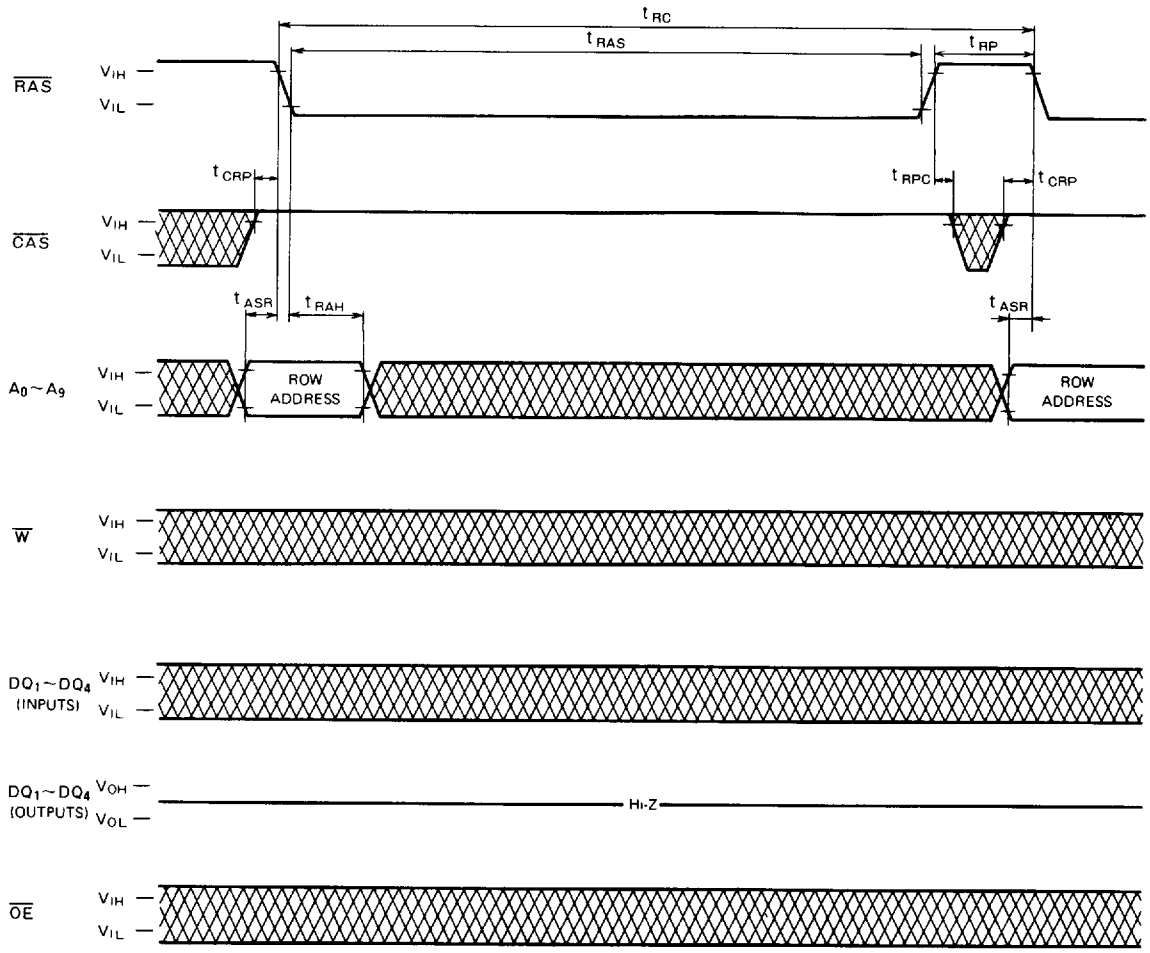
Write Cycle (Delayed Write)



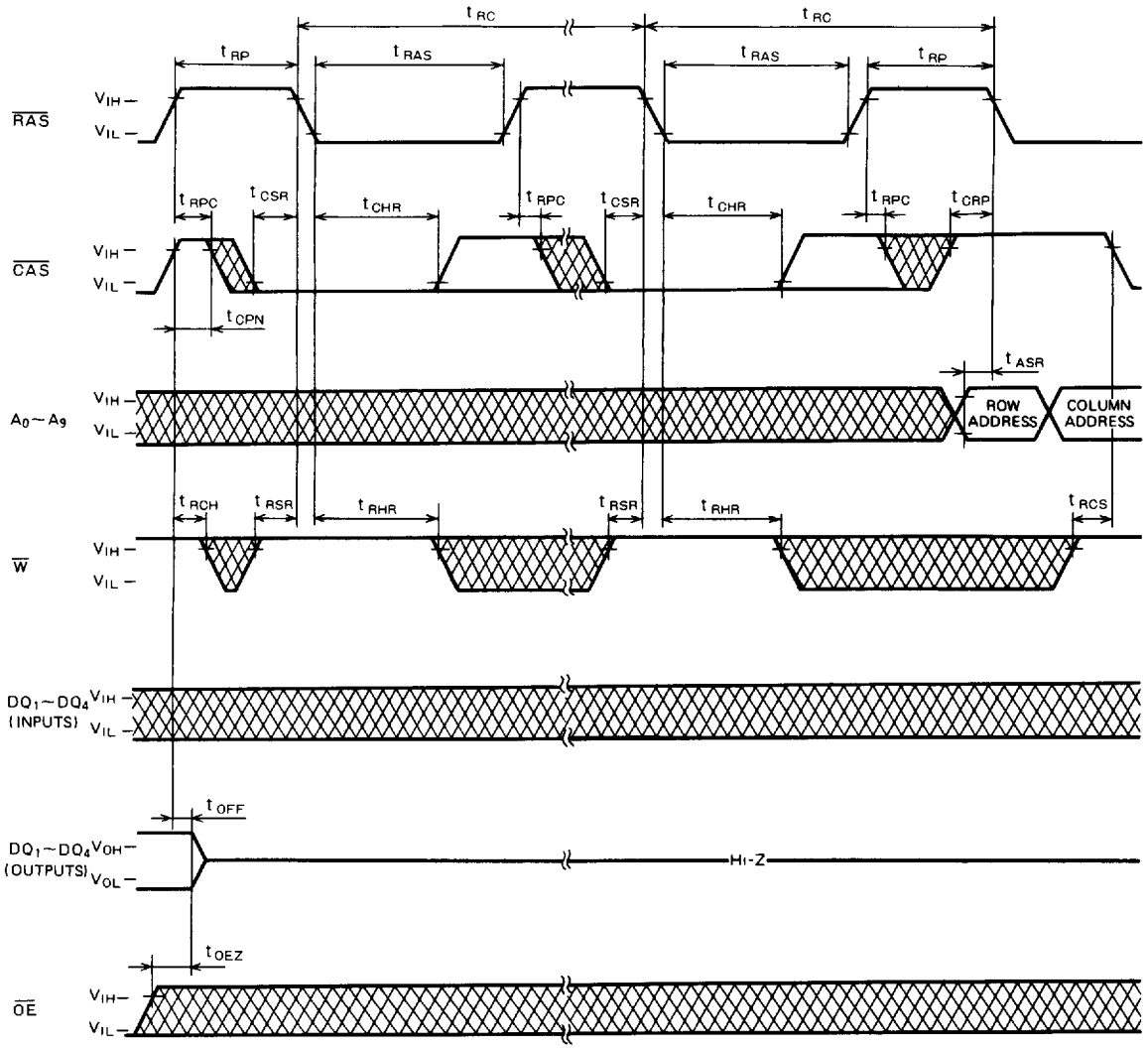
Read-Write, Read-Modify-Write Cycle



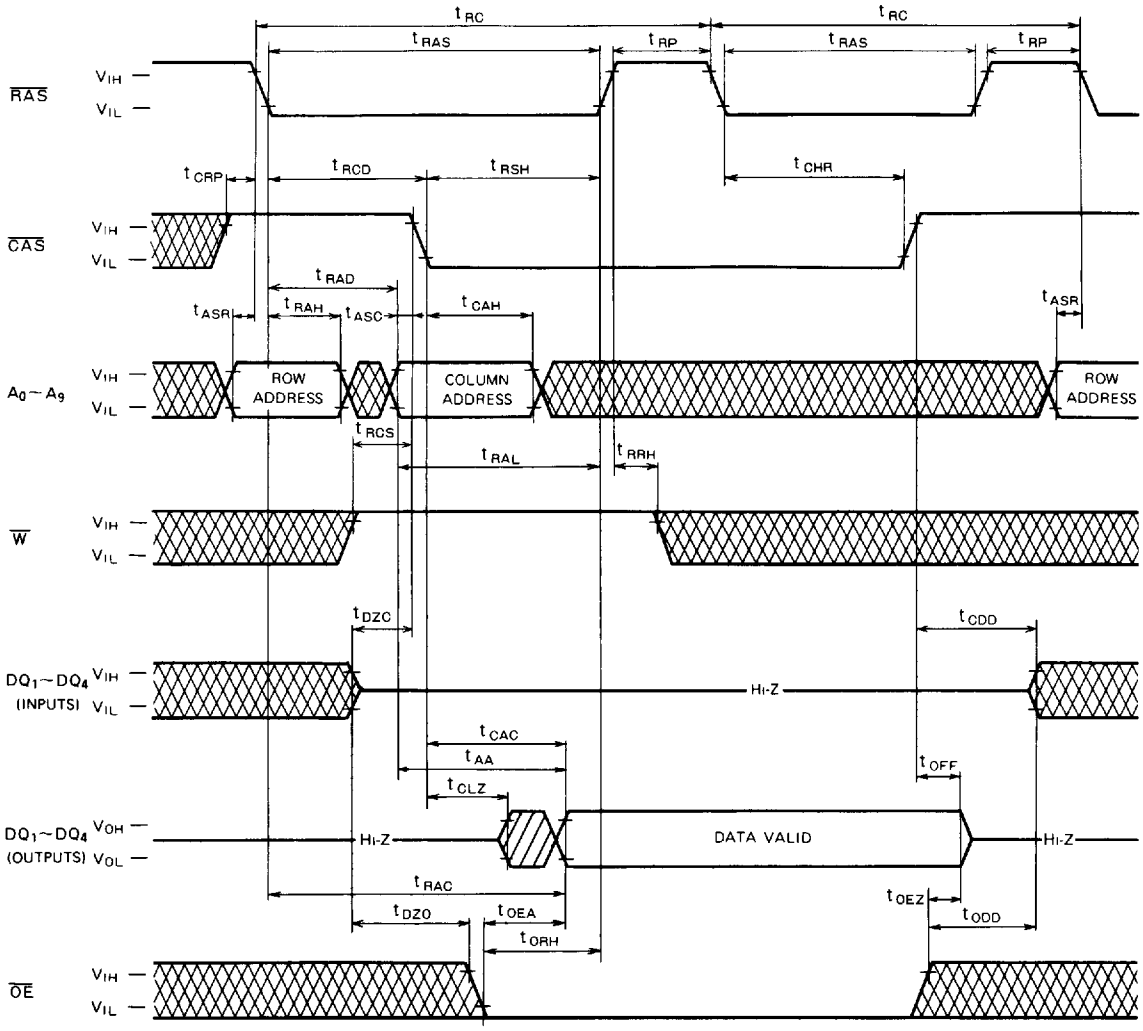
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

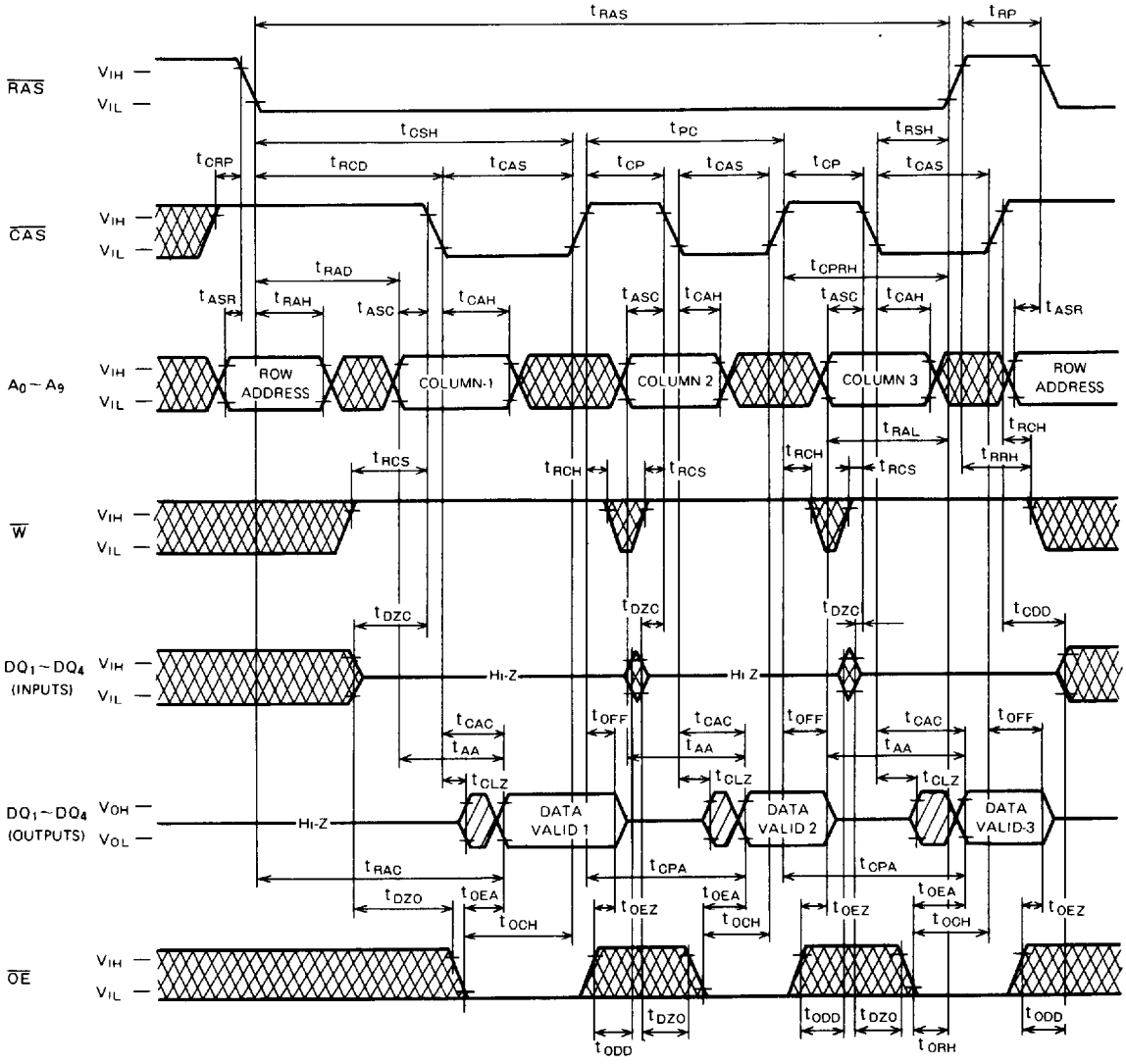


Hidden Refresh Cycle (Read) (Note 29)

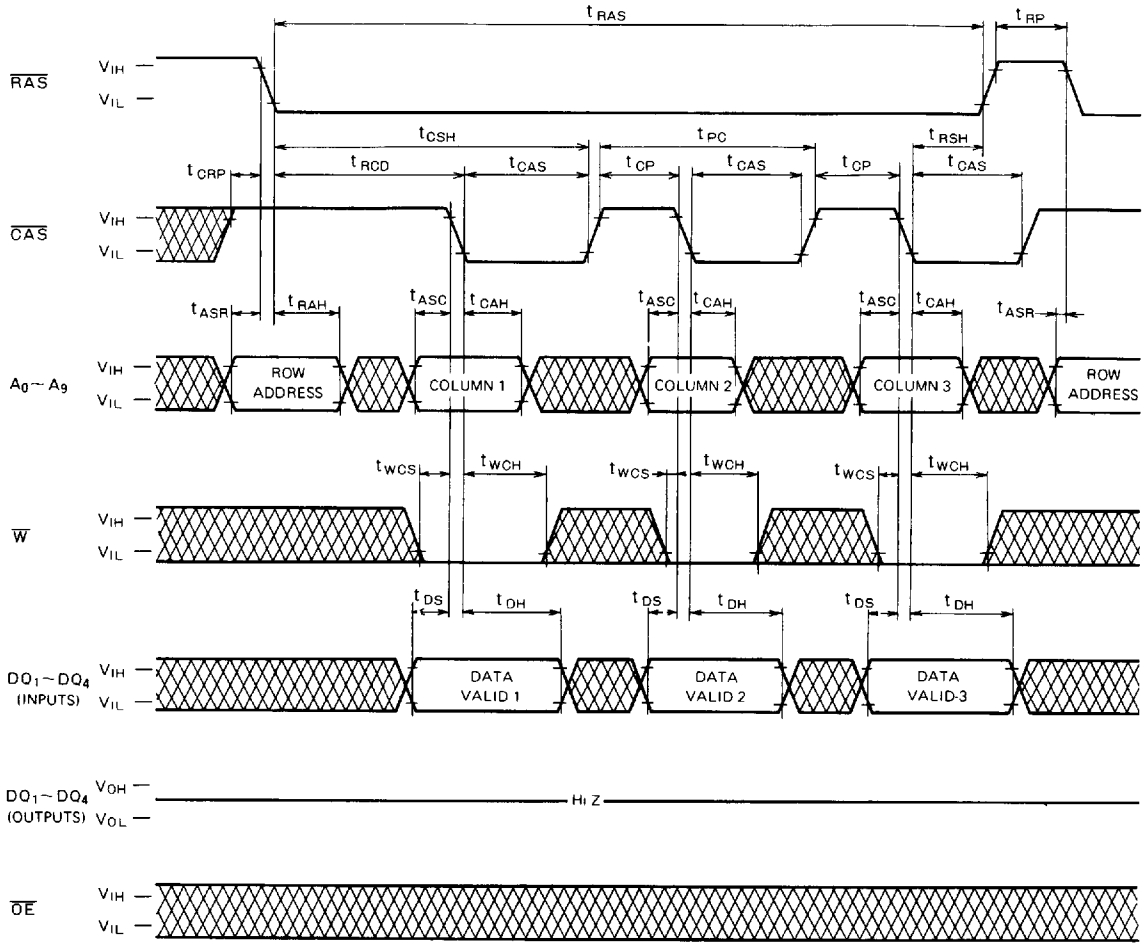


Note 29 Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above

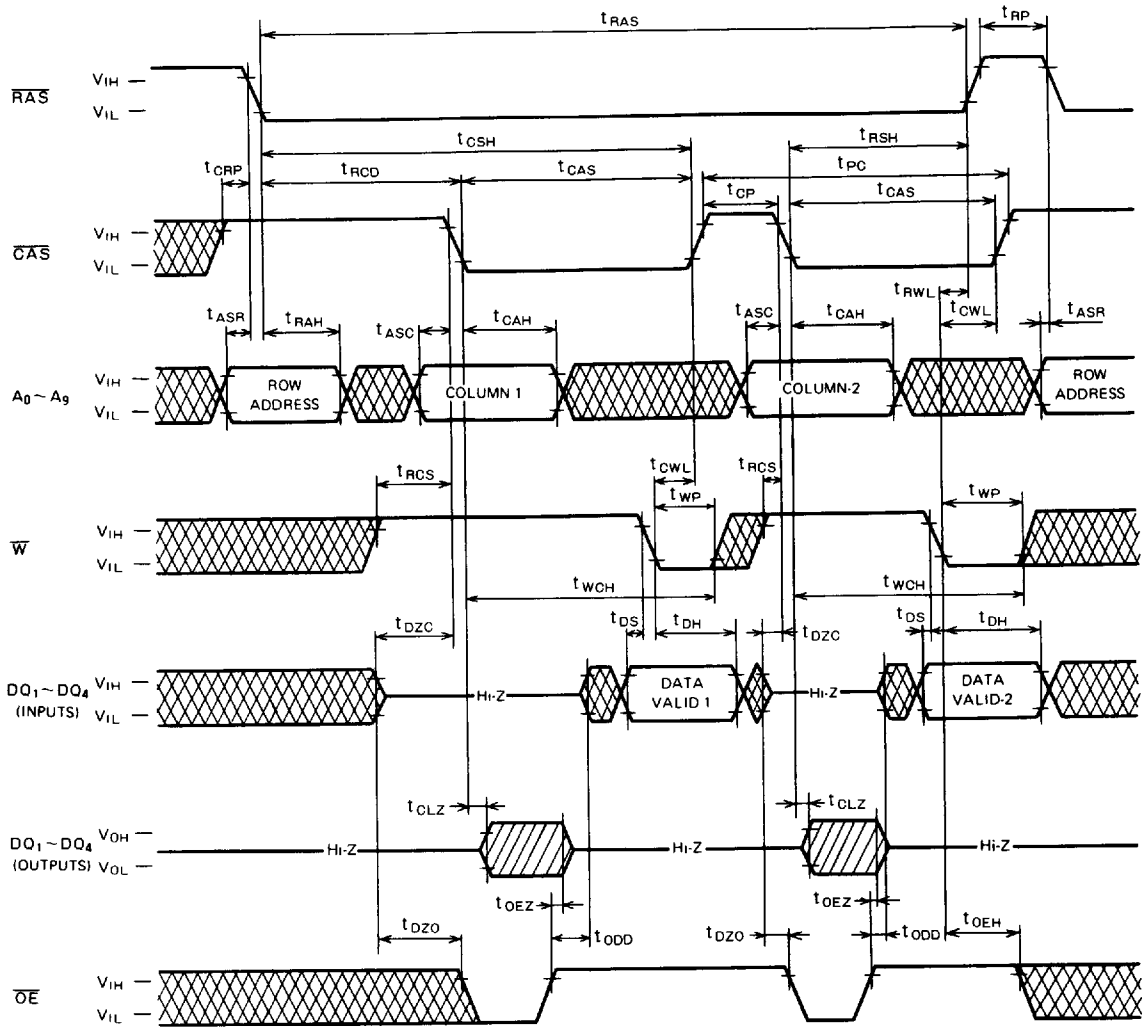
Fast Page Mode Read Cycle



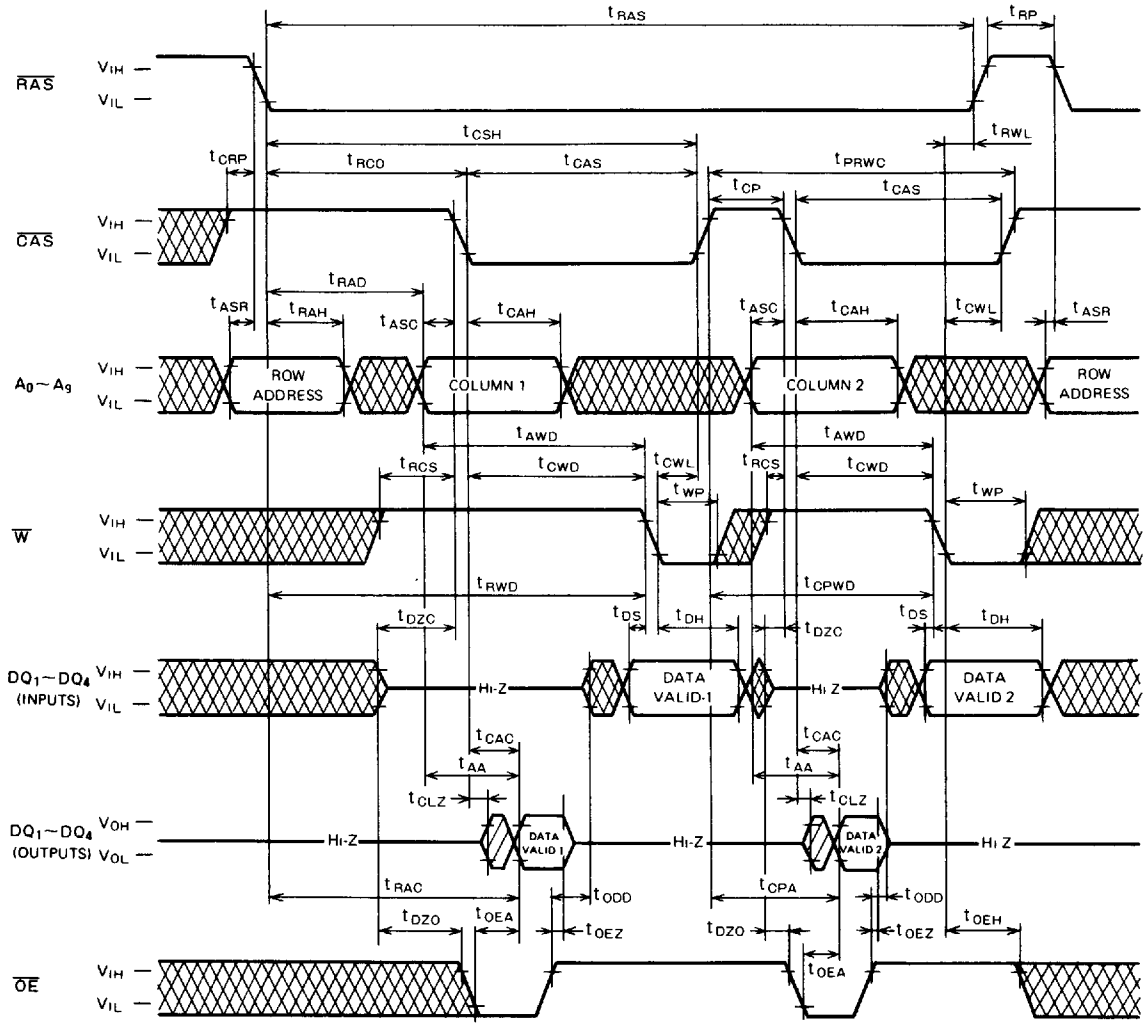
Fast Page Mode Write Cycle (Early Write)



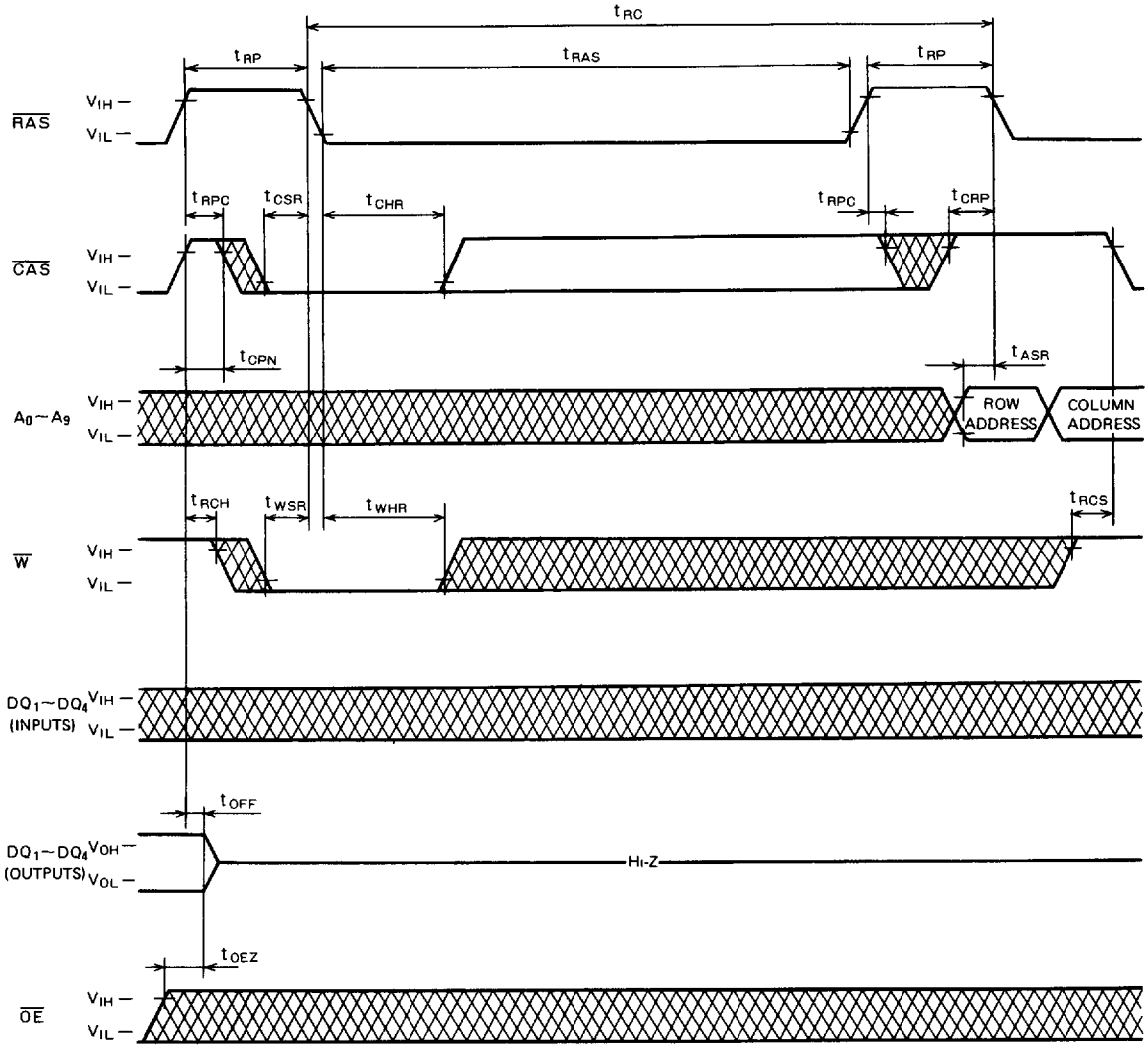
Fast Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Test Mode Set Cycle (Note 30)



Note 30 This cycle is also available for the initialization cycle, but in this case device enters test mode
The test mode function is initiated with a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified above timing diagram
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh or a $\overline{RAS}$ only refresh cycle
During the test mode, the device is internally organized as 4 bits wide (256 kilobytes deep) for each DQ (input/output) port
No addressing of A_0, A_1 (column only) is required
During a write cycle, data on the each DQ (input) pin is written in parallel into all 4 bits for each DQ port and can be written independently for each DQ port
During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4 bits are equal, and a LOW state if any bits differ
During the test mode operation, a WCBR cycle is used to perform refresh