

CMOS single-chip 8-bit microcontroller

80C32/80C32-16
80C52/80C52-16

FEATURES

- 80C51 architecture
 - 8k × 8 ROM
 - 256 × 8 RAM
 - Three 16-bit counter/timers
 - Full duplex serial channel
 - Boolean processor
- Memory addressing capability
 - 64k ROM and 64k RAM
- Power control modes:
 - Idle mode
 - Power-down mode
- CMOS and TTL compatible
- Two speed ranges:
 - 3.5 to 12MHz
 - 3.5 to 16MHz
- Military temperature ranges

DESCRIPTION

The Philips 80C52 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The CMOS 80C52 is functionally compatible with the NMOS SCN8032/8052 microcontrollers. The Philips CMOS technology combines the high-speed and density characteristics of HMOS with the low-power attributes of CMOS. Philips epitaxial substrate minimizes latch-up sensitivity.

The 80C52 contains an 8k × 8 ROM, a 256 × 8 RAM, 32 I/O lines, three 16-bit counter/timers, a six-source, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 80C52 has two software selectable modes of power reduction – idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running.

To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-up, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON.

DESIGN CONSIDERATIONS

At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

When the idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when idle is terminated by reset, the instruction following the one that invokes idle should not be one that writes to a port pin or to external memory.

Table 1 shows the state of I/O ports during low current operating modes.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
40-Pin Ceramic DIP 12MHz	80C32/BQA	GDIP1-T40
40-Pin Ceramic DIP 12MHz	80C52/BQA	GDIP1-T40
40-Pin Ceramic DIP 16MHz	80C32-16/BQA	GDIP1-T40
40-Pin Ceramic DIP 16MHz	80C52-16/BQA	GDIP1-T40
44-Pin Ceramic QFP, 12 MHz	80C32-12/BMA	GQCC1-J44
44-Pin Ceramic QFP 12 MHz	80C52-12/BMA	GQCC1-J44
44-Pin Ceramic QFP 16MHz	80C32-16/BMA	GQCC1-J44
44-Pin Ceramic QFP 16MHz	80C52-16/BMA	GQCC1-J44

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

CMOS single-chip 8-bit microcontroller

80C32/80C32-16
80C52/80C52-16

PIN CONFIGURATION

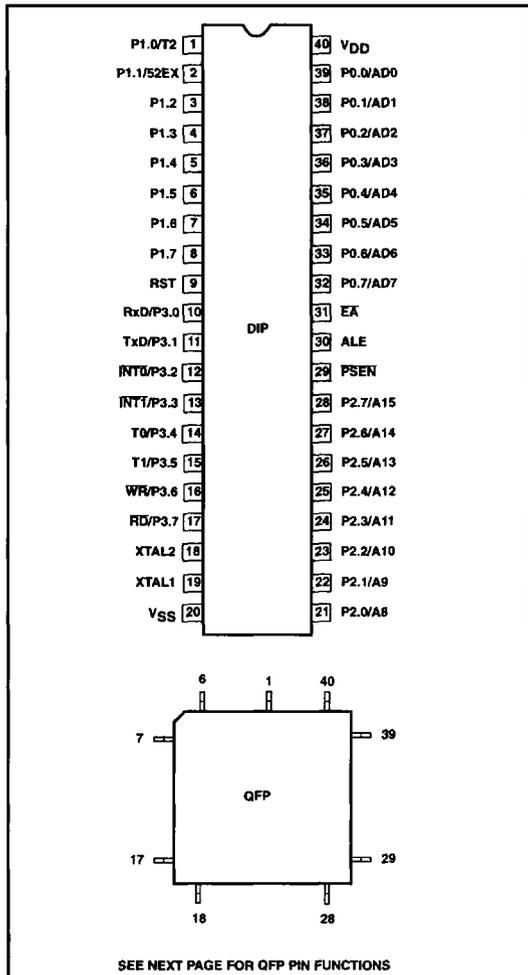


Table 1. External Pin Status During Idle and Power-Down Modes

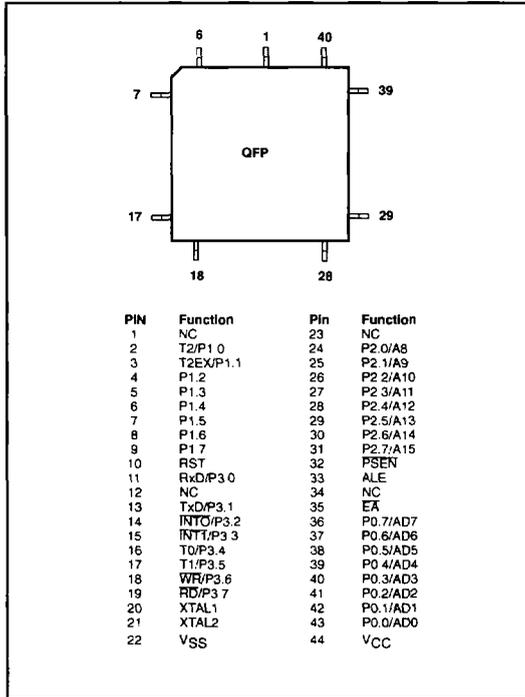
MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

CMOS single-chip 8-bit microcontroller

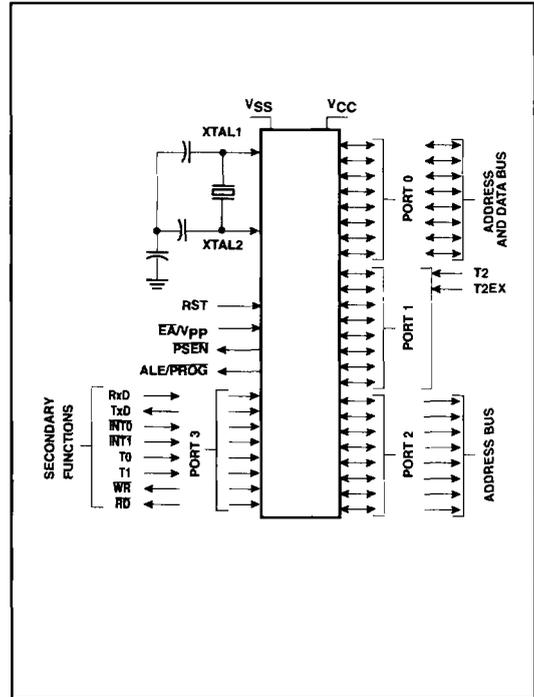
80C32/80C32-16

80C52/80C52-16

QFP PIN FUNCTIONS



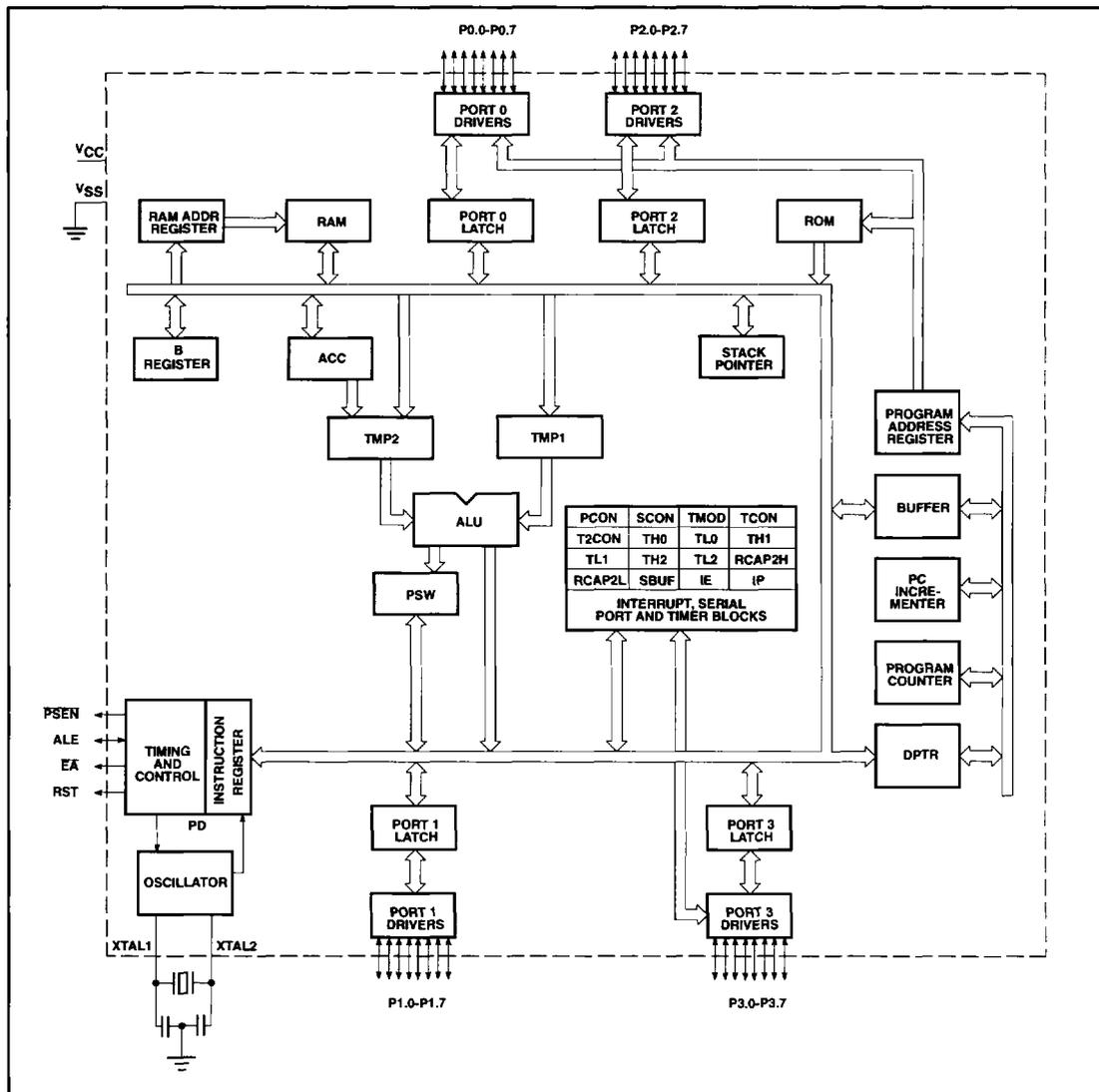
LOGIC SYMBOL



CMOS single-chip 8-bit microcontroller

80C32/80C32-16
80C52/80C52-16

BLOCK DIAGRAM



CMOS single-chip 8-bit microcontroller

80C32/80C32-16

80C52/80C52-16

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION			
	DIP	QFP					
V _{SS}	20	22	I	Ground: 0V reference.			
V _{CC}	40	44	I	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.			
P0.0-0.7	39-32	43-46	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C52. External pull-ups are required during program verification.			
P1.0-P1.7	1-8	2-9	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Pins P1.0 and P1.1 also. Port 1 also receives the low-order address byte during program memory verification. Port 1 also serves alternate functions for timer 2:			
				1	2	I	T2 (P1.0): Timer/counter 2 external count input.
				2	3	I	T2EX (P1.1): Timer/counter 2 trigger input.
P2.0-P2.7	21-28	24-31	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.			
P3.0-P3.7	10-17	11, 13-19	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:			
				10	11	I	RxD (P3.0): Serial input port
				11	13	O	TxD (P3.1): Serial output port
				12	14	I	INT0 (P3.2): External interrupt
				13	15	I	INT1 (P3.3): External interrupt
				14	16	I	T0 (P3.4): Timer 0 external input
				15	17	I	T1 (P3.5): Timer 1 external input
				16	18	O	WR (P3.6): External data memory write strobe
				17	19	O	RD (P3.7): External data memory read strobe
RST	9	10	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V _{SS} permits a power-on reset using only an external capacitor to V _{CC} .			
ALE	30	33	I/O	Address Latch Enable: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.			
PSEN	29	32	O	Program Store Enable: The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.			
EA	31	35	I	External Access Enable/Programming Supply Voltage: EA must be externally held low to enable the device to fetch code from external program memory locations 0000H to 1FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH.			
XTAL1	19	21	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.			
XTAL2	18	20	O	Crystal 2: Output from the inverting oscillator amplifier.			

CMOS single-chip 8-bit microcontroller

80C32/80C32-16

80C52/80C52-16

ABSOLUTE MAXIMUM RATING^{1, 2, 3}

PARAMETER	RATING	UNIT
Operating temperature under bias	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Voltage on any pin to V_{SS}	-0.5 to +6.5	V
Input, output current on any two pins	±10	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.5	W

DC ELECTRICAL CHARACTERISTICS

 $T_A = -55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ⁴	MAX	
V_{IL}	Input low voltage, except \overline{EA}		-0.5		$0.2V_{CC}-0.25$	V
V_{IL1}	Input low voltage to \overline{EA}		0		$0.2V_{CC}-0.45$	V
V_{IH}	Input high voltage, except XTAL1, RST		$0.2V_{CC}+1.1$		$V_{CC}+0.5$	V
V_{IH1}	Input high voltage, XTAL1, RST		$0.7V_{CC}+0.2$		$V_{CC}+0.5$	V
V_{OL}	Output low voltage, ports 1, 2, 3	$I_{OL} = 1.6\text{mA}^5$			0.45	V
V_{OL1}	Output low voltage, port 0, ALE, PSEN	$I_{OL} = 3.2\text{mA}^5$			0.45	V
V_{OH}	Output high voltage, ports 1, 2, 3, ALE, PSEN ⁶	$I_{OH} = -60\mu\text{A}$, $I_{OH} = -25\mu\text{A}$ $I_{OH} = -10\mu\text{A}$	2.4			V
			$0.75V_{CC}$			V
			$0.9V_{CC}$			V
V_{OH1}	Output high voltage (port 0 in external bus mode)	$I_{OH} = -80\mu\text{A}$, $I_{OH} = -300\mu\text{A}$ $I_{OH} = -80\mu\text{A}$	2.4			V
			$0.75V_{CC}$			V
			$0.9V_{CC}$			V
I_{IL}	Logical 0 input current, ports 1, 2, 3	$V_{IN} = 0.45\text{V}$			-75	μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	See note 7			-750	μA
I_{L1}	Input leakage current, port 0	$V_{IN} = V_{IL}$ or V_{IH}			±10	μA
I_{CC}	Power supply current: Active mode @ 16MHz ⁸ Idle mode @ 16MHz ⁸ Power-down mode	See note 9		12.8	39	mA
				1.5	7	mA
				3	75	μA
R_{RST}	Internal reset pull-down resistor		50		300	k Ω
C_{IO}	Pin capacitance ¹³				10	pF

CMOS single-chip 8-bit microcontroller

80C32/80C32-16
80C52/80C52-16

AC ELECTRICAL CHARACTERISTICS

T_A = -55°C ≤ T_A ≤ +125°C, V_{CC} = 5V ±10%, V_{SS} = 0V^{10, 11}

SYMBOL	FIGURE	PARAMETER	12MHz CLOCK		16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1/t _{CLCL}	1	Oscillator frqcy: Speed Versions 8XC32/52 E					3.5	16	MHz
t _{LHLL}	1	ALE pulse width	112		68		2t _{CLCL} -55		ns
t _{AVLL}	1	Address valid to ALE low	13		5		t _{CLCL} -70		ns
t _{LLAX}	1	Address hold after ALE low	33		12		t _{CLCL} -50		ns
t _{LLIV}	1	ALE low to valid instruction in		218		132		4t _{CLCL} -115	ns
t _{LLPL}	1	ALE low to PSEN low	28		7		t _{CLCL} -55		ns
t _{PLPH}	1	PSEN pulse width	190		125		3t _{CLCL} -60		ns
t _{PLIV}	1	PSEN low to valid instruction in		130		65		3t _{CLCL} -120	ns
t _{PXIX}	1	Input instruction hold after PSEN	0		0		0		ns
t _{PXIZ}	1	Input instruction float after PSEN		58		37		t _{CLCL} -25	ns
t _{AVIV}	1	Address to valid instruction in		312		188		5t _{CLCL} -120	ns
t _{PLAZ}	1	PSEN low to address float		25		25		25	ns
Data Memory									
t _{RLRH}	2, 3	RD pulse width	400		270		6t _{CLCL} -100		ns
t _{WLWH}	2, 3	WR pulse width	400		270		6t _{CLCL} -100		ns
t _{RLDV}	2, 3	RD low to valid data in		232		123		5t _{CLCL} -185	ns
t _{RHDX}	2, 3	Data hold after RD	0		0		0		ns
t _{RHDZ}	2, 3	Data float after RD		82		38		2t _{CLCL} -85	ns
t _{LLDV}	2, 3	ALE low to valid data in		496		320		8t _{CLCL} -170	ns
t _{AVDV}	2, 3	Address to valid data in		565		370		9t _{CLCL} -185	ns
t _{LLWL}	2, 3	ALE low to RD or WR low	185	315	120	250	3t _{CLCL} -65	3t _{CLCL} +65	ns
t _{AVWL}	2, 3	Address valid to WR low or RD low	188		102		4t _{CLCL} -145		ns
t _{QVWX}	2, 3	Data valid to WR transition	8		5		t _{CLCL} -75		ns
t _{WHOX}	2, 3	Data hold after WR	18		5		t _{CLCL} -65		ns
t _{RLAZ}	2, 3	RD low to address float		0		0		0	ns
t _{WHLH}	2, 3	RD or WR high to ALE high	18	148	5	127	t _{CLCL} -65	t _{CLCL} +65	ns
External Clock									
t _{CHCX}	5	High time	20		20		20		ns
t _{CLCX}	5	Low time	20		20		20		ns
t _{CLCH}	5	Rise time ¹²		20		20		20	ns
t _{CHCL}	5	Fall time ¹²		20		20		20	ns
Shift Register									
t _{XLXL}	4	Serial port clock cycle time	1000		740		12t _{CLCL}		ns
t _{QVXH}	4	Output data setup to clock rising edge	700		484		10t _{CLCL} -133		ns
t _{XHQX}	4	Output data hold after clock rising edge	50		6		2t _{CLCL} -117		ns
t _{XHDX}	4	Input data hold after clock rising edge	0		0		0		ns
t _{XHDV}	4	Clock rising edge to input data valid		700		484		10t _{CLCL} -133	ns

NOTES: On following page.

CMOS single-chip 8-bit microcontroller

80C32/80C32-16

80C52/80C52-16

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
4. Typical ratings are not guaranteed. The values listed are at room temperature, 5V.
5. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL} s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
6. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.
7. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
8. I_{CCMax} at other frequencies is given by: Active mode: $I_{CCMax} = 0.94 \times \text{FREQ} + 23.72$; Idle mode: $I_{CCMax} = 0.14 \times \text{FREQ} + 4.32$, where FREQ is the external oscillator frequency in MHz. I_{CCMAX} is given in mA. See Figure 8.
9. See Figures 9 through 12 for I_{CC} test conditions.
10. Parameters are valid over operating temperature range unless otherwise specified.
11. Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
12. This parameter is guaranteed but not tested to the limits specified.
13. C_{IO} is tested initially and after any design or process changes which may affect capacitance.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A - Address
- C - Clock
- D - Input data
- H - Logic level high
- I - Instruction (program memory contents)
- L - Logic level low, or ALE
- P - PSEN

- Q - Output data
- R - \overline{RD} signal
- t - Time
- V - Valid
- W - \overline{WR} signal
- X - No longer a valid logic level
- Z - Float

Examples:

- t_{AVLL} = Time for address valid to ALE low.
- t_{LLPL} = Time for ALE low to PSEN low.

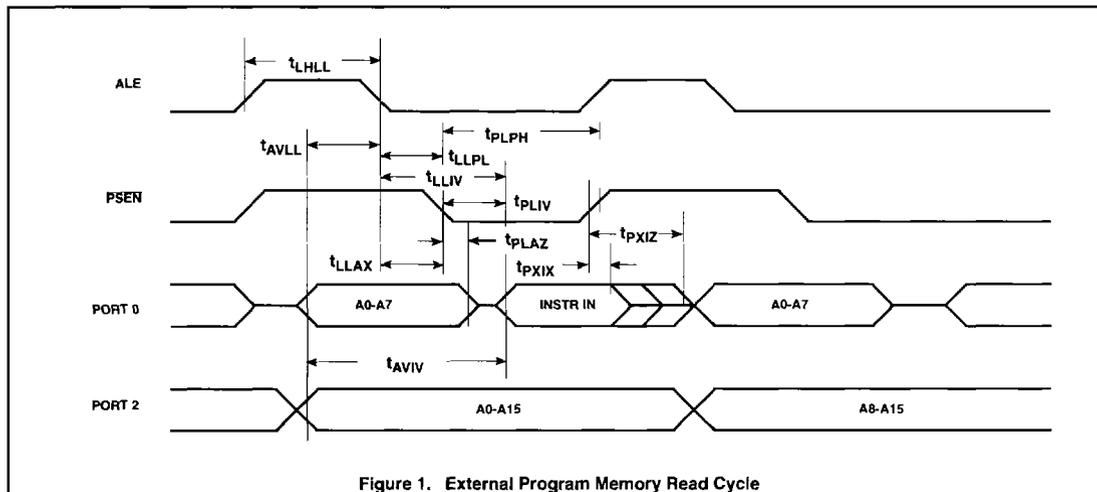


Figure 1. External Program Memory Read Cycle

CMOS single-chip 8-bit microcontroller

80C32/80C32-16

80C52/80C52-16

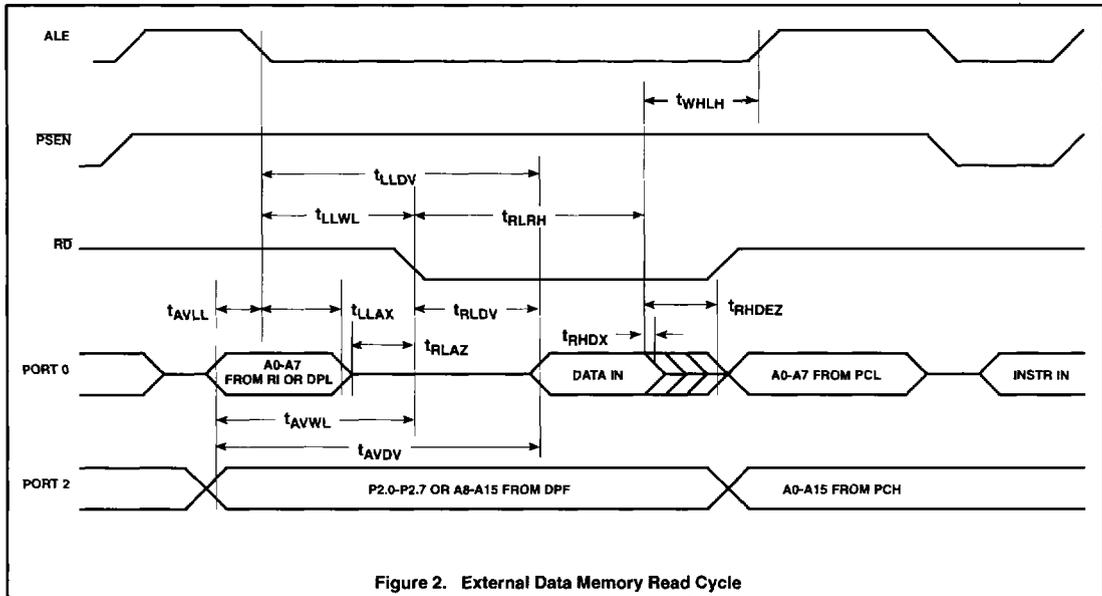


Figure 2. External Data Memory Read Cycle

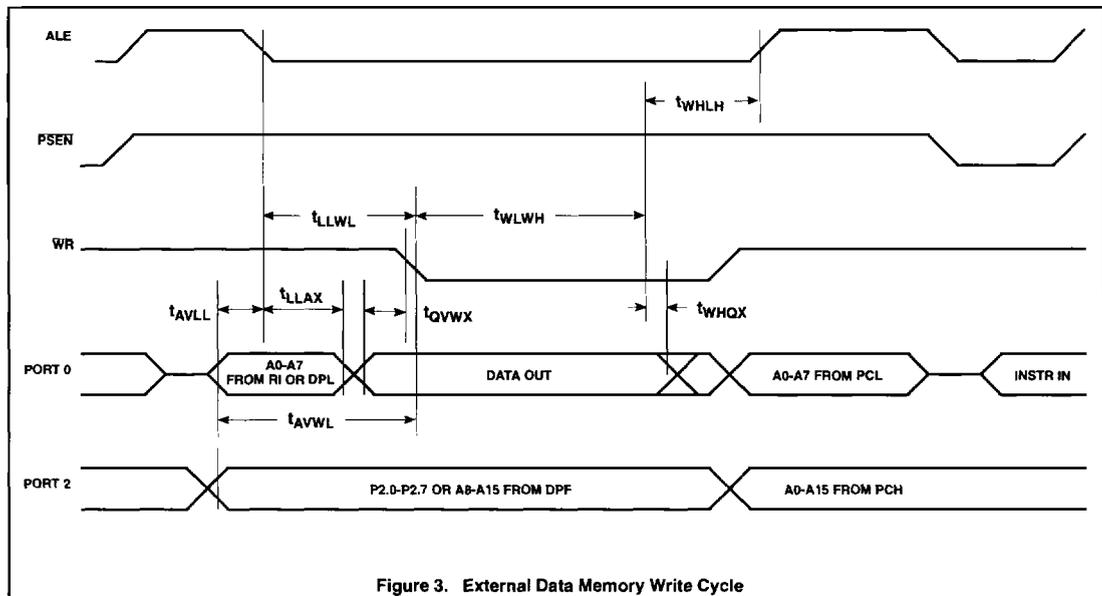


Figure 3. External Data Memory Write Cycle

CMOS single-chip 8-bit microcontroller

80C32/80C32-16

80C52/80C52-16

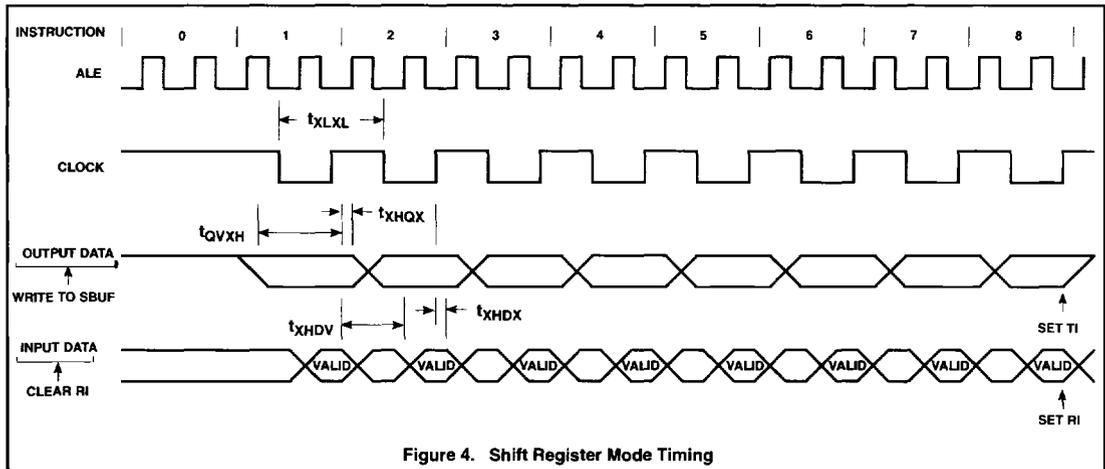


Figure 4. Shift Register Mode Timing

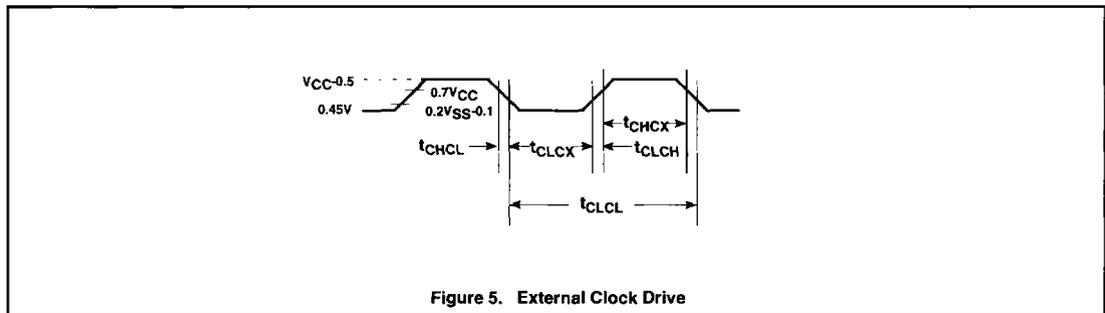


Figure 5. External Clock Drive

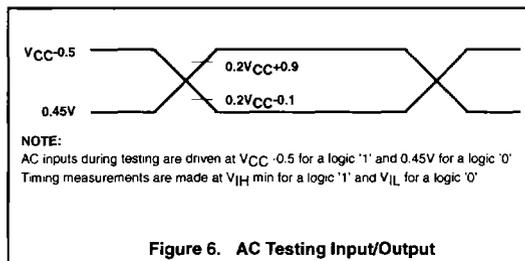


Figure 6. AC Testing Input/Output

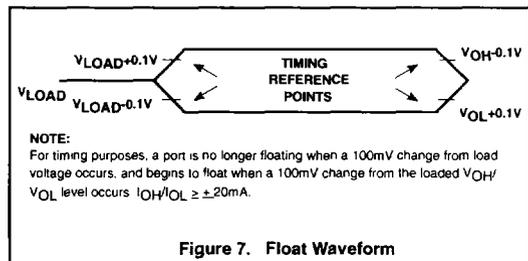
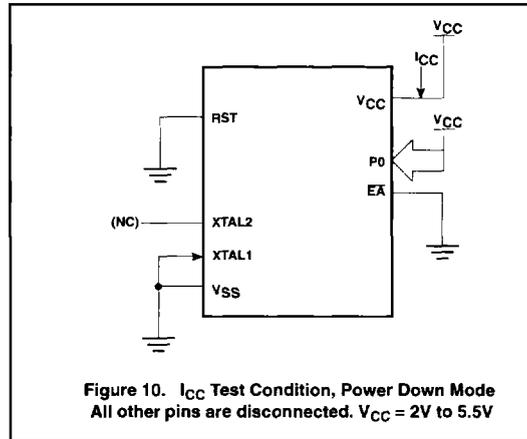
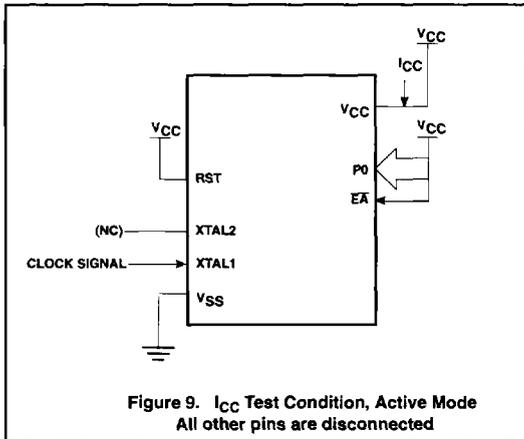
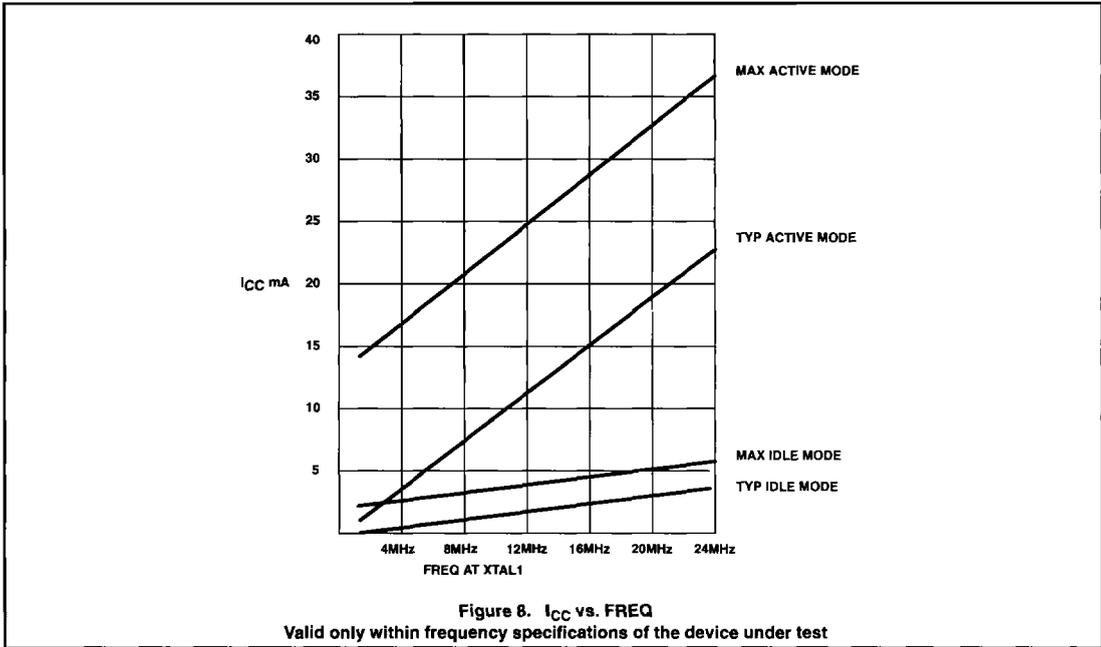


Figure 7. Float Waveform

CMOS single-chip 8-bit microcontroller

80C32/80C32-16

80C52/80C52-16



CMOS single-chip 8-bit microcontroller

80C32/80C32-16
80C52/80C52-16

