

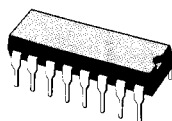
## 2 x 8 CROSSPOINT MATRIX

- VERY LOW ON RESISTANCE
- HIGH CROSS-TALK AND OFF-STATE ISOLATION
- SERIAL SWITCH ADDRESSING,  $\mu$ -PROCESSOR COMPATIBLE

### DESCRIPTION

The M089 is a 2 x 8 crosspoint matrix consisting of 16 N-channel MOS transistors.

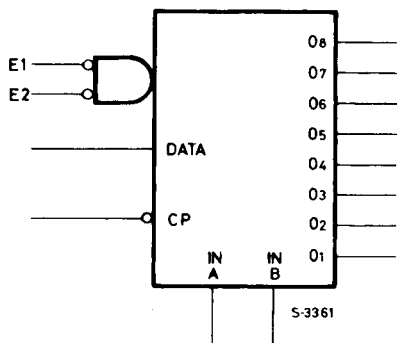
The device has been specially designed to provide switches with low cross-talk, high off-state isolation (both better than - 90dB) and low on-resistance.



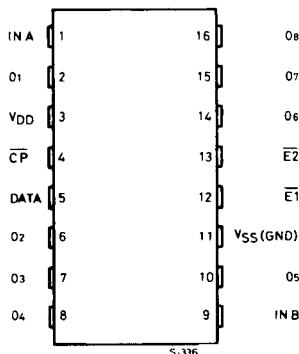
(Plastic)  
(Ceramic Frit-seal)  
(Ceramic Metal-seal)

**ORDER CODES :** M089 B1  
M089 F1  
M089 D1

### LOGIC DIAGRAM



### PIN CONFIGURATION

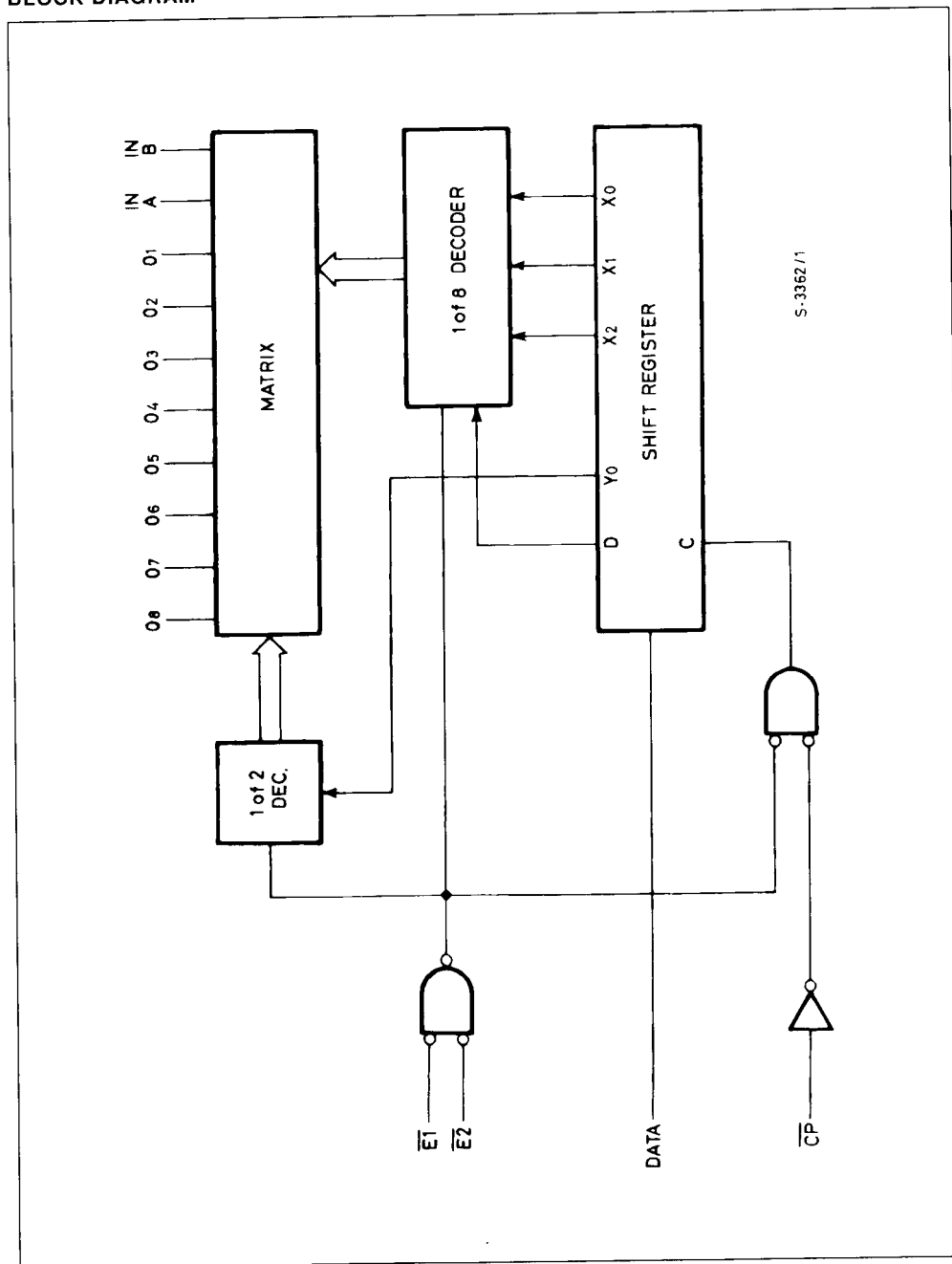


### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	- 0.5 to 17	V
$V_I$	Input Voltage Pins 4, 5, 12, 13	- 0.5 to 17	V
$V_{IN-V_{OUT}}$	Differential Voltage Across any Disconnected Switch	10	V
$P_{tot}$	Total Power Dissipation	640	mW
$T_{op}$	Operating Temperature Range : for Plastic for Ceramic	0 to 70 - 40 to 70	$^{\circ}$ C
$T_{stg}$	Storage Temperature Range	- 65 to 150	$^{\circ}$ C

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The M089 is capable of forming any combination of switch conditions in an 8 x 2 matrix. Each switch is individually set and a latch maintains it in its set condition.

The switch address and control bits are loaded serially into an internal shift register (5 bits), when inputs E<sub>1</sub> and E<sub>2</sub> are low. The address bits consist of : 3 input selection bits (X<sub>0</sub>-X<sub>2</sub>) and a single output selection bit (Y<sub>0</sub>). A fifth (control) bit (D) defines whether the chosen switch is to be opened or closed.

D	Y <sub>0</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>
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M089 Shift Register Bit Allocation

Data bits are clocked into the shift register on the high to low transition of the clock input (CP). If more than 5 clock transmission are applied during loading of the shift register the last 5 data bits are loaded into it. The status of the switch addressed changes

ENABLE INPUTS TRUTH TABLE

$\bar{E}_1$	$\bar{E}_2$	Function
		Data Load
L	L	Addressed Switch Changed
$\neg$ L	L	
L	$\neg$ L	
$\neg$ L	$\neg$ L	

DATA BIT TRUTH TABLE

Data	Switch Status after Enable Transition
L	Disconnect
H	Connect

on the low to high transition of one or both enable inputs.

DATA BITS TRUTH TABLE FOR SWITCH SELECTION

	O <sub>1</sub> Y <sub>0</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub>	O <sub>2</sub>	O <sub>3</sub>	O <sub>4</sub>	O <sub>5</sub>	O <sub>6</sub>	O <sub>7</sub>	O <sub>8</sub>
IN A	1111	1011	1101	1001	1110	1010	1100	1000
IN B	0111	0011	0101	0001	0110	0010	0100	0000

For example to address the switch connecting IN A to O<sub>5</sub> the shift register must be loaded with the code :

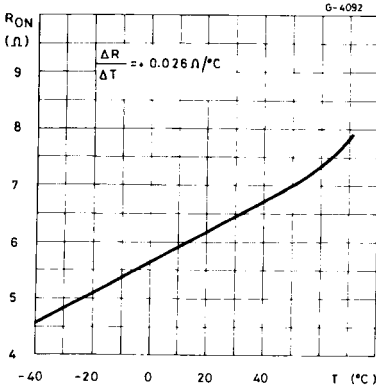
	D Y <sub>0</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub>
to Connect	11110
to Disconnect	01110

**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 0$  to  $70^{\circ}\text{C}$  for M089 B1 ;  $-40$  to  $70^{\circ}\text{C}$  for M089 F1, D1 ;  $V_{DD} = 14\text{V}$  to  $16\text{V}$  unless otherwise specified)

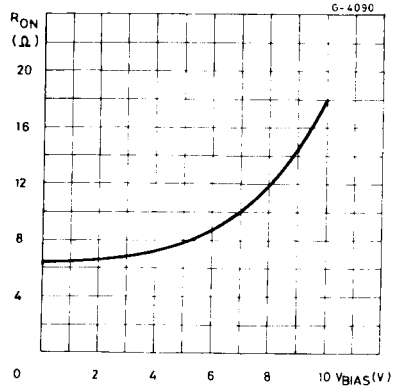
Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
R <sub>ON</sub> *	ON-resistance		T <sub>amb</sub> = 25°C V <sub>I(A, B)</sub> = 3.5V V <sub>DD</sub> = 14V I <sub>D(min)</sub> = 10mA		10	15	Ω
ΔR <sub>ON</sub>	ON-resistance Variation in any Package		T <sub>amb</sub> = 25°C V <sub>i</sub> = 3.5V V <sub>DD</sub> = 14V I <sub>D</sub> = 10mA			± 2	%
I <sub>DD</sub>	Supply Current					7	mA
I <sub>LI</sub>	Input Leakage	Pins 4, 5, 12, 13	V <sub>i</sub> = 5V			1	μA
		Pins 1, 9	V <sub>IA</sub> , V <sub>IB</sub> = 4.5V V <sub>O1</sub> , V <sub>O8</sub> = 1.5V			0.2	μA
			V <sub>IA</sub> , V <sub>IB</sub> = 6V V <sub>O1</sub> , V <sub>O8</sub> = 1.5V			1	μA
I <sub>LO</sub>	Output Leakage	Pins 2, 6, 7, 8, 10, 14, 15, 16	V <sub>O1</sub> , V <sub>O8</sub> = 4.5V V <sub>IA</sub> , V <sub>IB</sub> = 1.5V			0.2	μA
			V <sub>O1</sub> , V <sub>O8</sub> = 6V V <sub>IA</sub> , V <sub>IB</sub> = 1.5V			1	μA
V <sub>low</sub>	Logic 0 Input Level		All Inputs	− 0.3		0.8	V
V <sub>high</sub>	Logic 1 Input Level		All Inputs	4.5		V <sub>DD</sub>	V
CT	Cross-talk Attenuation		See fig. 4	90	95		dB
I <sub>O</sub>	Off Isolation		See fig. 5	90	95		dB
f <sub>CL</sub>	Maximum Clock Input Frequency		See fig. 6			1	MHz
T <sub>LG</sub>	Lag Time			100			ns
T <sub>LD1</sub>	Lead Time			400			ns
T <sub>LD2</sub>				150			
T <sub>WR</sub>	Write Time					3	μs
t <sub>w</sub>	Clock Pulse Width			0.4		100	μs

\* See figure 1 and 2 for  $R_{ON}$  variation with temperature and  $V_{BIAS}$ .

**Figure 1 :  $R_{ON}$  derating vs. temperature typ.**

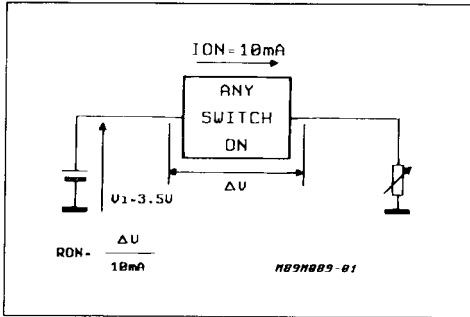


**Figure 2 :  $R_{ON}$  derating vs.  $V_{BIAS}$ .**

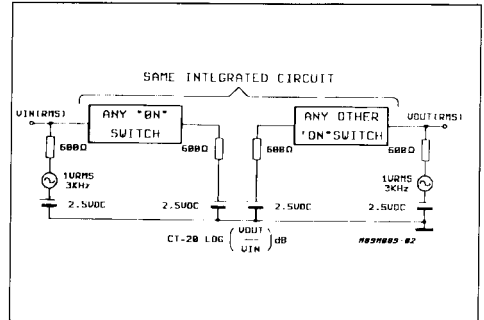


## TEST CIRCUITS

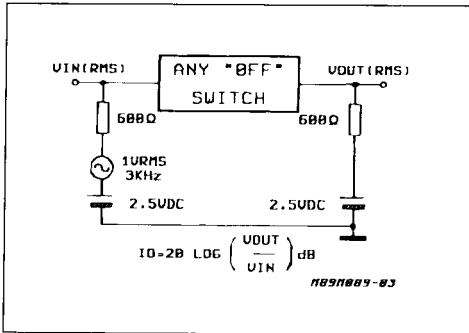
**Figure 3 :  $R_{ON}$  measurement.**



**Figure 4 : Crosstalk Measurements.**

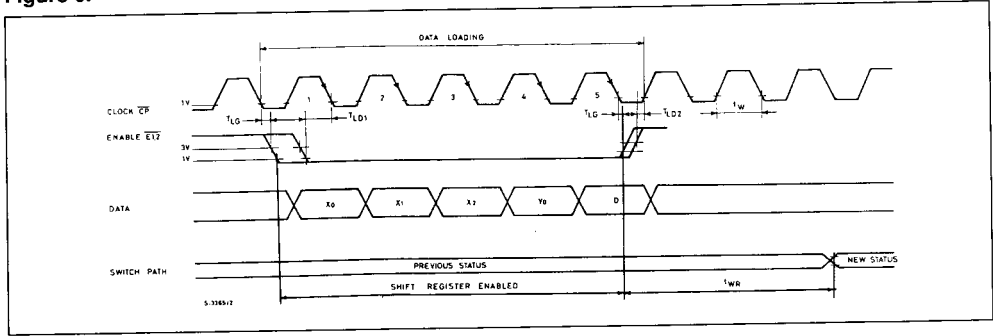


**Figure 5 : Off Isolation Measurement.**



TIMING DIAGRAM

Figure 6.

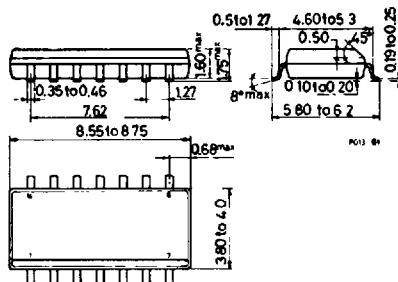
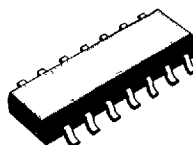
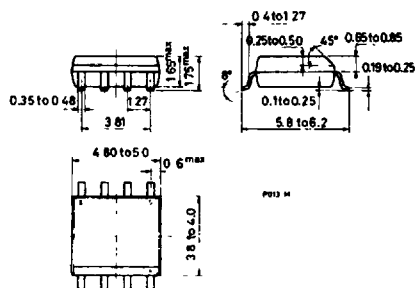
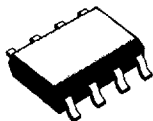


SO-8J

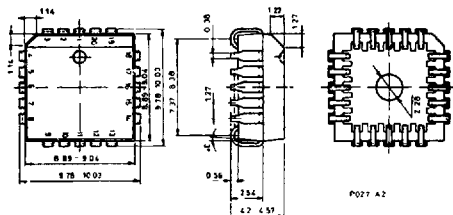
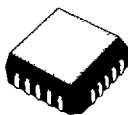
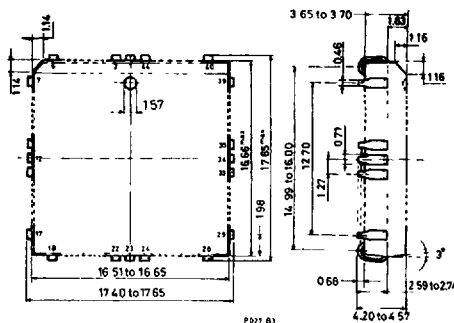
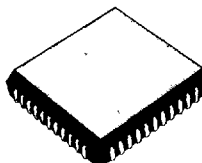
SO-14J

T-90-20

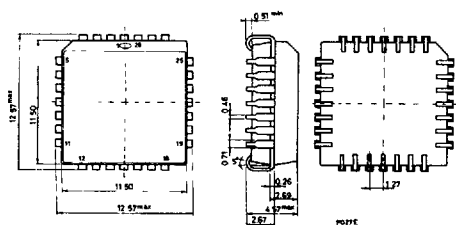
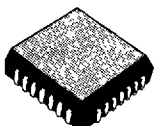
S G S-THOMSON



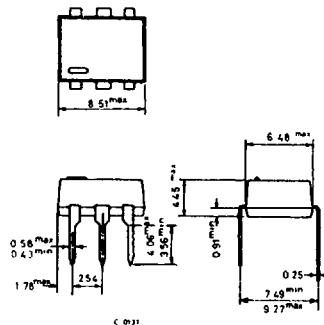
## PLCC20

**PLCC44**

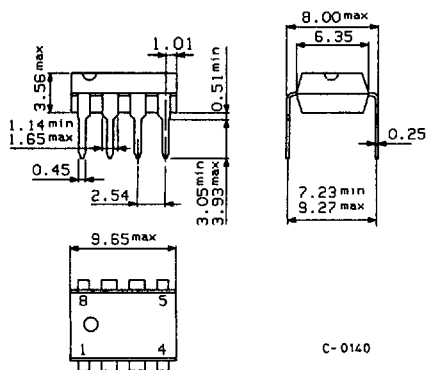
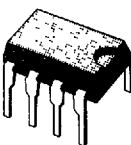
## PLCC-28 Plastic Chip Carrier



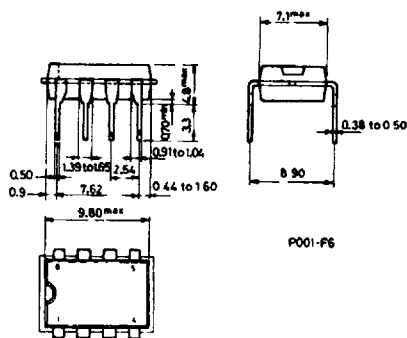
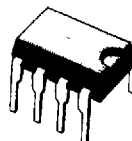
## DIP-6



## Minidip A Plastic



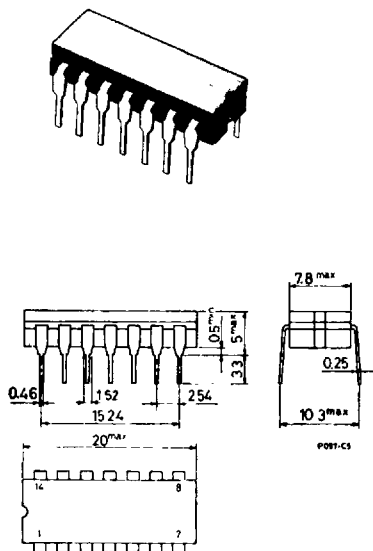
## 8 lead Plastic Minidip



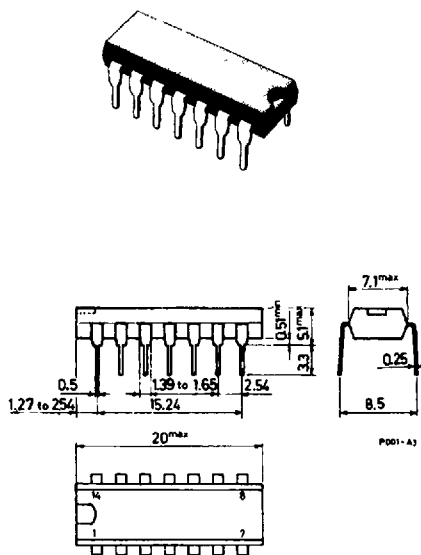


S G S-THOMSON

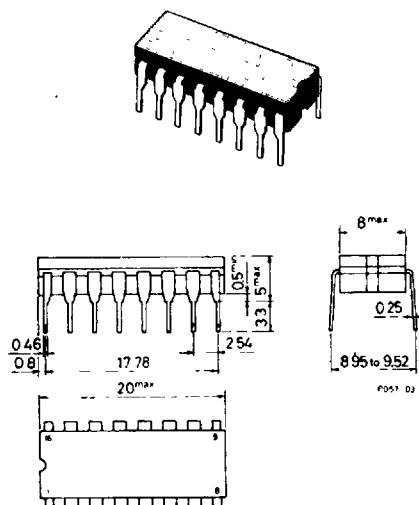
## 14 lead Ceramic Dip



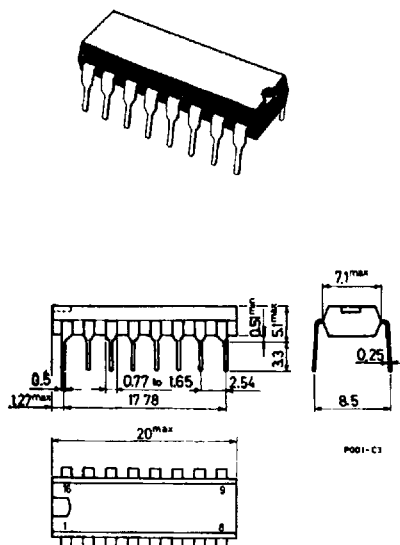
## 14 lead Plastic Dip



## 16 lead Ceramic Dip



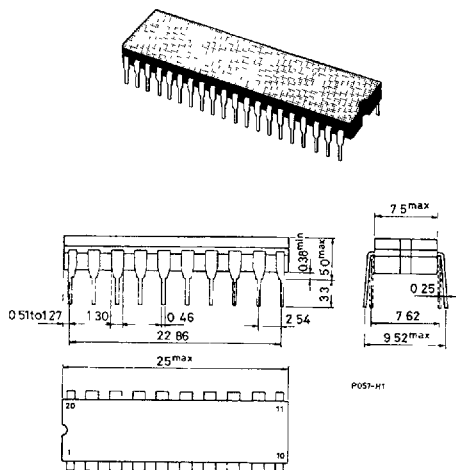
## 16 lead Plastic Dip (0.25)



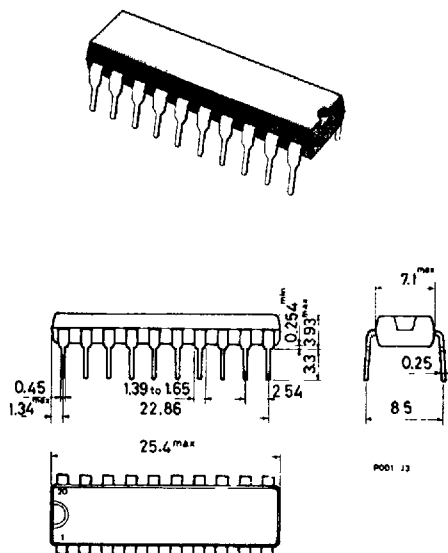
## PACKAGES

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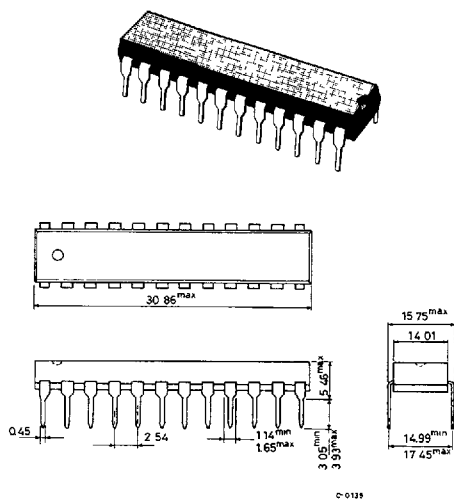
## DIP-20 Ceramic



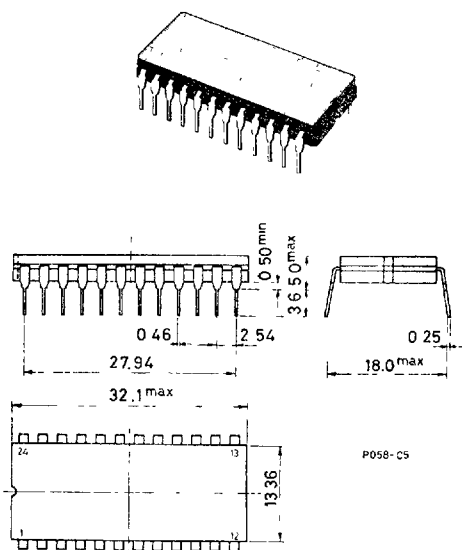
## 20 lead Plastic Dip (0.25)



## DIP-24 Plastic

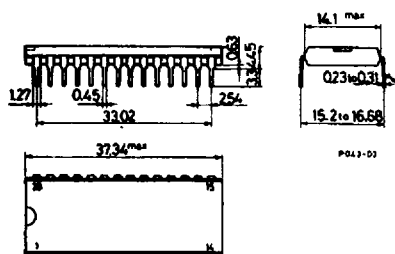
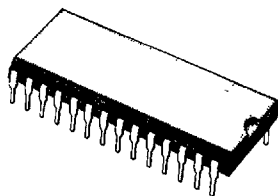


## DIP-24 Ceramic (0.25)

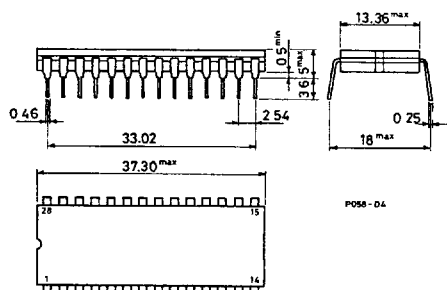
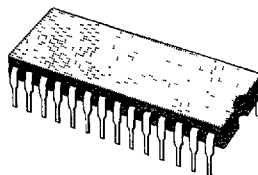


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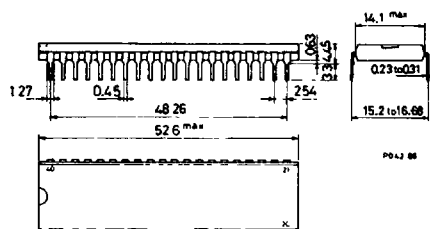
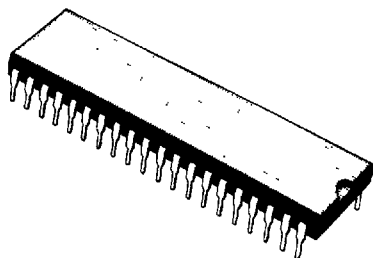
## 28 lead Plastic Dip



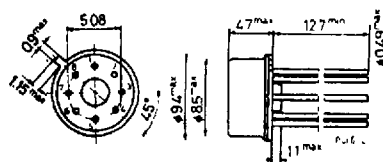
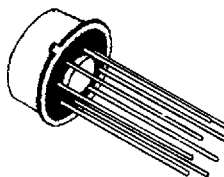
## DIP-28 Ceramic (0.25)



## 40 lead Plastic Dip



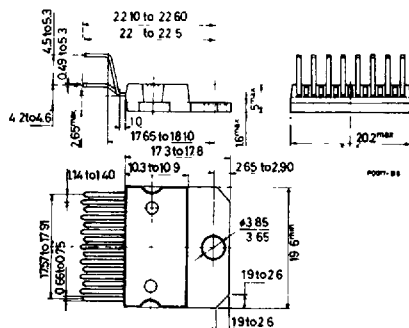
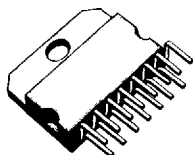
## TO-99



## PACKAGES

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## MULTIWATT-15



## FLEXIWATT-15

