IBM 1394 400Mb/s Physical Layer Transceiver (PHY)

Features

- Designed to provisions of the IEEE 1394 Serial Bus Standard [1]
- 400Mb/s max data rate; interoperable with 100 & 200Mb/s devices
- Available with one or three ports
- Supports major P1394a enhancements
  - Multi-speed Concatenation
  - Arbitrated Short Reset
  - ACK Accelerated Arbitration
  - Three TpBias Regulators
  - Connection Debounce
- "Missing SID bits" register
- "No reset on unplug" option
- Fully Compliant with OpenHCI requirements
  - Programmable Port Disable
  - No phy_ID wrap past 63
- Selectable Link-PHY interface timings
- Single 3.3V power supply
- Advanced Power Management:
  - Programmable Power Save Mode on unconnected ports
  - Sleep Mode to minimize quiescent power
  - Utilizes sophisticated clock gating to reduce power consumption
- Tolerant of extra IDLE indications which circumvents Link-PHY "Bus Collision" conditions
- On-device PLL generates the 50MHz SCLK using an external 25MHz crystal oscillator
- Supports optional 1394-1995 Isolation Barrier Feature at Link-PHY Interface
- Supports optional IBM Dynamic Termination Isolation Barrier Feature at Link-PHY Interface
- Interoperable with 5V Link Layer Controllers and 5V Transceivers
- Cable ports exceed 5kV of ESD protection (Human Body Model)

Overview

The IBM21S850 and IBM21S851 devices (PHYs) provide transceivers to implement a three or one port node in a 1394 cable based network. The PHY is designed to the provisions of the IEEE 1394-1995 specification [1] and includes many of the P1394a [2] and all OpenHCI enhancements. These enhancements include Arbitrated Short Reset (for uninterrupted Isochronous data transport), multi-speed concatenation, ACK Accelerated Arbitration (to improve bandwidth utilization), Connection Debounce Hysteresis (to avoid "Reset Storms"), three independent TpBias regulators (providing the ability to disable individual ports), and numerous other features.

Each cable port is composed of two differential line transceivers (TPA and TPB) that transmit and receive serial data at 100, 200, or 400Mb/s (actually 98.304, 196.608, and 393.216Mb/s, respectively), depending on which data speed is routed through the bus. Each transceiver contains a differential current mode driver whose outputs provide signal swings around a common mode voltage called TpBias, which is generated on the PHY device. Two off-device 55 ohm resistors are connected in series across the differential outputs of each transceiver. TpBias voltage is connected to the midpoint connection of the resistors at TPA, while a 5K ohm resistor and a 250pF capacitor to ground are attached to the midpoint connection of the resistors at TPB. The TpBias voltage for the TPB line is supplied by the TPA of the PHY at the other end of the cable.

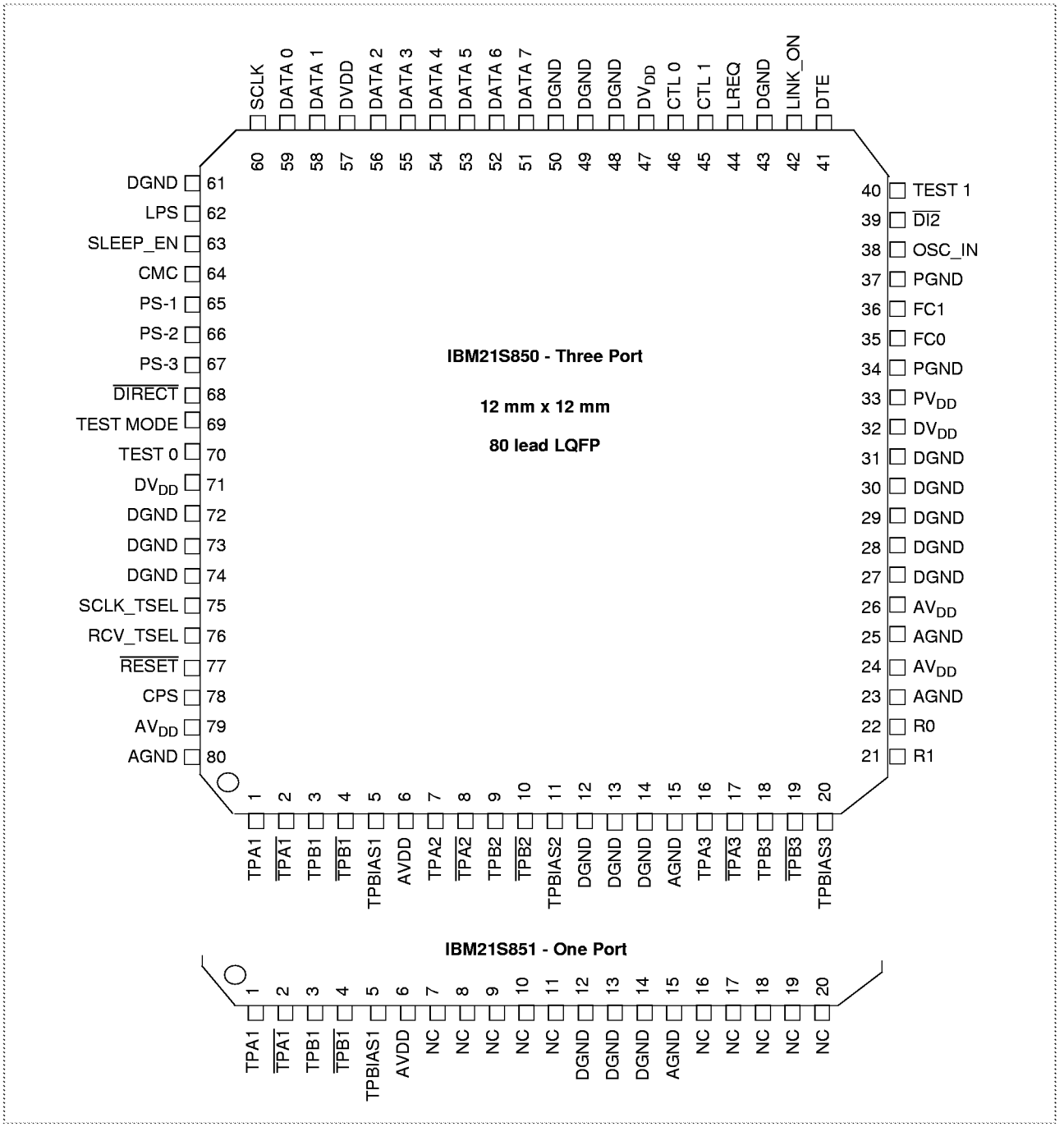
In addition to providing bus transceivers, the PHY serializes and deserializes data using Data and Strobe encoding. Data is sent from the Link Layer Controller on an eight bit wide parallel bus to the PHY. The two devices are synchronized by a 49.152MHz reference clock provided by the PHY. The data is then serialized and transmitted to the cable as Strobe on TPA and Data on TPB. Received data is resynchronized to the reference clock and decoded for parallel transmission to the Link Layer Controller.

PHY devices communicate their speed capabilities to one another through a process called Speed Signaling, in which common mode currents are withdrawn from the cable at TPB and $\overline{\text{TPB}}$. Three such common mode currents exist for this PHY: one for each of the supported transfer speeds. The nominal common mode currents are defined for 100Mb/s, 200Mb/s, and 400Mb/s as 0mA, -3.5mA, and -10mA respectively. The PHY is capable of 100, 200 or 400Mbits/sec operation, and will send or receive data at any of these speeds according to the capabilities of the adjacent PHYs.

Other functions of the PHY include system initialization and bus arbitration. The PHY also determines whether its ports are connected to other ports by detecting the presence or absence of TpBias volt-

age from the other transceiver. Moreover, it functions as a repeater to pass data along the bus.

Pinout



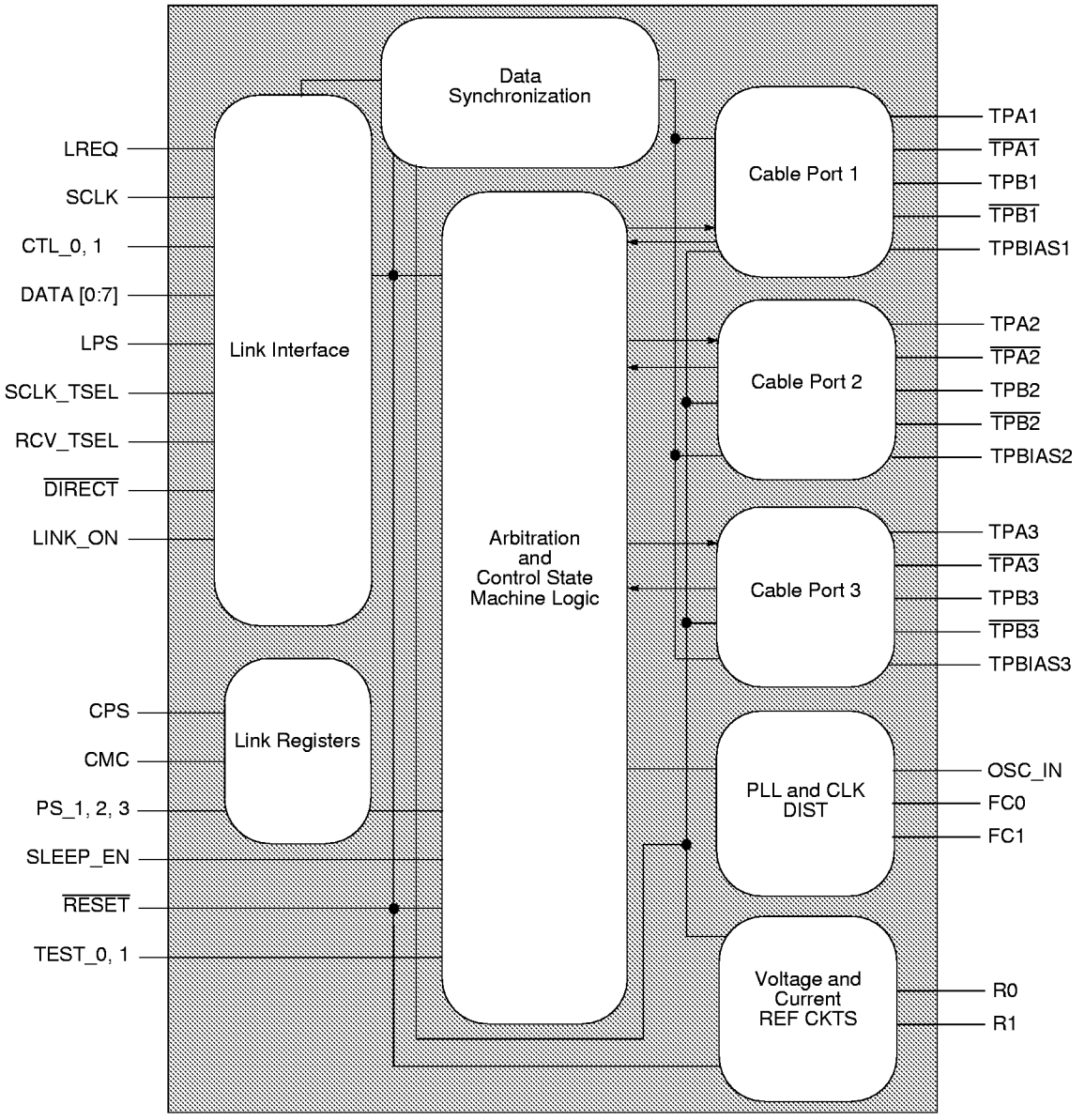
Ordering Information

Product Number	Number of Ports	Maximum Data Rate	Power Supply
IBM21S850	3	400Mb/s	3.3V

Ordering Information

Product Number	Number of Ports	Maximum Data Rate	Power Supply
IBM21S851	1	400Mb/s	3.3V

Block Diagram: Three-Port PHY



Note: ¯ represents an active low input or inverted output

Circuit Description

Phase Locked Loop

The system reference clocks are generated by a frequency synthesizing Phase Locked Loop. Using an external 24.576MHz crystal oscillator as a reference, the PLL generates a 49.152MHz system clock (SCLK) which is shipped to the Link Layer Controller to synchronize data transfer. The PLL also generates 98.304MHz, 196.608MHz and 393.216MHz clocks for data encode/decode. Several of the PLL loop filter components have been integrated onto the device, therefore only a single external capacitor is needed for the loop filter.

Bandgap Reference Generator

The band gap reference generator provides a precision voltage supply from which several voltage and current sources required by the PHY are derived. One of the most important of these is the 4mA current source which is used in the current mode serial bus driver to maintain constant current.

TpBias Circuits

TpBias is a constant voltage source that maintains the common mode voltage of the TPA cable twisted pair at 1.84V nominal for each port. This PHY contains three independent TpBias circuits (one per port). Each TpBias circuit can be disabled via software (Link Accessible Register 0xE), thereby implementing the port disable feature required by OpenHCI. In order to meet the speed signaling requirements, each port must be used in conjunction with a 0.3µF minimum ceramic capacitor. However, a 1.0µF ceramic capacitor is recommended at each port for added margin. The capacitor physical size is recommended to be the 1206 or 1210 form factor to reduce the parasitic inductance associated with the capacitor.

The external capacitor on TpBias provides phase compensation. It is required that the capacitor be added even at unused ports of the three port PHY.

Analog Transceivers

There are two 4mA differential current mode serial bus drivers per port. They are designed to operate with external 110 ohm line matching resistor networks located at each end of the twisted pair cable. Each driver can be placed in a Hi-Z state in which the drive current is shut off. The receivers are connected to the drivers in a Bi-Di configuration, and capture differential data and strobe signals at each port.

The arbitration comparators are connected across the driver outputs, similar to the receivers. They detect logical DC levels used during bus arbitration. Two comparators are required per driver output, one to detect a logical “1” and one for a logical “0”. A logical “Z” state is also used in arbitration. It is considered to be the midpoint logical state in which both comparators are inactive.

The speed signaling comparator senses the common mode voltage at driver TPA and compares it with the TpBias reference, in order to detect whether any common mode controlled current signaling has been sent from the other end of the cable. The current pulses are used to signal the speed capability of the port at the other end.

The port status comparator senses the common mode voltage at driver TPB and compares it with a reference voltage, in order to detect whether TpBias voltage is being supplied by the port at the other end. It is used to determine whether or not the port is connected.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Supply voltage range	-0.3 to 5.1	V	1
V_{IN}	Logic input voltage range	-0.5 to 5.5	V	1
V_{OUT}	Logic output voltage range	-0.5 to 5.5	V	1
V_T	Test I/O voltage range	-0.5 to 3.6	V	1
V_C	Cable transceiver voltage range	-0.5 to 3.6	V	1
T_{OPR}	Operating Temperature	0 to 70	°C	1, 2
T_{STG}	Storage Temperature	-65 to +150	°C	1

1. The device is not guaranteed to function at these limits, and exceeding the limits may damage the device.
2. See the Supply Current and Dissipation Rating tables on page 7.

Operating Conditions and Electrical Characteristics

The current polarity convention used in these tables is that current *into* a transceiver input is considered positive, while a current *out of* a transceiver output is considered positive.

Symbol	Parameter	Pin	Min	Typ	Max	Units	Notes
V_{DD}	Supply Voltage		3.0	3.3	3.6	V	
V_{OH}	High Level Output Voltage	CMOS outputs	V_{DD} - 0.5			V	
V_{OL}	Low Level Output Voltage	CMOS outputs			0.5	V	
V_{IH}	High Level Input Voltage	CMOS inputs	0.8 V_{DD}			V	
V_{IL}	Low Level Input Voltage	CMOS inputs			0.2 V_{DD}	V	
V_{ID}	Differential Input Voltage	Cable inputs	>90		265	mV	
V_{IC}	Common Mode input Voltage	TPB, $\overline{TPB}$	1.165		2.515	V	
		TPA, $\overline{TPA}$	1.665		2.015	V	
V_{IT}+	Positive input threshold Voltage, V_{IT} +	Hysteresis	$V_{DD}/2$ + 0.1		$V_{DD}/2$ + 0.8	V	
		$\overline{RESET}$	$V_{DD}/2$ + 0.2		$V_{DD}/2$ + 0.8	V	
V_{IT}-	Negative input threshold Voltage, V_{IT} -	Hysteresis	$V_{DD}/2$ - 0.9		$V_{DD}/2$ - 0.3	V	
		$\overline{RESET}$	$V_{DD}/2$ - 0.9		$V_{DD}/2$ - 0.3	V	
I_{IL}	Dynamic Termination Latch input Current @ V_{IL} = 0.66V	LREQ, CTL, DATA	0.1		1.2	mA	
I_{IH}	Dynamic Termination Latch input Current @ V_{IH} = 2.64V	LREQ, CTL, DATA	-1.2		-0.1	mA	
V_{OD}	Differential output voltage	Cable output	172	220	265	mV	
V_O	Common mode output voltage	TPBIAS	1.665	1.82	2.015	V	
I_{SP100}	S100 common mode output current (signaling off)	TPB, $\overline{TPB}$	-0.81		0.44	mA	
I_{SP200}	S200 common mode output current (signaling on)	TPB, $\overline{TPB}$	-4.84	-3.5	-2.53	mA	
I_{SP400}	S400 common mode output current (signaling on)	TPB, $\overline{TPB}$	-12.40	-10.00	-8.10	mA	
I_{OL}	Output current @ 0.4V	SCLK	-12			mA	
I_{OH}	Output current @ 2.4V	SCLK			16	mA	
I_{OL}	Output current @ 0.4V	CTL, DATA	-12			mA	
I_{OH}	Output current @ 2.4V	CTL, DATA			16.0	mA	
I_O	Output current IO	TPBIAS1, TPBIAS2, TPBIAS3	-2.0		10.0	mA	
T_{OPR}	Free Air Temperature		0		70	°C	1
P_D	Power dissipation			1.0	1.30	W	1

1. See the Supply Current and Dissipation Rating tables on page 7.

Supply Current

Test Condition	Product	Supply Voltage (V)	Typ	Max	Units
Rcv on 1 port, Tx on 2 ports, 400Mb/s	IBM21S850	3.3	262		mA
		3.6		360	
Transmitting or receiving	IBM21S851	3.3	150		
		3.6		190	
PHY Asleep		3.3	30		mA

Dissipation Rating

Package	$T_A \leq 25°C$	Derating Factor Above 25°C	T_A=70°C	Notes
LQFP-80	2071mW	23.8 mW/°C	1000 mW	1

1. Junction to free air thermal resistance = 42°C/W

Thermal Characteristics

Symbol	Parameter	Test Condition	Max
$R_{\Theta JA}$	Junction to free air thermal resistance	Board mounted, natural convection	42°C/W

Data Signal Characteristics

Symbol	Parameter		Min	Typ	Max	Units
T_R	Output rise time		0.5	0.8	1.2	ns
T_F	Output fall time		0.5	0.8	1.2	ns
	Input slope		175			mV/ns
	Transmitter skew				0.10	ns
	Transmitter jitter				0.15	ns
	Skew at receive pins	Receiving 100Mb/s			0.80	ns
		Receiving 200Mb/s			0.55	ns
		Receiving 400Mb/s			0.50	ns
	Jitter at receiving pins	Receiving 100Mb/s			8.50	ns
		Receiving 200Mb/s			3.50	ns
		Receiving 400Mb/s			0.315	ns

I/O Pin Function (Part 1 of 3)

Pin Name	Function	Pin Number	Pin Type	I/O Type	Notes
TPA1	Port 1, Twisted pair A, positive signal	1	Differential	I/O	
$\overline{\text{TPA1}}$	Port 1, Twisted pair A, negative signal	2	Differential	I/O	
TPB1	Port 1, Twisted pair B, positive signal	3	Differential	I/O	
$\overline{\text{TPB1}}$	Port 1, Twisted pair B, negative signal	4	Differential	I/O	
TPBIAS1	Bias voltage supply. Provides 1.84V nominal bias voltage for Port 1 twisted pair signal cables. Indicates a valid cable connection to remote nodes. This supply can be individually disabled via software when not needed.	5	Supply	Output	
AV_{DD}	Analog circuit power (3.3V nom). These pins are separated from other power pins internal to the device to provide noise isolation. Decoupling capacitor networks are recommended at each pin. All the power supply pins should be tied together at a low impedance point on the circuit board.	6, 24, 26, 79	Supply	-	
TPA2	Port 2, Twisted pair A, positive signal	7	Differential	I/O	1
$\overline{\text{TPA2}}$	Port 2, Twisted pair A, negative signal	8	Differential	I/O	1
TPB2	Port 2, Twisted pair B, positive signal	9	Differential	I/O	1
$\overline{\text{TPB2}}$	Port 2, Twisted pair B, negative signal	10	Differential	I/O	1
TPBIAS2	Bias voltage supply. Provides 1.84V nominal bias voltage for Port 2 twisted pair signal cables. Indicates a valid cable connection to remote nodes. This supply can be individually disabled via software when not needed.	11	Supply	Output	1
DGND	Digital circuit ground. These pins are separated from other ground pins internal to the device to provide noise isolation. All ground pins should be tied together at a low impedance point on the circuit board.	12, 13, 14, 27, 28, 29, 30, 31, 43, 48, 49, 50, 61, 72, 73, 74	Supply	-	
AGND	Analog circuit ground. These pins are separated from other ground pins internal to the device to provide noise isolation. All ground pins should be tied together at a low impedance point on the circuit board.	15, 23, 25, 80	Supply	-	
TPA3	Port 3, Twisted pair A, positive signal	16	Differential	I/O	1
$\overline{\text{TPA3}}$	Port 3, Twisted pair A, negative signal	17	Differential	I/O	1
TPB3	Port 3, Twisted pair B, positive signal	18	Differential	I/O	1
$\overline{\text{TPB3}}$	Port 3, Twisted pair B, negative signal	19	Differential	I/O	1
TPBIAS3	Bias voltage supply. Provides 1.84V nominal bias voltage for Port 3 twisted pair signal cables. Indicates a valid cable connection to remote nodes. This supply can be individually disabled via software when not needed.	20	Supply	Output	1
R1, R0	3.6 Kohm (±0.5%) external current setting resistor terminals	21, 22	Analog	Output	
DV_{DD}	Digital circuit power (3.3V nom). These pins are separated from other power pins internal to the device to provide noise isolation. Decoupling capacitor networks are recommended at each pin. All the power supply pins should be tied together at a low impedance point on the circuit board.	32, 47, 57, 71	Supply	-	

1. These ports exist on the three-port PHY only. These pins are NC on the one port PHY.
2. See Operating Conditions and Electrical Characteristics on page 6 for electrical characteristics.

I/O Pin Function (Part 2 of 3)

Pin Name	Function	Pin Number	Pin Type	I/O Type	Notes
PV_{DD}	PLL analog circuit power (3.3V nom). These pins are separated from other power pins internal to the device to provide noise isolation. Decoupling capacitor networks are recommended at each pin. All the power supply pins should be tied together at a low impedance point on the circuit board.	33	Supply	-	
PGND	PLL analog circuit ground. These pins are separated from other ground pins internal to the device to provide noise isolation. All ground pins should be tied together at a low impedance point on the circuit board.	34, 37	Supply	-	
FC0, FC1	0.1µF Cap (±10%) external PLL filter capacitor terminals	35, 36	Analog	Output	
OSC_IN	Crystal Oscillator @ 24.576MHz (±100 ppm), 3.3V. External oscillator provides stable reference frequency without sensitivity to board parasitics, and without the need for tank circuit components.	38	CMOS	Input	
$\overline{DI2}$	Driver Inhibit 2 test pin only. 1 = normal operation.	39	CMOS	Input	
TEST_1, 0	Reserved for test only. 0 = normal operation.	40, 70	CMOS	Input	
DTE	Dynamic termination enable pin. Used for Link-PHY interface isolation in instances where the Link uses bus holder circuitry. 1 = enable.	41	CMOS	Input	
LINK_ON	A 6MHz signal is transmitted from this pin when a Link Power On packet is addressed to the device's PHY ID and the LPS pin = 0.	42	CMOS	Output	
LREQ	Link request from controller for the PHY to perform some service.	44	Hysteresis	I/O	2
CTL_1, 0	Link interface bidirectional control pins.	45, 46	Hysteresis	I/O	2
DATA [0:7]	Link interface bidirectional data pins.	59, 58, 56, 55, 54, 53, 52, 51	Hysteresis	I/O	2
SCLK	49.152MHz system clock to Link controller.	60	CMOS	Output	
SLEEP_EN	Sleep enable pin. '1' tells the PHY to power down if none of its ports are in use.	63	CMOS	Input	
CMC	Bus Configuration Manager Contender. "1" causes the PHY to indicate in the self-ID packet that the node is capable of being the Bus Manager.	64	CMOS	Input	
LPS	Link power status. This pin monitors the Link power status by receiving either the Link V_{CC} or nominally a 1MHz signal indicating that the Link is powered. If this input is low for more than 1.3µS, then the Link is considered powered down. If the input is high for more than 20nS, then the Link is considered powered up. If the Link is not powered, then the Link-PHY interface is disabled, and the PHY performs basic repeater functions.	62	Hysteresis	Input	2
PS_1, 2, 3	Power Status pins. These inputs are used to set the three POWER_CLASS bits in the self-ID packet. They are used to describe the power consumption and source characteristics of the node, and are programmed by tying the pins high or low. PS_1, 2, & 3 are reflected in the self_id bits 21, 22, & 23, respectively.	65, 66, 67	CMOS	Input	

1. These ports exist on the three-port PHY only. These pins are NC on the one port PHY.
2. See Operating Conditions and Electrical Characteristics on page 6 for electrical characteristics.

I/O Pin Function (Part 3 of 3)

Pin Name	Function	Pin Number	Pin Type	I/O Type	Notes
$\overline{\text{DIRECT}}$	Indicates presence of an Isolation Barrier using differentiated signals between the Link & PHY. 0 (GND) = direct coupling 1 (V_{DD}) = isolation with differentiated signals	68	CMOS	Input	
TEST_ MODE	Reserved for test. For normal operation, connect to '0' (GND).	69	CMOS	Input	
SCLK_TSEL	Select SCLK setting. 0 = default SCLK timings. 1 = alternate timings. See Link-PHY Interface Timing on page 16.	75	CMOS	Input	
RCV_TSEL	Select receive timing. This pin enables the selection of alternate timings between data received from the Link and the system clock. 0 = default timings. 1 = alternate timings. See Link-PHY Interface Timing on page 16.	76	CMOS	Input	
$\overline{\text{RESET}}$	Reset (active low). The reset pin is connected to an internal 10K ohm resistor and an external 2.2µF capacitor to allow time for voltage buildup at power-on. 1 = normal operation of the PHY.	77	Custom	Input	2
CPS	Cable power status. This pin is connected to the cable power through a 400 K ohm resistor. When cable power is detected, the information is kept in an internal register which the Link can access through a register read. A diode is required between the module pin and the PHY V_{DD} to clamp the input voltage.	78	Hysteresis	Input	2

1. These ports exist on the three-port PHY only. These pins are NC on the one port PHY.
2. See Operating Conditions and Electrical Characteristics on page 6 for electrical characteristics.

Device Power Supply

The PHY device uses a single 3.3V system power supply which can be sourced on the card or externally. The 3.3V system supply powers the Digital, Analog and PV_{DD} inputs. There may exist a need to electrically isolate the Digital, Analog and PV_{DD} (the portion of the Analog supply feeding the Phase Locked Loop) inputs using either a ferrite bead and/or decoupling capacitor configuration. The three power supplies (V_{DD}/GND, AV_{DD}/AGND, PV_{DD}/PGND) are separate within the PHY to allow for this electrical isolation on the card. The GND, AGND, and PGND are connected via the die substrate. See I/O Pin Function on page 8 or External Component Connections on page 39 for the locations of the power supply pins.

Establishing the Link-PHY Interface

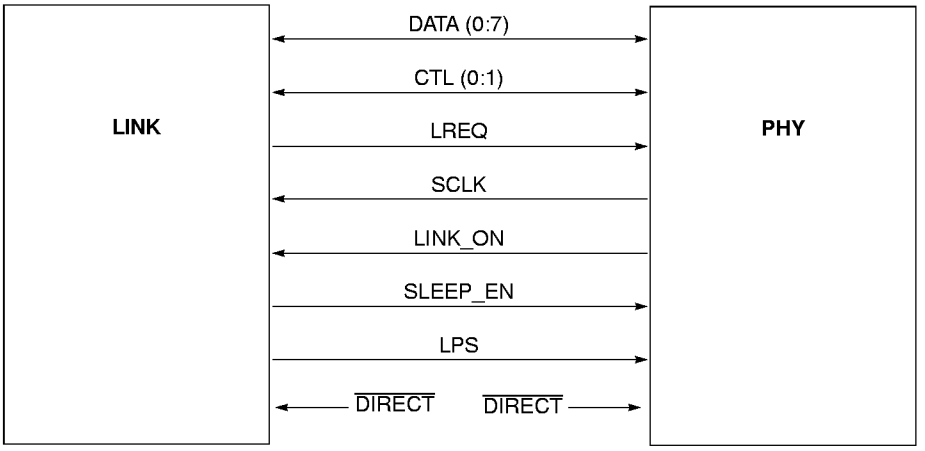
Overview

The Link-PHY interface is a scalable, cost effective method for connecting one 1394 Link device to one 1394 PHY device. The characteristics of this interface are described in the diagram below and in the Link-PHY Interface Pin Description on page 11. The PHY device has control of the bidirectional pins. The Link only drives these pins when control is transferred to it by the PHY.

Data is transmitted between the two devices on the data bus. The data bus between the PHY and the Link device is clocked at the same rate for all supported speeds; however, the data rate is increased by widening the bus. The PHY uses two bits for 100Mb/s transfers, four bits for 200Mb/s, and eight bits for 400Mb/s. The control bus carries control information and is always two bits wide. The LREQ pin is used by the Link to request access to the serial bus and to read or write PHY registers. The $\overline{\text{DIRECT}}$ pin is used to disable the digital differentiator on the DATA and CTL pins, indicating that the two devices are connected directly, rather than through an isolation barrier requiring differentiating signals.

Specific guidelines for routing particular signals are given in Board Layout Recommendations on page 41.

Link-PHY Interface Diagram



Link-PHY Interface Pin Description

Pin	Driven By	Description
DATA(0:7)	Link & PHY (tri-state)	Data
CTL(0:1)	Link & PHY (tri-state)	Control
LREQ	Link	Link Request
SCLK	PHY	49.152MHz (sync to serial bus) clock
LINK_ON	PHY	Drives 6MHz signal to wake up Link when Link Power On packet is received and LPS = 0
SLEEP_EN	Link	Tells PHY to power down if none of its ports are in use
LPS	Link	Link Power Status
$\overline{\text{DIRECT}}$	neither	Controls differentiator for interface pins

Link-PHY Electrical Isolation

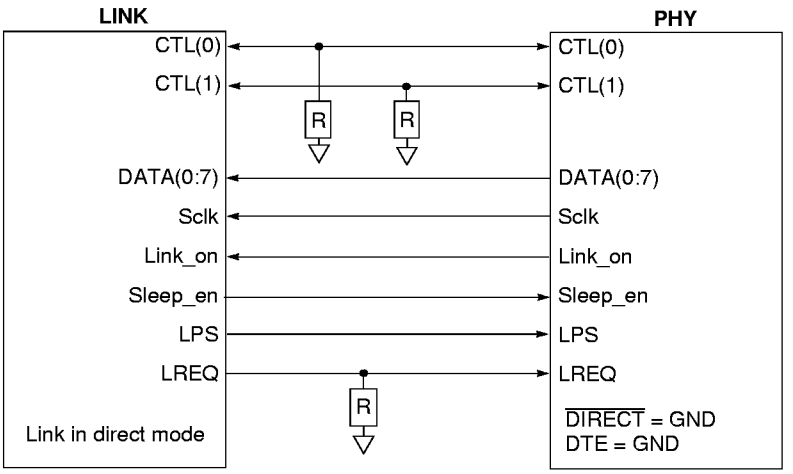
The need to isolate the Link from the PHY electrically may arise when a difference in potential exists between their respective grounds (GND_L and GND_P). The particular device connected to the Link (CPU, disk drive, etc.) may also require isolation. Electrical isolation may also be implemented when the Link is disconnected and the cable becomes the PHY's source of power.

The PHY supports three types of connections between the Link and PHY: Direct, Capacitive, and IBM's Dynamic Termination for isolation between the IBM's PCI Link and PHY.

Direct Connection Between Link and PHY

1. LREQ should have a pull down resistor (3.3Kohm recommended) if the PHY can be powered while the Link is powered down.
2. Each control line should have a pull down resistor if it is possible for the PHY to be in power-on-reset longer than the Link (less than 30mS with a 2.2µF cap on $\overline{RESET}$) or if the preferred timing mode causes the control lines to float for a portion of a cycle in which noise may create problems for the Link. This is not a concern for the PHY.
3. LPS may be tied directly to the Link's V_{DD} if the Link does not support LPS.
4. Sleep_en may be tied directly to V_{DD} or GND to control the sleep function if the Link is unable to control this function.
5. If Link_on cannot be connected to the Link or Link support circuitry, it must be floated. This pin cannot be connected directly to ground.
6. The PHY supports communication with 3 or 5 volt Links.

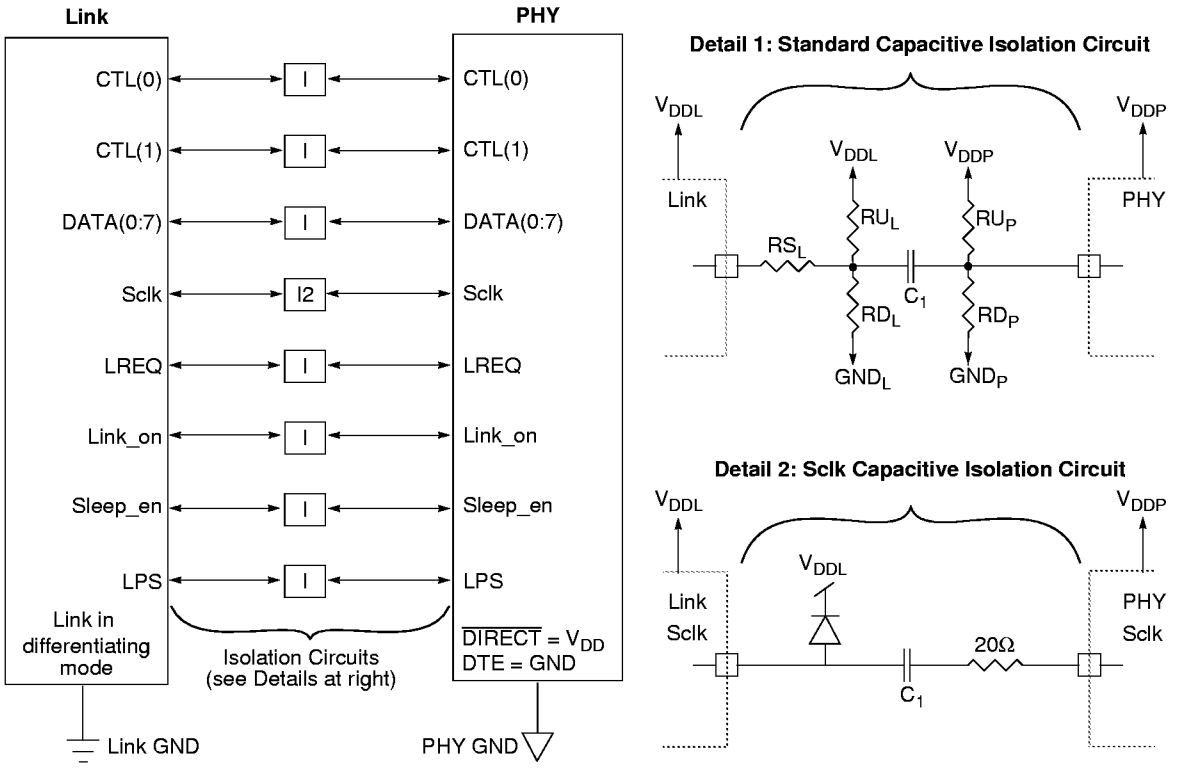
Direct Connection Diagram



Capacitive Isolation with Differentiated Signals

The diagram below shows electrical isolation between the Link and the PHY using cost efficient capacitive isolation barrier circuits. Each circuit provides isolation for one Link-PHY connection and handles a ground potential difference between the Link and the PHY based upon the voltage rating of the capacitor. See Component Values for Capacitive Isolation Barrier Circuit on page 14 for the specific component values based upon the Link V_{DD} supply (3.3V or 5V). Set the $\overline{DIRECT}$ pin high for this operation.

Capacitive Isolation Barrier



Notes:

1. "I" represents the isolation circuit illustrated in Detail 1 and specified in Component Values for Capacitive Isolation Barrier Circuit on page 14. The isolation network can be reduced for most unidirectional signals (Link_on, Sleep_en, and LPS) by removing the resistors on the transmit side of the network.
2. "I2" represents the isolation circuit illustrated in Detail 2 and specified in Component Values for Capacitive Isolation Barrier Circuit on page 14.
3. Isolation networks are not needed for Link_on, Sleep_en, and LPS if the pin is not utilized by the Link or Host and are connected as described below.
4. LPS can NOT be tied directly to V_{DD} of the PHY if the Link does not support LPS. LPS must be connected though a resistor (3.3K ohm recommended) if it is to be connected to a power source or GND.
5. Sleep_en may be tied directly to V_{DD} or GND to control the sleep function if the Link is unable to do so.
6. Link_on must be connected to a 3.3K ohm resistor to GND or floated if it is not utilized. This pin cannot be connected directly to ground.

Component Values for Capacitive Isolation Barrier Circuit

Component	V_{DDP} = 3.3V and V_{DDL} = 3.3V	V_{DDP} = 3.3V and V_{DDL} = 5.0V
C_I	1.0 nF	1.0 nF
RS_L	Shorted	160 Ohm
RU_L	5.0 KOhm	750 Ohm
RD_L	5.0 KOhm	750 Ohm
RD_P	5.0 KOhm	5.0 KOhm
RU_P	5.0 KOhm	5.0 KOhm
D_I	general purpose high-speed switching diode	general purpose high-speed switching diode
The voltage rating of the capacitor is dependent on the level of isolation required.		

Isolation Using IBM's Dynamic Termination

The Link and the PHY can be isolated using IBM's Dynamic Termination circuitry, provided that the power supply voltages of each are at the same nominal value. Isolation is achieved by using a 1.0nF capacitor, the PHY Dynamic Termination, and a Link bus latch, as shown below. For correct operation with isolation, this circuitry must be applied to each of the DATA, CTL, and LINK_ON pins. LREQ, SLEEP_EN, LPS, and SCLK only need capacitors.

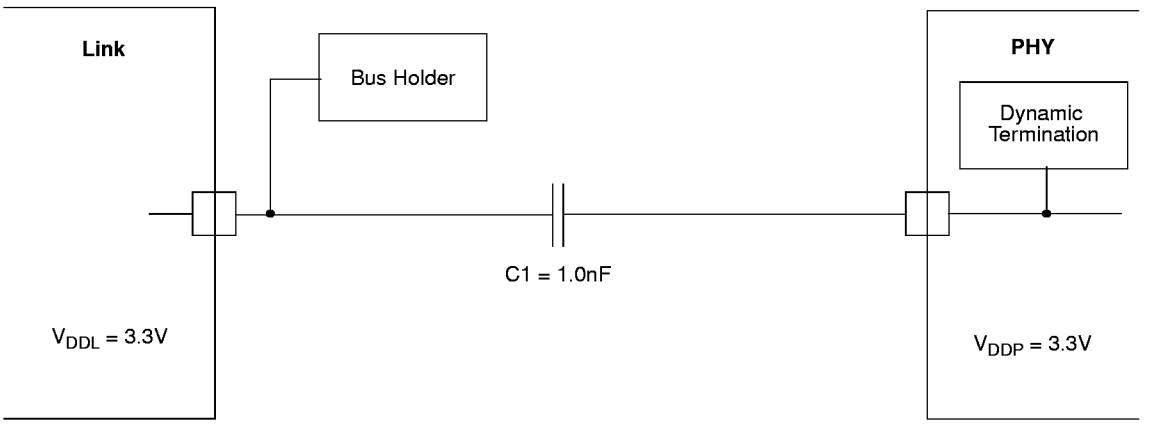
The Link bus latch, which may be either built into the Link or external to it, holds received signals from the PHY at either an UP level or a DOWN level after they pass through the capacitor. Similarly, data pulses transmitted from the Link are held at their UP or DOWN levels by the Dynamic Termination of the PHY, which is enabled by tying the DTE pin high and the $\overline{\text{DIRECT}}$ pin low.

The PHY Dynamic Termination pins are automatically initialized at a DOWN level at power-on-reset. To assure proper data transmission, the Link must also be initialized at a DOWN level at power-on-reset.

Timing is not affected by the Dynamic Termination, so the timing values given in Link-PHY Interface Timing on page 16 are valid.

The Link and PHY ground planes must be connected to each other by at least one trio of 0.001μF, 0.01μF and 0.1μF coupling capacitors to provide an AC return path. The trio should be repeated as often as is feasible, equally distributed along the mutual borders of the ground planes, with a maximum spacing of about 1" between each capacitor and between each trio.

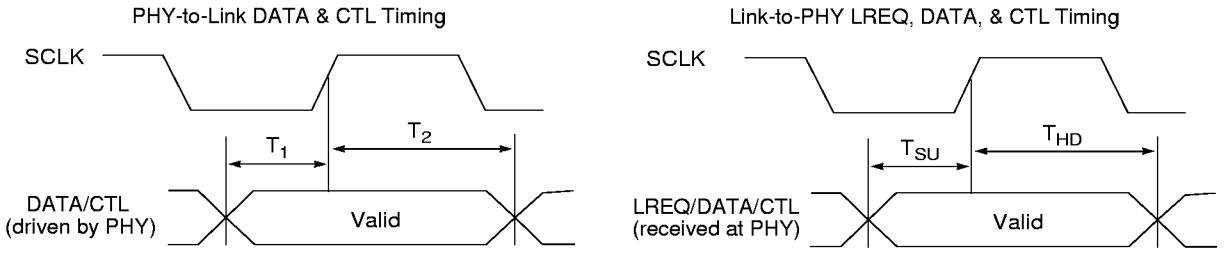
Dynamic Termination Diagram



Link-PHY Interface Timing

The IBM PHY features selectable SCLK timing that can be tailored to the needs of the Link device. The SCLK timing is controlled by the SCLK_TSEL pin. When tied low, the SCLK has normal mode timing, and when tied high, the SCLK has early mode timing. In addition, the timing of data received from the Link can be adjusted using the RCV_TSEL pin.

Link-PHY Interface Timing Relationships



Normal Mode Timing

Symbol	Parameter	Min	Units
T_1	Time DATA/CTL valid before rising SCLK edge (PHY sending)	16.0	ns
T_2	Time DATA/CTL valid after rising SCLK edge (PHY sending)	0.0	ns
T_{SU}	Setup time LREQ, DATA, CTL before rising SCLK edge (PHY receiving)	6.0	ns
T_{HD}	Hold time LREQ, DATA, CTL after rising SCLK edge (PHY receiving)	0.0	ns

Timing calculated with C_L = 10 pF
Module pin settings: SCLK_TSEL = 'GND', RCV_TSEL = 'GND'.

Early Mode SCLK Timing

Symbol	Parameter	Min	Units
T_1	Time DATA/CTL valid before rising SCLK edge (PHY sending)	8.0	ns
T_2	Time DATA/CTL valid after rising SCLK edge (PHY sending)	8.0	ns
T_{SU}	Setup time LREQ, DATA, CTL before rising SCLK edge (PHY receiving)	-2.0	ns
T_{HD}	Hold time LREQ, DATA, CTL after rising SCLK edge (PHY receiving)	9.5	ns

Timing calculated with C_L = 10 pF
Module pin settings: SCLK_TSEL = 'V_{DD}', RCV_TSEL = 'GND'.

RCV Delayed Timing

Symbol	Parameter	Min	Units
T_1	Time DATA/CTL valid before rising SCLK edge (PHY sending)	16.0	ns
T_2	Time DATA/CTL valid after rising SCLK edge (PHY sending)	0.0	ns
T_{SU}	Setup time LREQ, DATA, CTL before rising SCLK edge (PHY receiving)	12.5	ns
T_{HD}	Hold time LREQ, DATA, CTL after rising SCLK edge (PHY receiving)	-2.5	ns
Timing calculated with C_L = 10 pF Module pin settings: SCLK_TSEL = 'GND', RCV_TSEL = 'V_{DD}'.			

Early Mode RCV Delayed Timing

Symbol	Parameter	Min	Units
T_1	Time DATA/CTL valid before rising SCLK edge (PHY sending)	8.0	ns
T_2	Time DATA/CTL valid after rising SCLK edge (PHY sending)	8.0	ns
T_{SU}	Setup time LREQ, DATA, CTL before rising SCLK edge (PHY receiving)	4.5	ns
T_{HD}	Hold time LREQ, DATA, CTL after rising SCLK edge (PHY receiving)	7.5	ns
Timing calculated with C_L = 10 pF Module pin settings: SCLK_TSEL = 'V_{DD}', RCV_TSEL = 'V_{DD}'.			

Link-PHY Diagnostics

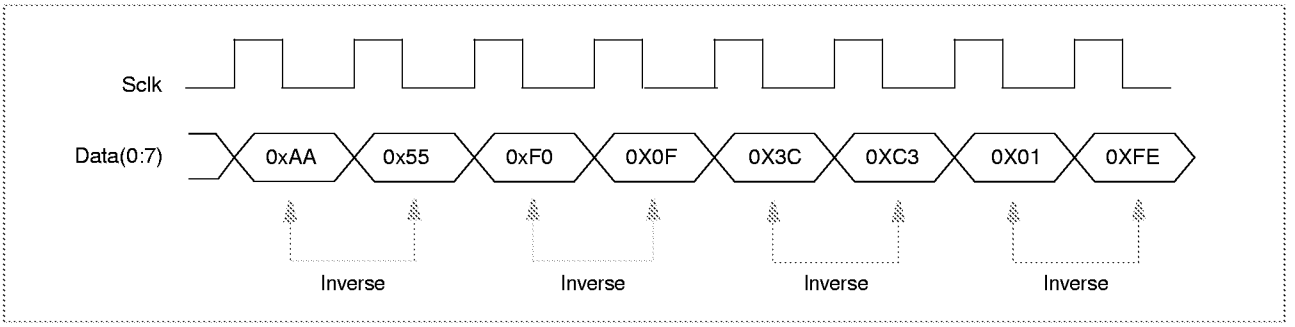
The IBM21S851 and IBM21S850 offer the ability to test the Link-PHY interface using available Link-PHY protocol, a beneficial feature for hardware testing and field diagnostic software. When utilizing this feature outside a controlled environment, all ports should be disabled via PHY register 0xE.

The Link-PHY interface can be tested in both directions: Link-to-PHY and PHY-to-Link. The following tests the interface from the Link to the PHY.

The Link-PHY interface self test is enabled by writing a logic '1' to bit 1 of PHY register 0xD.

At this point, the link issues either a fair, priority, or isochronous bus request via the LREQ to transmit a 400Mb/s packet. When the PHY grants the bus to the Link, the Link must respond by sending a packet of any length (IEEE-1394 packet length rules do not apply) to the PHY. The data must be in groups of two bytes in which the second byte is the logical inverse of the previous byte. For example, the 400Mb/s packet may be as follows:

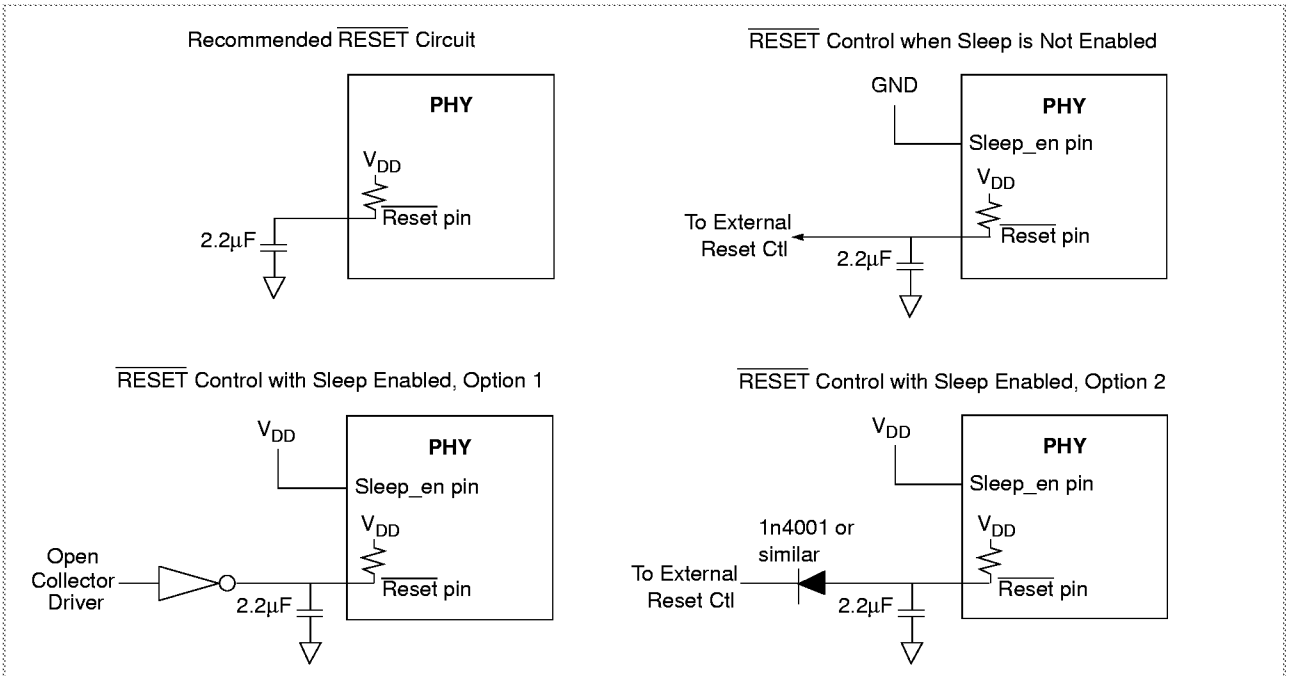
400Mb/s Diagnostic Packet Example



The Link may use normal protocol (i.e. issue a "Hold" prior to Transmit). The data integrity is confirmed by the PHY inverse checking of the packet. The PHY indicates an inverse error by setting the Link-PHY Error Ever Happened bit. To confirm data transmission from the PHY to the Link, the Link needs to set the Send Phy/Link Diag Pkt bit in PHY register 0xF. The PHY responds by sending its self_ID packet to the Link as a 400Mb/s packet, at which time the Link and/or software may check that the last 32 bits are the inverse of the first 32 bits. The Phy/Link Diag Pkt bit is cleared after the transmission of the 400Mb/s self_ID packet.

Configuring Hardware Alternatives

$\overline{\text{RESET}}$ Circuit Design



It is important that the following information be considered if the $\overline{\text{RESET}}$ pin is to be controlled by something other than the recommended RC circuit shown above.

If the PHY is allowed to sleep, one of the two circuits shown in the RESET Control with Sleep Enabled diagrams is required for use in applications where the $\overline{\text{RESET}}$ pin is controlled by something other than the RC circuit created with the 2.2µF capacitor and the internal resistor. The open collector driver should not be shared with any other circuitry.

The circuit shown in the RESET Control when Sleep is Not Enabled diagram is recommended when external control of the $\overline{\text{RESET}}$ pin is desired and the PHY is not allowed to go to sleep.

The 2.2µF capacitor can only be removed if the external reset control will guarantee that the PHY remains in POR for no less than 10mS after power on. After power on, the PHY can be reset with a negative pulse lasting no less than 100nS. The PHY should not be held in POR for longer than 100mS after power on and less than 100µS during normal operation. Causing the PHY to enter POR will disrupt any activity on the serial bus and cause a long reset (not an arbitrated short reset). The Software POR in Link Accessible Register (LAR) 0xF bit 0 should be used as a first approach to resetting the PHY.

While in POR, the PHY tri-states the CTL(0:1), DATA(0:7), LREQ, and LPS interface pins. The SCLK continues to generate Sclk in POR. Link_on is driven low at this time.

The PHY offers the Link the ability to issue a POR to the PHY by writing PHY register 0xF with 0x80. Within a few cycles, the PHY will issue the Link a status of bus reset as it exits POR and enters bus reset.

Holding the PHY in Power-On-Reset

While in Power-On-Reset (POR), the PHY will create Tp_Bias on all ports. Holding the PHY in POR could create problems on the serial bus as other nodes sense the PHY's Tp_Bias and try to go through reset. All ports should be disabled by writing 0x7 in PHY register 0xE when holding the PHY off the network for long periods. Disabling a port reduces the amount of power consumed and prevents the PHY from generating TpBias. In addition, if ports are disabled within the remote PHY's debounce time (usually 0.3 seconds), the serial cable connection will not interrupt the existing network until after the port is enabled.

Normally when the PHY is initially powered on, the PHY is held in reset via an RC circuit created with a 2.2µF capacitor and an internal resistor as shown in Recommended RESET Circuit on page 19.

Setting Module Pins to Configure PHY as a Repeater

Module Pin	Connection
Sclk	Float (or 3.3K ohm to GND to reduce EMI emissions).
Ctl(0:1), Data(0:7)	Float
$\overline{\text{Direct}}$	GND
DTE	GND
SLEEP_EN	V_{DD} to enable Sleep otherwise GND
LPS	Resistor to GND (1K to 3.3K ohm typical)
Link_on	Float (or 3.3 K ohm to GND to reduce EMI emissions).

PHY Hardware Simulation Mode

The IBM PHY offers the unique ability to operate in an environment that is at a very slow speed. This feature enables the IBM PHY to be connected directly to hardware emulators (i.e. emulating a Link), while supporting IEEE-1394 communication over the standard IEEE 1394 cable to other IBM PHYs running in the same mode. The PHY will initialize the bus and operate as it would normally, except much more slowly.

The procedure to slow down the PHY for simulation purposes is as follows.

1. The PHY must be wired normally as defined by this specification. The following changes must be made:
   - Module pin TEST_0 must be tied to V_{DD}.
   - The TpBias capacitor must be changed according to the following equation:

     $$C = \frac{0.0248\text{Amps} \times 48\text{cycles} \times \text{Toscin}}{0.05\text{V}}$$

     where Toscin = 1/(osc_in input frequency)
   - Osc_in is applied a frequency that should not exceed 50MHz.
2. All the PHYs on the "slow down" network must have their oscillators set within 100 PPM to function properly. You must comply with all 1394 rules (e.g. max. packet length at a given speed). For example, if you request the bus for a 400Mb/s, your packet length must not exceed 4K bytes even though you slowed down the frequency.

Frequency Translation for Hardware Simulation Mode

Signal Name	Signal Rate
Osc_in	400MHz
Osc_in/2	200MHz
Osc_in/4	100MHz
Osc_in/8	50MHz (sclk)

If you apply a 25MHz signal to osc_in, your sclk will be 3.13MHz (Osc_in/8) rather than the 50MHz if you were in normal mode. If you send the PHY a 400Mb/s link request, the PHY will transmit 400Mb/s speed signaling but the actual rate will be your osc_in (25Mb/s in this example).

Using Only One or Two Ports of the Three-Port PHY

Unused Port	Wire As …
TPAn, $\overline{\text{TPAn}}$	Floated or tied to GND
TPBn, $\overline{\text{TPBn}}$	Connected to GND
TpBias_n	≥0.1µf cap to GND
n = the number of unused ports.	

Programming the PHY

Register Mapping

Register Map for One-Port PHY

Address	0	1	2	3	4	5	6	7
0000_2	Physical_ID						R	CPS
0001_2	RHB	IBR	Gap_Count					
0010_2	SPD		E	Number of Ports				
0011_2	AStat 1		BStat 1		Ch 1	Con 1	Peer Sp 1	
0100_2	ENV		Reg Count					
0101_2	Reserved							
0110_2								
0111_2								
1000_2								
1001_2								
1010_2								
1011_2	LPS Input	PHY Delay		CMC	Power Class			Reserved
1100_2	CMC Input	CPS Interrupt	L-P Self-test EEH	Arbitration Phase		Arbitration State		
1101_2	Reserved	Enable L-P Selftest	Reserved		En. Ack Accel Arb	Reserved	En. Multi Sp Concat	Mask LPS bit
1110_2	En. TX/RX timeout	Ignore Unplug	Override CMC	Soft CMC	Reserved	Disable P1	Reserved	
1111_2	Soft POR	Reserved	Send P-L packet	Ack_Accel Cycle Sync	ISBR	Reserved		

Register Map for Three-Port PHY

Address	0	1	2	3	4	5	6	7
0000_2	Physical_ID						R	CPS
0001_2	RHB	IBR	Gap_Count					
0010_2	SPD		E	Number of Ports				
0011_2	AStat 1		BStat 1		Ch 1	Con 1	Peer Sp 1	
0100_2	AStat 2		BStat 2		Ch 2	Con 2	Peer Sp 2	
0101_2	AStat 3		BStat 3		Ch 3	Con 3	Peer Sp 3	
0110_2	ENV		Reg Count					
0111_2	Reserved							
1000_2								
1001_2								
1010_2								
1011_2	LPS Input	PHY Delay		CMC	Power Class			Reserved
1100_2	CMC Input	CPS Interrupt	L-P Self-test EEH	Arbitration Phase		Arbitration State		
1101_2	Reserved	Enable L-P Selftest	Reserved	Reserved	En. Ack Accel Arb	Reserved	En. Multi Sp Concat	Mask LPS bit
1110_2	En. TX/RX timeout	Ignore Unplug	Override CMC	Soft CMC	Reserved	Disable P1	Disable P2	Disable P3
1111_2	Soft POR	Reserved	Send P-L packet	Ack_Accel Cycle Sync	ISBR	Reserved		

PHY Register Fields (Part 1 of 3)

Field	Size	Type	Description
Physical_ID	6	r	Node address determined during self-identification.
R	1	r	Root indication. 1 = this node is the root.
CPS	1	r	Cable power status. 1 = power in the cable.
RHB	1	rw	Root hold-off bit. 1 = the PHY will attempt to become the root during the next bus reset.
IBR	1	rw	Initiate bus reset.1 = initiate a bus reset at the next normal arbitration phase.
Gap_count	6	rw	Arbitration timer setting. Used to optimize the Subaction Gap time, the Arbitration Reset Gap time, and the Arbitration Response Time threshold, based on the size of the network. This field is initially reset to a value of 0b'111111'. See clauses 4.3.6 and 8.4.6.2 of the IEEE 1394-1995 Standard [1].
SPD	2	r	Maximum data transfer rate. 00 = 98.304Mb/s 01 = 196.608Mb/s 10 = 393.216Mb/s 11 = reserved When read, the IBMIBM21S850 and IBM21S851 both return 10 to indicate 400Mb/s.
E	1	r	Enhanced register map indication. This product has an enhanced register map, so this field will always be '1'.
Number of Ports	5	r	The number of ports on this PHY. IBM21S850 will always read 0b'00011' indicating it has three ports. IBM21S851 will always read 0b'00001' indicating it has one port.
AStat 1	2	r	TPA arbitration signal state on Port 1. 11 = Z 01 = 1 10 = 0 00 = invalid
BStat 1	2	r	TPB arbitration signal state on Port 1. 11 = Z 01 = 1 10 = 0 00 = Port not connected
Ch 1	1	r	Port 1 child indication. 1 = child port; 0 = parent port.
Con 1	1	r	Port 1 connection status. 1 = port 1 is connected; 0 = port 1 is disconnected.
Peer Sp 1	2	r	Maximum Peer Speed latched during SID Speed Capability Exchange for Port 1.
AStat 2	2	r	TPA arbitration signal state on Port 2. 11 = Z 01 = 1 10 = 0 00 = invalid
BStat 2	2	r	TPB arbitration signal state on Port 2. 11 = Z 01 = 1 10 = 0 00 = Port not connected
Ch 2	1	r	Port 2 child indication. 1 = child port; 0 = parent port.
Con 2	1	r	Port 2 connection status. 1 = port 2 is connected; 0 = port 2 is disconnected.
Peer Sp 2	2	r	Maximum Peer Speed latched during SID Speed Capability Exchange for Port 2.

PHY Register Fields (Part 2 of 3)

Field	Size	Type	Description
AStat 3	2	r	TPA arbitration signal state on Port 3. 11 = Z 01 = 1 10 = 0 00 = invalid
BStat 3	2	r	TPB arbitration signal state on Port 3. 11 = Z 01 = 1 10 = 0 00 = Port not connected
Ch 3	1	r	Port 3 child indication. 1 = child port; 0 = parent port.
Con 3	1	r	Port 3 connection status. 1 = port 3 is connected; 0 = port 3 is disconnected.
Peer Sp 3	2	r	Maximum Peer Speed latched during SID Speed Capability Exchange for Port 3.
ENV	2	r	Environment indication. Cable PHY value = 0b'01'.
Reg Count	6	r	Register count. This field indicates the number of registers that follow. IBM21S850 always reads 0b'001001' indicating nine registers to follow. IBM21S851 always reads 0b'001011' indicating eleven registers to follow.
LPS Input	1	r	Reflects LPS input pin. Indicates Link Power Status from either DC or a toggling signal of greater than 0.5MHz received at that pin.
PHY Delay	2	r	Worst case repeater data delay. Set to '00' which indicates less than or equal to 144 ns.
CMC	1	r	Configuration manager capable. Reflects CMC value to be transmitted in the SID packet. If CMC override is enabled, this bit may differ from CMC input.
Power Class	3	r	Power consumption and source characteristics. These bits simply reflect the present state of the PS1, PS2, and PS3 primary input pins. Register bit 4 reflects PS1 module pin which is reflected in self_id bit 21. Register bit 5 reflects PS2 module pin which is reflected in self_id bit 22. Register bit 6 reflects PS3 module pin which is reflected in self_id bit 23.
CMC Input	1	r	Reflects module CMC input pin. Enables software to read the hardwired input pin.
CPS Int	1	r	Cable power status interrupt. This bit indicates that the Cable Power Status input has transitioned from being active ('1') to inactive ('0'), indicating a power failure. A status transfer is initiated as a result, with the State_Timeout bit getting set. Writing '1' to this bit clears the State_Timeout field to '0'.
LP_Selftst EEH	1	r	Link-PHY interface self test Error Ever Happened status indication. This bit is set to '1' when an error has occurred when testing the Link-PHY interface. This bit is reset to '0' at POR or when "Enable L-P selftest" bit is disabled.
ARB Phase	2	r	Present arbitration state machine phase. 00 = Bus Reset 01 = Tree ID 11 = self-ID 10 = Normal Arbitration
Arb State	3	r	The current Arbitration State Machine state, encoded in binary as defined in [1].
Enable L-P Selftest	1	rw	Enables the Link-PHY self test function to test. Defaults to '0' at POR.
Enable Ack Accel Arbitration	1	rw	Enables the Ack Accelerated Arbitration function. 1 = the PHY will arbitrate immediately following an ACK packet (i.e. it will not wait for a sub-action gap). 0 (Default) = the PHY waits for sub-action gaps before handling the next fair or priority request.

PHY Register Fields (Part 3 of 3)

Field	Size	Type	Description
Enable Mult_Sp Concat	1	rw	Enables the PHY to interpret the Link-PHY Data lines in the Link Hold Cycle (indicating the transmitter wants to concatenate) as the speed of the next pkt. The encoding is identical with that given to the Link in receive. (i.e. S200 = 0100xxxx. and S400 = 01010000). NOTE: According to the P1394a specification [2], one can never downgrade to S100 speed due to compatibility issues with existing hardware. 0 (Default) = 1394-1995 behavior: all packets at same speed as the initial packet. 1 = interpret speed from data.
Mask LPS Bit	1	rw	Masks out the LPS bit transmitted in the SID packet. Defaults to '0' on POR. 0 = SID LPS bit set to LPS input 1 = SID LPS bit forced to be 0
Enable TxRx Timeout	1	rw	Control of PHY's response regarding state timeout when in either Tx or Rx. (Default)0 = 1394-1995 response: do not reset in Tx or Rx (default) 1 = reset in Tx or Rx
Ignore Unplug	1	rw	Control of PHY's response to a port disconnecting from the network. 0 (Default) = 1394-1995 response: force a bus reset to disconnect 1 = ignore disconnecting
Override CMC	1	rw	Enables software to override hardwired CMC bit. 0 = hardwired CMC output 1 = soft CMC output
Soft CMC	1	rw	Software CMC bit. This bit holds the override value for CMC.
Disable P1	1	rw	Software control of port 1 operation. Two operations affected: Port status of port (local port disable) and TpBias output voltage. 0 = normal operation 1 = local port disabled and TpBias forced to 0V, which emulates a disconnect for the remote port connected to this PHY.
Disable P2	1	rw	Software control of port 2 operation. Two operations affected: Port status of port (local port disable) and TpBias output voltage. 0 = normal operation 1 = local port disabled and TpBias forced to 0V, which emulates a disconnect for the remote port connected to this PHY.
Disable P3	1	rw	Software control of port 3 operation. Two operations affected: Port status of port (local port disable) and TpBias output voltage. 0 = normal operation 1 = local port disabled and TpBias forced to 0V, which emulates a disconnect for the remote port connected to this PHY.
Soft POR	1	rw	Software control of Power On Reset function that is normally initiated through $\overline{\text{RESET}}$ module pin.
Send PL Diag Pkt	1	rw	Send a PHY-Link interface diagnostic packet (SID Pkt) to the Link at 400Mb/s. This will enable the checking of PHY-Link data lines and timings. This feature is a diagnostic aid only and should not be used when the Link could receive information from the serial bus. One should disable all ports via LAR_Reg14 (Link Accessible Register) when using this feature to prevent unwanted packets. An additional function performed is the generation of the first quadlet for the self-ID packet.
Ack_Acc CycleSync	1	rw	One method of degating the Ack_Acc_Arb using a register write since most existing Links will not be able to send out a CycleSync request.
ISBR	1	rw	Initiate Short Bus Reset will cause the PHY to arbitrate for the serial bus and perform a short (1.3mS) reset.

Multi-Speed Concatenation

The IEEE-1394 standard requires that all concatenated packets be transmitted at the same speed. If a node is required to transmit packets at various speeds, as in the case of isochronous data directed to different portions of the bus, the PHY must arbitrate for each change in speed. Multi-speed concatenation enables the node to concatenate packets at different speeds and therefore recover the lost bandwidth due to arbitration.

The PHY device concatenated packet reception follows the mechanism of Annex J of the 1394-1995 Standard [1], in which the packet speed code is expected at the beginning of each packet. Receive speed codes are shown in the Send and Receive Speed Codes table below. For transmission at multiple speeds, the Link needs a way to signal to the PHY what speed the next packet in the concatenated chain will be. This is accomplished in the P1394a specification [2] by letting the Link drive the speed code for the next packet onto the data bus at the same time that it drives the bus_hold code onto the control bus. See the following concatenation timing diagrams, as well as Block Diagram: Three-Port PHY on page 3 , Direct Connection Diagram on page 12, and Capacitive Isolation Barrier on page 13. The same speed codes that are used for receiving are to be used for sending. Note that in order to maintain compatibility with existing hardware, the speed is not allowed to be downgraded to S100 from a higher speed.

The IBM PHY has a control bit called Enable Mult_Sp Concat in the PHY register that enables it to interpret the speed codes as they are sent in each packet. When the control bit is set to 1, the PHY conforms to P1394a multi-speed concatenation rules. For compatibility with earlier vintage hardware, the control bit may be set to 0, causing the PHY to conform to 1394-1995 concatenation in which all packets are transmitted at the same speed as the first packet.

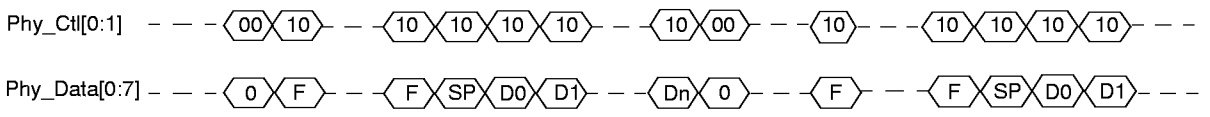
Even if this feature is disabled because the Link cannot handle it, the PHY always remains compatible with multi-speed concatenation on the serial bus. The concatenation is transparent to the Link. This enables the node to remain compatible with other nodes that will transmit multiple speed concatenated packets.

Send and Receive Speed Codes

D[0:7]	Data Rate
00xxxxxx[1]	S100
0100xxxx	S200
01010000	S400

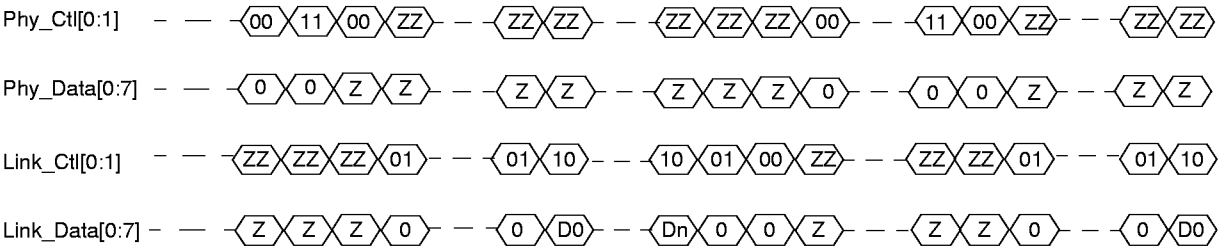
1. The “x” means transmitted as 0, ignored on receive.

Concatenated Packet Reception



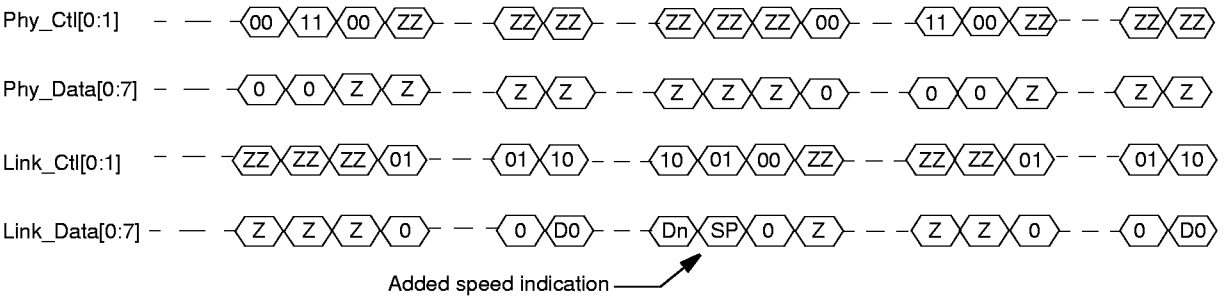
Note: Timing information is binary for control and hexadecimal for data.

1394-1995 Concatenated Packet Transmission



Note: Timing information is binary for control and hexadecimal for data.

P1394a Multi-Speed Packet Transmission



Note: Timing information is binary for control and hexadecimal for data.

Functions Pertaining to Annex-J of the IEEE Standard 1394-1995

Control Lines

The control lines between the Link and PHY are bidirectional and are encoded as described in the following two tables.

Ctl(0:1) When the PHY is Driving

Ctl(0:1)	Name	Description
00	Idle	No Activity.
01	Status	Status information is being sent to the Link.
10	Receive	Data is being transferred to the Link.
11	Grant	The PHY grants the Link the bus to transmit.

Ctl(0:1) When the Link is Driving

Ctl(0:1)	Name	Description
00	Idle	Transmit is complete, the Link releases the bus.
01	Hold	The Link is holding the bus or indicating that it wishes to concatenate a packet.
10	Transmit	Data is being transferred to the Link.
11	Unused	

Link Request

The link uses a serial data stream over the link request connection to request access to the serial bus, issue a register read or write, or to disable ACK acceleration (CycleSync) packet.

Bus Request

If the Link request transfer is a bus request, it is seven bits long and is of the format shown in the table below.

Bus Request Format

Bit(s)	Name	Description
0	Start Bit	Always 1.
1-3	Request Type	Indicates the type of bus request: 000: Immediate request. 001: Isochronous request. 010: Priority request. 011: Fair request.
4-5	Request Speed	Requested speed for the transmission. 00: 100Mb/s. 01: 200Mb/s. 10: 400Mb/s. 11: > 400Mb/s. (Invalid for this PHY)
6	Stop Bit	Stop Bit. Must be 0 for a valid request.

There are four types of bus requests that the Link may send the PHY: Immediate, Isochronous, Priority, and Fair. With the exception of the isochronous request, the Link must not send the PHY another bus request until

the first bus request is either lost or completed (the Link returns the Link-PHY interface back to the PHY after it has completed its transmission, or after the last transmission in the case of a concatenated packet). The handling of the isochronous request has been expanded to accept a subsequent request in transmit (P1394a enhancement).

With some packets as short as one cycle (400Mb/s acknowledge), it is possible that the PHY may enter and leave receive while the Link is sending the PHY a bus request (seven cycles long). The PHY does not consider a request as "received" until one cycle after the reception of the stop bit. All bus requests are lost when the PHY enters bus reset.

Immediate Request

An Immediate Request is used by the Link to acknowledge an asynchronous packet addressed to it. The PHY accepts the immediate request any time after the PHY indicates receive on the control lines and up until the fourth cycle after the PHY asserts Idle. An immediate request is ignored if the start bit for the request is received later than the fourth cycle after the Link-PHY interface went idle.

Isochronous Request

The PHY accepts an isochronous request at any time and will hold the request until honored, or until the bus is reset. The IBM21S850 and IBM21S851 feature enhanced handling of isochronous requests to accept the isochronous request while in transmit. This P1394a enhancement is limited to only isochronous requests. Even though the PHY will accept this request at any time, the P1394a specification [2] places specific restrictions on when the Link is allowed to issue the request.

Priority Request

The PHY accepts a priority request any time the Link-PHY interface does not indicate transmit or receive. This request is lost when the PHY indicates either transmit, receive, or bus reset. The PHY asserts the serial bus to either arbitrate or take control of the bus after a subaction gap plus an arbitration delay for a priority request that is pending at the time of a subaction gap. Fair protocol is ignored. A request received after a subaction gap is honored after the arbitration reset gap plus the arbitration delay.

With ACK acceleration enabled, the PHY asserts the bus according to the rules above unless an ACK is received by the PHY. When the PHY receives a priority request and the previous packet was an ACK, the PHY will honor the priority request immediately. (Please refer to ACK Accelerated Arbitration on page 33 for a discussion of ACK accelleration.)

Fair Request

A fair request is handled the same as the priority request with the limitation that the PHY only honors one fair request within a fairness interval (i.e. an arbitration reset gap must be detected between fair requests). Fairness protocol is imposed with ACK acceleration.

Read Request Format

Bit(s)	Name	Description
0	Start Bit	Always 1.
1-3	Request Type	100: Indicates that is a PHY register read request.
4-7	Address	The address of the request PHY register.
8	Stop Bit	Always 0 for a valid request.

Write Request Format

Bit(s)	Name	Description
0	Start Bit	Always 1.
1-3	Request Type	101: Indicates that is a PHY register write request.
4-7	Address	The address of the register to be written.
8-15	Data	Data to be written to the addressed register.
16	Stop Bit	Always 0 for a valid request.

Status Transfer

The PHY places status on the control lines (ctl=01b) while it transfers the status information on data(0:1). The PHY may initiate a status transfer any time that the interface is idle and the PHY has status information to be transferred to the Link. The only exception is that the PHY does not return status information during the transmission or reception of a concatenated packet, nor does it return read data just prior to a subaction gap as discussed in Register Read Data Near a Subaction Gap on page 32. The PHY may prematurely end the status transfer by placing anything other than status on the control lines. A status transfer can vary between four and 15 bits and is of the format shown in the table below.

Status Format

Bit(s)	Name	Description
0	Arbitration Reset Gap	The PHY has detected an arbitration reset gap.
1	Subaction Gap	The PHY has detected a subaction gap.
2	Bus Reset	The PHY has entered the bus reset state
3	State Time-out	One of the following events has occurred on the PHY: 1) PHY stayed in a particular state for too long. Usually the network has been configured in a loop. Refer to the “Loop Detection” section on p.38. 2) The module CPS pin has transitioned from being active (‘1’) to inactive (‘0’).
4-7	Address	This contains address of the register data when register data is being transferred.
8-15	Data	The register data from the address in bits 4-7.

Because the IEEE Standard 1394-1995 [1] is not clear on how the PHY is to handle an interrupted status, the IBM PHY handles status transfers in the following manner:

1. The PHY never interrupts the first four bits of a status transfer.
2. All interrupted status transfers are resent at the first opportunity and contain the entire status from the beginning. The first four status bits are always updated and valid for the transfer.

Register Read Data Near a Subaction Gap

A node uses the PHY's indication of subaction gap to determine the completion of bus reset and the end of an isochronous cycle. If the Link issues the PHY a register read such that the PHY could be returning the data as the subaction gap occurs, the PHY may go into receive before it has the opportunity to notify the node of the status. To prevent this, the PHY does not return register data a few cycles prior to a subaction gap to ensure that gap indications are sent to the Link. The PHY returns the register read data with the status notification. If the PHY begins receiving data on the serial bus, the PHY interrupts the status transfer only after sending the first four status bits to the Link. The PHY attempts to send the read data again at the first opportunity that the L/P interface is idle.

Link Power Status

The PHY uses the LPS pin to detect the presence of an active link and this is reflected in the PHY's self_id packet. To accommodate isolation, the PHY will tolerate an oscillating signal at this pin. If the input is high for one or more Sclk cycles, the Link is considered powered up. If the input is held low for more than 1.3µS, then the Link is considered powered down. When the PHY considers the Link as powered down, the PHY asserts low on Ctl(0:1), and Data(0:7) pins. Sclk will continue for as long as the PHY is not asleep.

When the PHY is in the idle state and detects a Link becoming active, it enables the Link-PHY interface. This prevents the PHY from sending the Link a partial packet. The PHY accepts all register reads and writes as long as the LREQ rules are followed, but a delay of up to 100µs (maximum bus occupancy) might occur before the PHY enters the idle state and enables the interface. During this time, all status indications are lost: only a register read request is held until the interface is enabled. Even though the PHY can process consecutive reads and/or writes, it may not have the interface to return the request. Therefore, the Link should not issue another read or write request while there is a pending read request.

The Link may wish to have the Link-PHY interface active without indicating to the network that it is fully operational. This may be the case where the Link wishes to read PHY register information before entering the network. With LPS low, the Link may write PHY register 0xD bit 7 with a logic '1'. This will override the value of the LPS input and cause the PHY to always report an inactive Link within its self_id packet until the override is disabled by writing a '0' to the same location.

Setting the Gaps

It is very important that all 1394 PHYs have their gaps set to the same value. It is also important to realize that the gaps are reset to 63 on the second bus reset after being set. This must be considered when issuing a bus reset from PHY register 0x1 if the network has its gaps set to something other than 63. The concern is that all remote PHYs may reset their gaps while the writing of register 0x1 holds the local PHY's gaps at the previous value. It may be required to transmit the appropriate PHY configuration packet prior to issuing the reset. All PHY configuration packets that alter the gap setting should be followed with a bus reset. The bus reset is needed to confirm that all PHYs have their gaps set identically and arm the PHYs to default back to a gap setting of 63 on the next reset (second reset from the PHY configuration packet) that could be caused by connecting two networks together. Defaulting back to a gap setting of 63 ensures a valid network after the reconfiguration.

Programming the CMC

The IBM PHY CMC module pin is used by the PHY to report in its self_ID packet whether the node is capable of being the configuration or resource manager. The IBM PHY allows the node to use software to change the value of the CMC reported by the PHY. The IBM PHY allows the software to:

1. Obtain the value for the CMC module pin by reading the “CMC input” in LAR 0xC, bit 3.
2. Change the value of the CMC to the value in LAR 0xE “Soft CMC” by setting the “Override CMC” bit, also in LAR 0xE.
3. Read the value of the CMC the PHY will use in the next self_id packet to ensure the desired setting. The value of the CMC in LAR 0xB is not necessarily what the PHY transmitted in the last self_ID packet if you have made any changes.

ACK Accelerated Arbitration

In normal communication, the PHY must wait for a subaction gap plus an arbitration delay before asserting the bus for a fair or priority bus request. The subaction gap is to ensure adequate time for an acknowledge packet to be returned after an asynchronous transfer. Arbitration delay ensures that all PHYs detect the subaction gap. With the gaps set to maximum, the subaction gap is ≅10uμS, and an Arbitration delay adds another ≅ 2.6μS. ACK Accelerated Arbitration allows the PHY to begin arbitrating for the bus as soon as it detects an idle bus after an acknowledge packet, and therefore recover the ≅ 12.6μS of bandwidth. As a result, serial bus utilization is significantly improved and cycle start jitter is minimized.

According to the P1394a specification [2], ACK acceleration has some restrictions when operating in a network with isochronous traffic. The timely transmission of the cycle start packet is key to proper isochronous operation. The nature of ACK acceleration could cause an undesirable delay in the transmission of the cycle start packet if the root node has not been enabled or is not capable of ACK acceleration. Therefore, proper operation of ACK acceleration must be limited to after isochronous data and before the next cycle start packet. The Link is responsible for disabling the ACK acceleration.

The CycleSync request method on the PHY was designed to earlier drafts of the P1394a specification in which the CycleSync disables the acceleration until the next subaction gap, at which time the PHY enables ACK acceleration. To maximize interoperability with existing Link hardware (which may not be able to issue this new type of request), a second more generic method of disabling the acceleration has been added to the PHY. A register write to PHY register 0xF bit 3 accomplishes the same result as the CycleSync request: the disabling of ACK acceleration at the time of a cycle start packet.

On this PHY, because the implementation does not require software intervention after the feature is enabled while the PHY is root, it is recommended that the root node always have this feature enabled. Installed applications that do not use isochronous data need only to enable this feature on all PHYs to greatly improve the network performance. If the network supports isochronous traffic, the Link should enable and disable ACK acceleration via the PHY register 0xD bit 4 on all child nodes to ensure timely cycle start transmission rather than using CycleSync or the CycleSync register bit in PHY register 0xF bit 3.

Sleep Mode

The PHY is capable of being put into a sleep mode when none of the ports are connected, simply by raising the SLEEP_EN pin to a logic '1'. Alternatively, in cases where Link-PHY isolation is required, the PHY may be put into sleep mode by toggling the SLEEP_EN pin with a signal between 4MHz and 20MHz. During sleep mode, the cable drivers, the Tp_Bias voltage sources, the phase-locked loop, and the SCLK output are all powered down, making it an attractive feature for battery powered applications.

The presence or absence of the SCLK can be used by the Link to determine whether the PHY is in sleep mode or not, and this information can be passed on to the device driver. When the SCLK is off, power is reduced even in Links that have no sleep mode, because the majority of the logic is clocked by the SCLK. When a Link with sleep mode is told by its device driver to power down, it reports that fact to the PHY through the LPS pin. The device driver may also want the PHY to power down, and would communicate that message through the SLEEP_EN pin. However, the PHY may need to remain awake to perform repeater functions. If no ports are connected, then both Link and PHY can be powered down.

When the PHY is asleep, it monitors only a cable connect or a low SLEEP_EN pin. Upon detection of either, the PHY awakens, begins self-ID, and reports the Link as powered down (LPS). When it is required that the Link wake up as well, the PHY receives a Link On packet and indicates it to the Link via the LINK_ON pin.

State Time-Out

The PHY has expanded the use of the state time-out indication to operate as a PHY interrupt similar to P1394a. The PHY initiates a status transfer of state time-out when the following events occur:

1. The PHY has stayed in a particular state for too long as defined by the IEEE Standard 1394-1995 [1]. Usually the network has been configured in a loop. Refer to Loop Detection below.

   The PHY also expands the controlling of state time-out to transmit and receive when PHY register 0xE bit 0 "enable TX/RX Time-out" is set. With the "enable Tx/Rx timeout" bit set, the PHY issues a state time-out and enters bus reset when it finds itself in transmit or receive for longer than the allowed time as defined in [1] for the arbitration states. The state time-out is significantly longer than the maximum bus occupancy allowed by the standard.

2. The CPS interrupt bit in PHY register 0xC bit 1 was set to '1'. As a result, the CPS module pin has changed from active (1) to inactive (0) indicating the loss of cable power. This interrupt only occurs when the CPS interrupt bit transitions to '1'. The interrupt bit must be cleared by writing a '1' to PHY register 0xC bit 1.

Loop Detection

If the PHY indicates state time-out, it may be the result of the network being configured in a loop. If the network does not recover from a state time-out and the time-out was not caused by the loss of cable power, the Arbitration State and Phase contained in PHY register 0xC will contain the current state of the PHY as defined by [1]. If the arbitration state and phase indicate the PHY is in state T0, then the network has been configured in a loop. Reading that the PHY is in states R0 or R1 is an indication that the PHY has returned to bus reset and is trying to recover the bus. From the time of the state time-out, the arbitration state and phase will always indicate T0 for as long as the PHY is configured in a loop. The decode of the arbitration state and phase is included in the register description of PHY register 0xC.

Cable PHY Packets

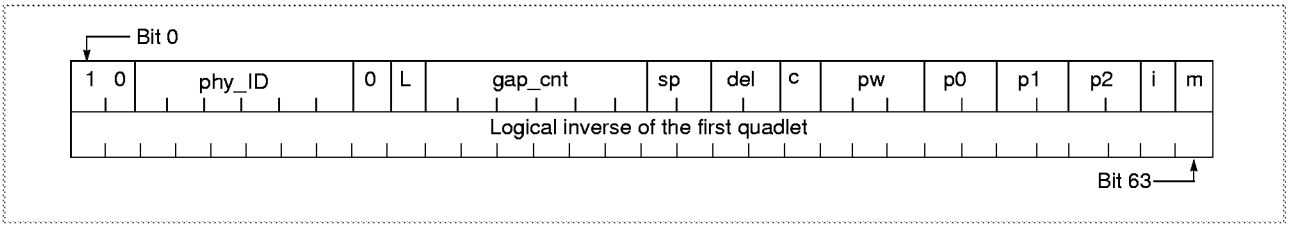
Three cable PHY packets are defined in the IEEE Standard 1394-1995 [1]:

- Self_ID packet
- Link-on packet (defined in section 4.3.4.2)
- PHY configuration packet (defined in section 4.3.4.3)

Self Identification

The PHY complies with [1] (section 4.3.4.1) which requires the sending of the contents of PHY register 0 to the link as a status transfer while it transmits its self_ID packet. The PHY does not send its own self_ID packet to the link (a P1394a requirement) but makes the information available in PHY register 0xB that would otherwise be unavailable to the local node. The PHY sends one self_ID Packet over the serial bus to identify its node. The self_ID packet is included here for completeness in the referencing throughout this document.

Self_ID Packet Format



Self-ID Packet Information

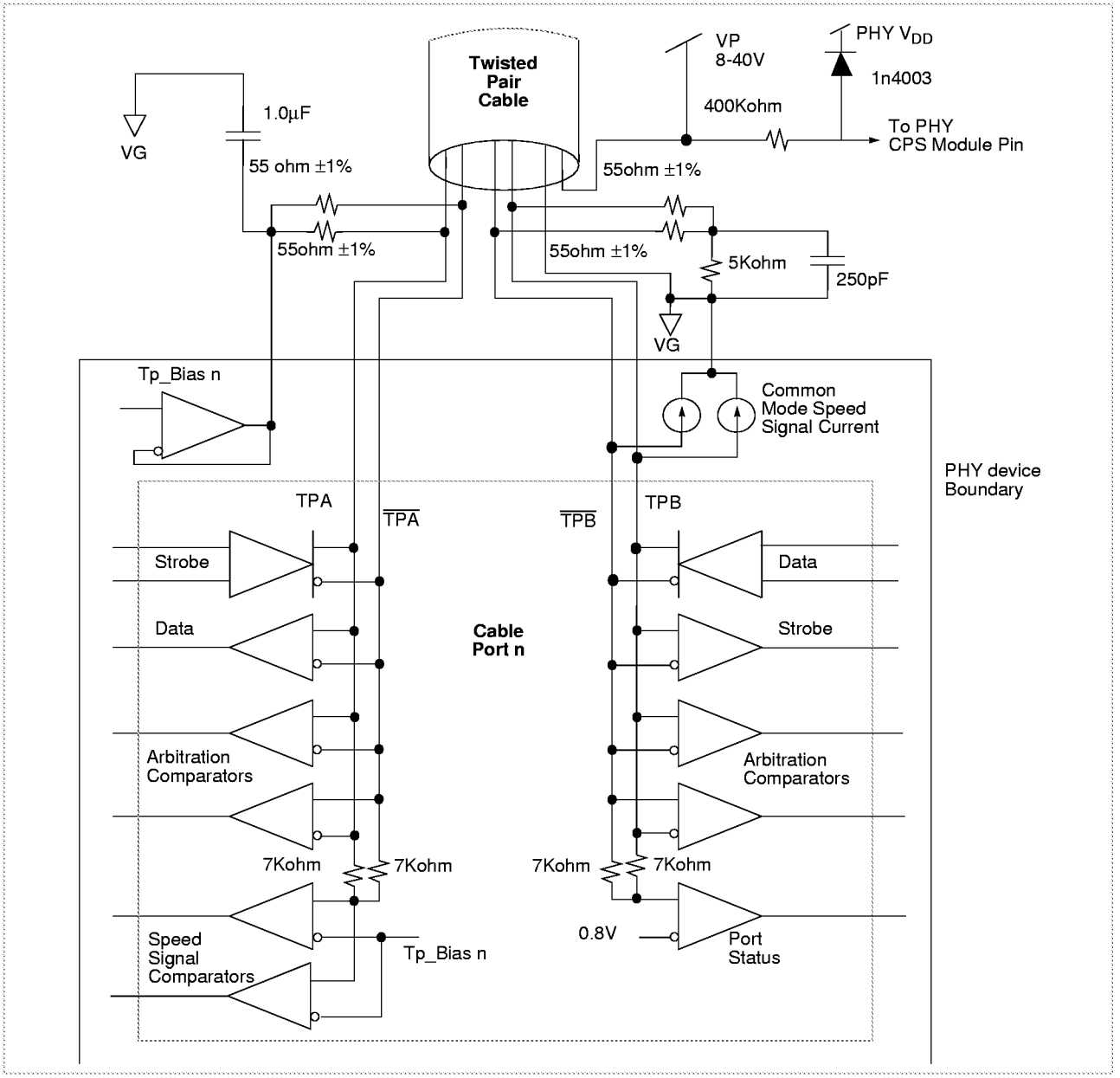
Bit(s)	Self_ID Packet Identifier
phy_ID	Physical address of the packet originator
L	Indicates an active link. 1 = active Link
gap_cnt	Value of the gap setting of the originator of this packet
sp	Maximum Speed capabilities for this PHY 00 = 98.304Mb/s 01 = 196.608Mb/s 10 = 393.216Mb/s The IBM21S850 or IBM21S851 transmits 10, indicating that it is capable of speeds up to 393.216Mb/s
del	Worst-case repeater data delay 00 indicates less than 144 ns.
c	Indicates that the link is a contender to be the bus or resource manager.
pwr	Indicates the power class for the identified node. Module pin PS_1, 2, & 3 are reflected in the self_ID bits 21, 22, & 23, respectively. In the table below (from left to right) the first position = PS-1, the second position = PS-2 and the third position = PS-3. 0 0 0 Node does not need power and does not repeat power. 0 0 1 Node is self-powered and provides a minimum of 15W to the bus 0 1 0 Node is self-powered and provides a minimum of 30W to the bus 0 1 1 Node is self -powered and provides a minimum of 45W to the bus 1 0 0 Node may be powered from the bus and is using up to 1W. 1 0 1 Node may be powered from the bus and is using up to 1W. An additional 2 W is needed to enable the link and higher layers. 1 1 0 Node is powered from the bus and is using up to 1W. An additional 5 W is needed to enable he link and higher layers. 1 1 1 Node is powered from the bus and is using up to 1W. An additional 9 W is needed to enable the link and higher layers. **Note:** This table is from the IEEE standard 1394-1995 [1].
p0... p3	Indicates the state of the ports on the PHY (p0 = port 0). 11 Connected to child node 10 Connected to parent node 01 Not connected to any other PHY 00 Not present on this PHY The IBM21S851 returns 00 for ports 2 & 3.
i	If set, this PHY initiated the bus reset. This optional bit is implemented on the IBM21S850 and IBM21S851.
m	0 = the PHY will not initiate additional self_ID packets.

Cable Interface

Twisted Pair

The twisted pair cable interface is the interface between the PHY and the serial cable. For the twisted pair A cables, TPA and $\overline{\text{TPA}}$, 55 ohm resistors are connected to Tp_Bias, with a 1.0µF capacitor from Tp_Bias to VG at each port. For the twisted pair B cables, TPB and $\overline{\text{TPB}}$, 55 ohm resistors are connected to a node having a 5 Kohm resistor and a 250 pF capacitor connected in parallel to VG. It is also important to note that the diagram below represents only one of the PHY's three cable ports. The external component connections indicated must be repeated for each port. Please read Board Layout Recommendations on page 41 for additional guidelines.

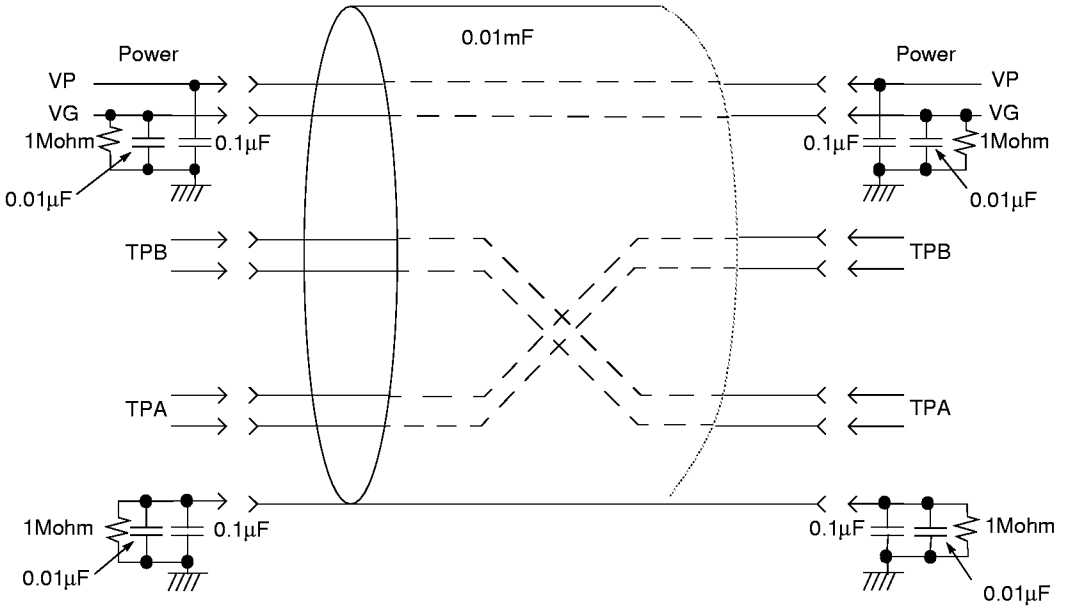
Twisted Pair Cable Interface Connections



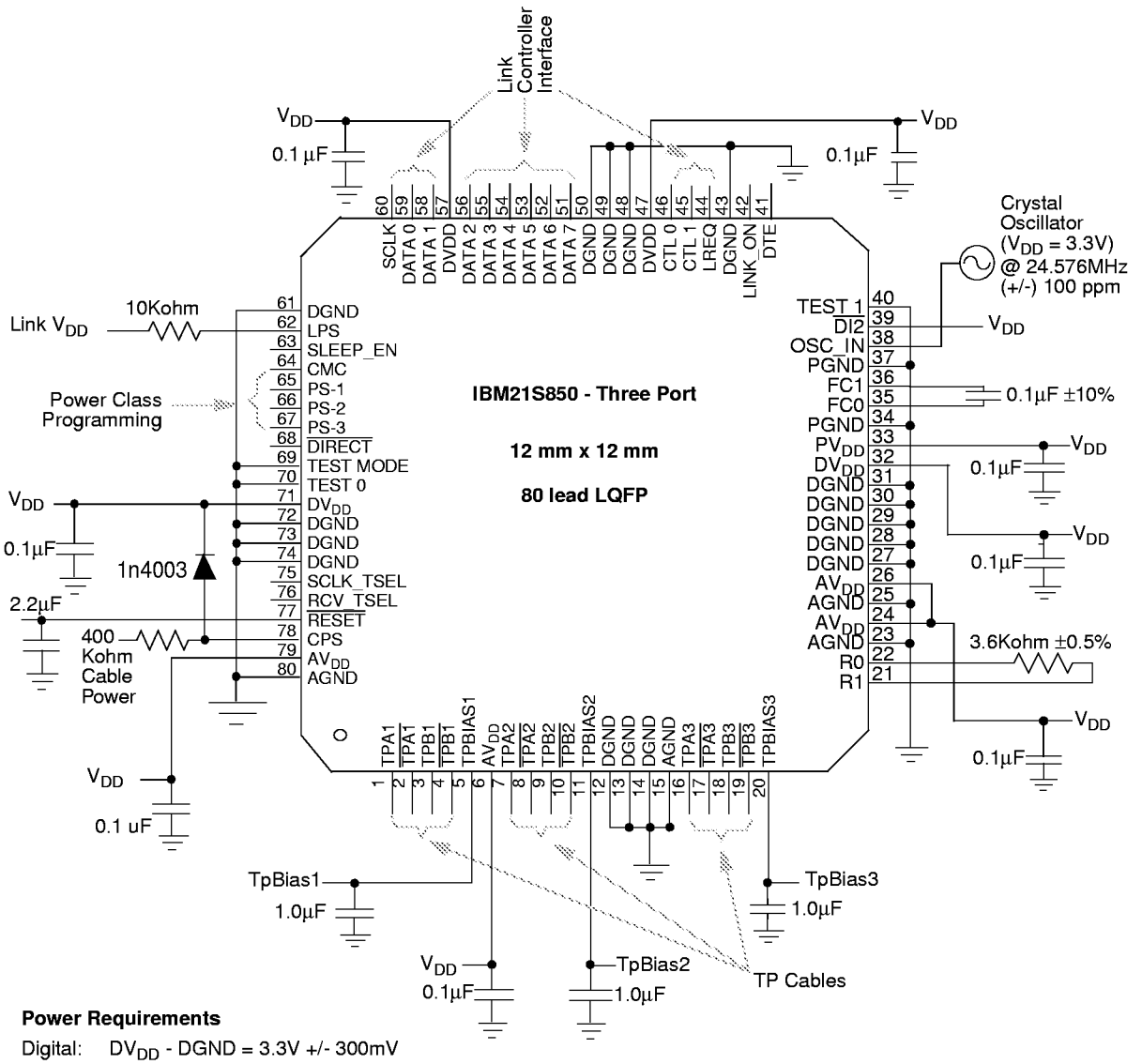
Cable Media

The cable media interface is the implementation of a physical connection. The cable media has two well shielded signal pairs with 110 ohm differential and one low impedance signal pair for the power. The diagram below shows all external component connections to the cable media. The cable shielding may be connected directly to ground in some applications.

Cable Media Interface



External Component Connections

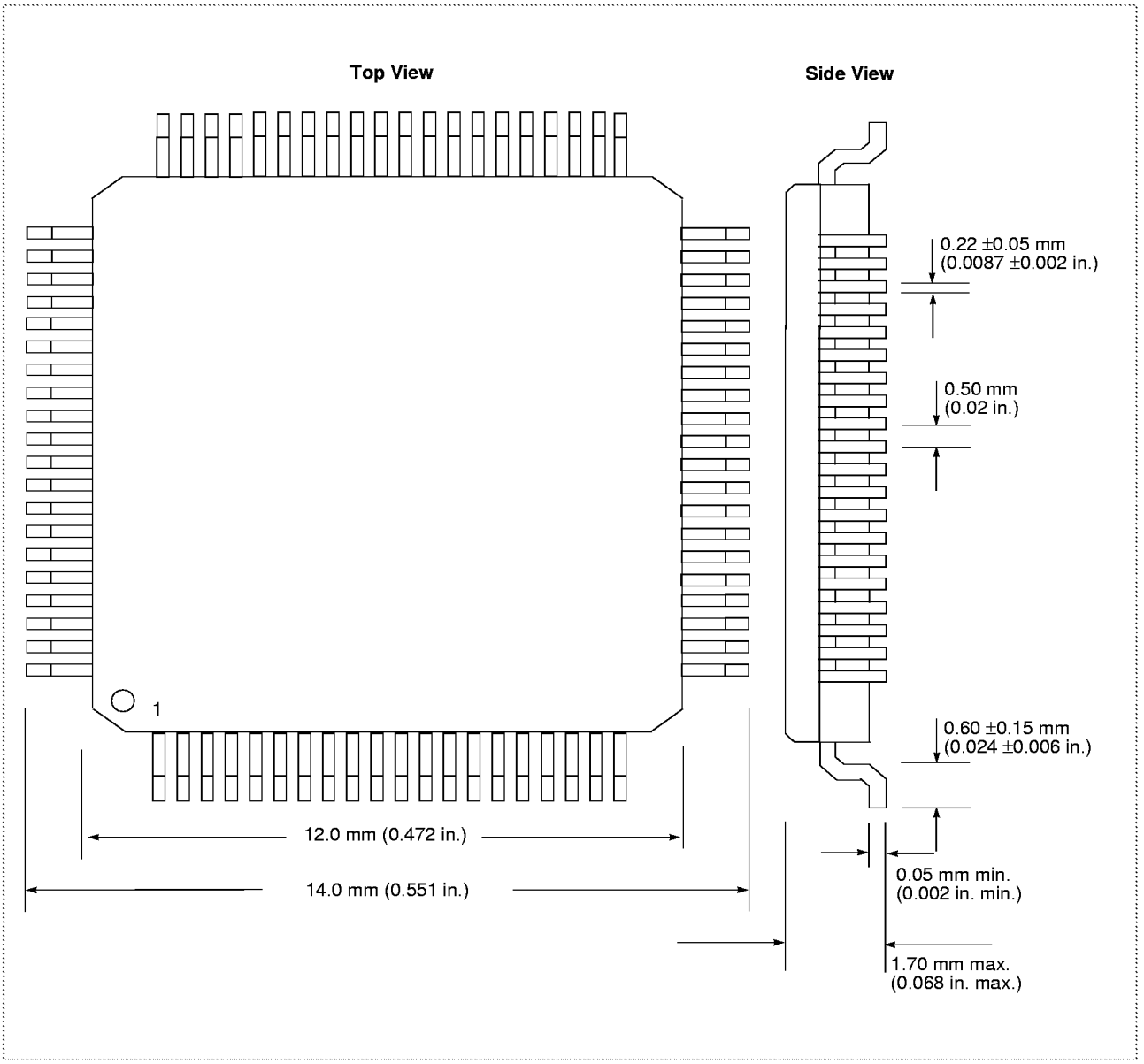


Power Requirements

Digital: DV_{DD} - DGND = 3.3V +/- 300mV

Analog: AV_{DD} - AGND = 3.3V +/- 300mV
PV_{DD} - PGND = 3.3V +/- 300mV (PLL supply may require filtering from the analog supply)

Package Diagram: 80-Lead LQFP



Board Layout Recommendations

- Route the traces for the differential pairs TPA/$\overline{\text{TPA}}$ and TPB/$\overline{\text{TPB}}$ very carefully. The signals within each pair should be routed quite closely, yet the two must maintain a differential impedance of 110 ohms. These guidelines help to achieve both of these goals.
  - Each trace should have a 55 ohm impedance.
  - Route the differential pair traces as closely as possible while maintaining a spacing between them of approximately four times the height of the traces from the ground plane. So, if the dielectric thickness between the signal traces and the ground plane is 10 mils, then maintain the spacing between the traces at approximately 40 mils.
  - The ground plane should be the layer directly under the signal layer on which the differential traces are run. Furthermore, in order to provide a good signal return path and avoid signal impedance discontinuities, the ground plane should be continuous in the area under the signal traces. In addition, route the majority of a given differential signal trace on the single signal layer above the ground plane to minimize the via count in the route. If the signal traces do change planes, ensure that there is no discontinuity in the ground return path by coupling the new power plane over which the signal trace is routed with the ground plane in close vicinity to the signal via. If the same ground plane is used, then place some vias connecting the two ground planes in close proximity (100 mils) to the signal via.
  - Differential pair traces must be the same length electrically so as not to introduce any skew between the differential signals. This is achieved by routing the two traces in each differential pair along the same path (adhering to the above spacings) and maintaining the same via count for each trace. The two traces within a pair should have matched lengths within approximately 50 mils of one anther. Furthermore, the lengths of the four traces within the two sets of differential pairs (TPA & TPB) in a given port should be kept within 100mils of one another. Each port, however, can be wired independently within these guidelines since there aren't any restrictions on trace variations from port to port.
- Transceiver signal routes should be routed from the 1394 connector to the PHY module pin and 55ohm terminator minimizing the stub length between the PHY module pins and terminator pins. Thus, the 55ohm terminators should be as close to the PHY as possible.
- Keep the TpBias traces from the PHY I/O to the filter capacitors short and wide to minimize delta I noise.
- Minimize interconnect signal trace length differences between the PHY and Link modules.
- In general, keep routes between the PHY and Link short and direct. Traces longer than 1.5 inches should be considered as transmissions lines and analyzed accordingly.

  Critical line length = $\frac{Vp \times tr}{2.5}$

  where tr = signal rise time in nsec
  and Vp = propagation velocity in unit length per nsec
- Place the 3.6Kohm external current setting resistor that is connected to PHY pins 21 & 22 as close to the pins as possible.
- Place the 0.1µF external PLL filter capacitor that is connected to PHY pins 35 & 36 as close to the pins as possible.
- As a general rule, each power pin on the PHY and Link modules should be capacitively decoupled with alternating 0.1 and 0.01µF ceramic capacitors to help reduce EMI emissions.
- As a general rule, each module power and ground pin should be connected directly to its appropriate power plane (i.e. do not float any of the power pins or run wires to connect to the power plane).
- The PHY should have its own ground plane which connects to Vg of the 1394 connector.
- When adding a via to TPA or TPB traces, ensure a 50 mil annular clearance (spacing from via barrel to solid GND/Power plane space).
- TpBias should have a 1.0µF ceramic capacitor.

References

1. IEEE Standard 1394-1995, IEEE Standard for a High Performance Serial Bus.
2. IEEE P1394a, Draft Standard for High Performance Serial Bus (Supplement), Draft Revision 2.0.

Revision Log

Revision	Contents Of Modification
5/19/98	Initial Release
6/22/98	First revision. • Corrected part numbers by switching the three-port part number for the one-port part number in Overview and Ordering Information. • Corrected graphic errors in the External Component Connections diagram: - Clarified connections of pins 75 and 76 - Corrected details of pins 37, 38, 39, and 80.
11/24/98	Second revision (02). In the Capacitive Isolation Barrier Circuit, updated resistor values and added Sclk circuit detail (page 13). Changed LPS pin type from CMOS to Hysteresis (page 9).

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