M5M44258BP,J,L-7,-8,-10

STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 262144-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of triple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

In addition to the $\overline{RAS}$-only refresh mode, the hidden refresh mode and $\overline{CS}$ before $\overline{RAS}$ refresh mode are available.

FEATURES

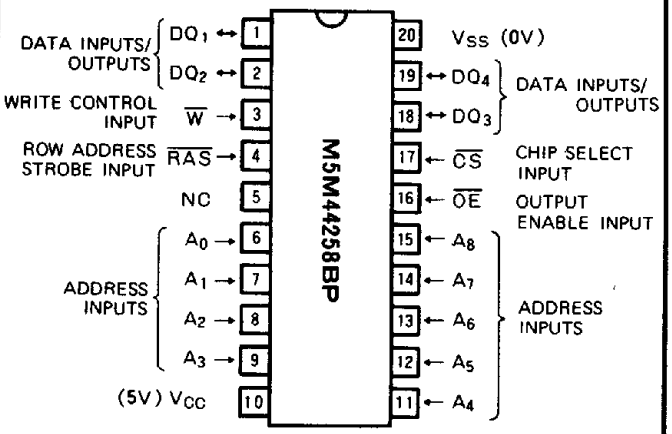
Type name	$\overline{RAS}$ access time (max ns)	$\overline{CS}$ access time (max ns)	Address access time (max ns)	$\overline{OE}$ access time (max ns)	Cycle time (min ns)	Power dissipation (typ mW)
M5M44258B-7	70	20	35	20	140	230
M5M44258B-8	80	20	40	20	160	200
M5M44258B-10	100	25	50	25	190	175

- High performance CMOS technology
- Standard 20 pin DIP, 26 pin SOJ, 20 pin ZIP
- Single 5V±10% supply
- Low stand-by power dissipation
  2.75mW (max) . . . . . CMOS Input level
- Low operating power dissipation
  M5M44258BP, J, L-7 . . . . . 440mW (max)
  M5M44258BP, J, L-8 . . . . . 385mW (max)
  M5M44258BP, J, L-10 . . . . . 330mW (max)
- All inputs, outputs TTL compatible and low capacitance
- Tri-state unlatched output
- 512 refresh cycles/8ms
- Early write mode and $\overline{OE}$ control output buffer impedance
- Read-Modify-write, $\overline{RAS}$-only refresh, Static column mode capabilities
- $\overline{CS}$ before $\overline{RAS}$ refresh mode capability
- $\overline{CS}$ controlled output allows hidden refresh
- Wide $\overline{RAS}$ pulse width for Static column mode . . . . . 50μs (max)

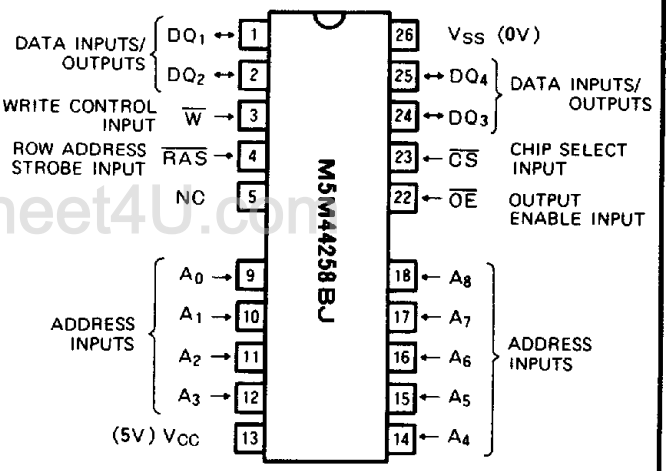
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

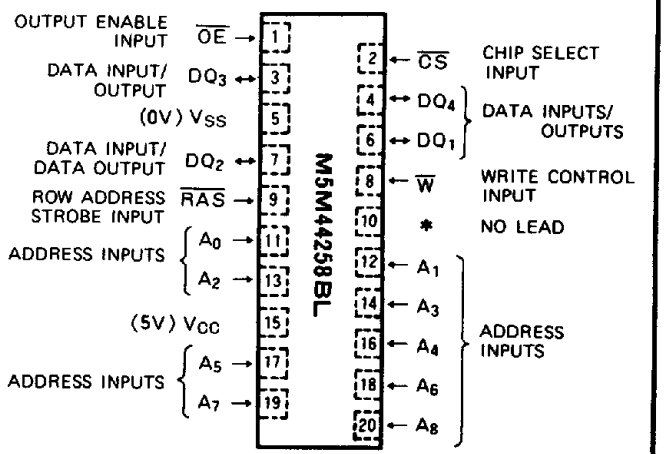
PIN CONFIGURATION (TOP VIEW)



Outline 20P4Y (DIP)



Outline 26P0J (SOJ)



Outline 20P5L-A(ZIP)

NC: NO CONNECTION

STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

FUNCTION

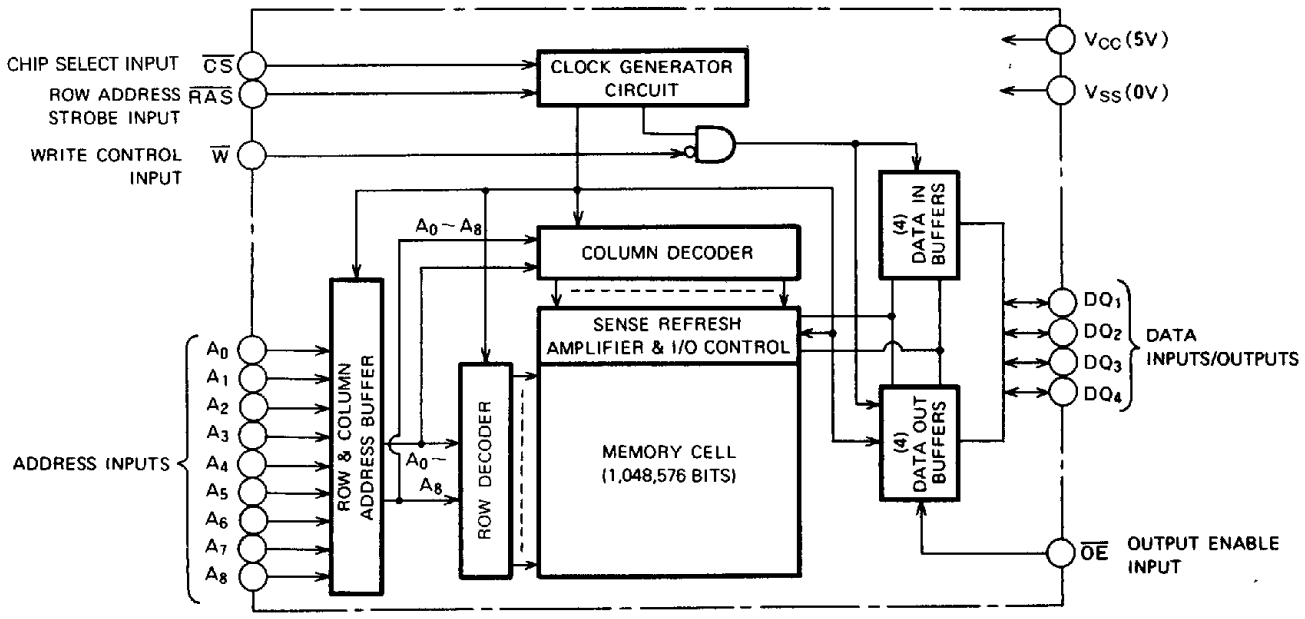
The M5M44258BP, J, L provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., static column mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Note
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Read-Modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note ACT active, NAC nonactive, DNC don't care, VLD valid, APD applied, OPN open
Static column mode is identical except early write

BLOCK DIAGRAM



STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		−65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low level input voltage, all inputs	−1.0		0.8	V

Note 1 All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off state output current		Q floating 0V≦V_{OUT}≦5.5V	−10		10	μA
I_I	Input current		0V≦V_{IH}≦6.5V, Other inputs pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 3, 4)	M5M44258B-7	$\overline{RAS}$, $\overline{CS}$ cycling $t_{RC}=t_{WC}$=min, output open			80	mA
		M5M44258B-8				70	
		M5M44258B-10				60	
$I_{CC2(AV)}$	Average supply current from V_{CC}, stand-by (Note 6)		$\overline{RAS}=\overline{CS}=V_{IH}$, output open			2	mA
			$\overline{RAS}=\overline{CS}=\overline{OE}$≧$V_{CC}$−0.5V, output open			0.5	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 3)	M5M44258B-7	$\overline{RAS}$ cycling, $\overline{CS}=V_{IH}$ t_{RC}=min, output open			80	mA
		M5M44258B-8				70	
		M5M44258B-10				60	
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44258B-7	$\overline{CS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min, output open			80	mA
		M5M44258B-8				70	
		M5M44258B-10				60	
$I_{CC7(AV)}$	Average supply current from V_{CC}, Static Column mode (Note 3, 4)	M5M44258B-7	$\overline{RAS}=V_{IL}$, Column address cycling t_{WSC}, t_{RSC}=min, output open			70	mA
		M5M44258B-8				60	
		M5M44258B-10				50	

Note 2 Current flowing into an IC is positive, out is negative
3 $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC6(AV)}$ and $I_{CC7(AV)}$ are dependent on cycle rate, maximum current is measured at the fastest cycle rate
4 $I_{CC1(AV)}$ and $I_{CC7(AV)}$ are dependent on output loading Specified values are obtained with the output open

CAPACITANCE (Ta=0~70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs (Note 5)	$V_I=V_{SS}$ f=1MHz Vi=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CS})}$	Input capacitance, $\overline{CS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

Note 5: $C_{I(A)}$ of ZIP is 6pF (max)

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 6)

Symbol	Parameter		Limits						Unit
			M5M44258B-7		M5M44258B-8		M5M44258B-10		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CS}$	(Note 7, 8)		20		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		70		80		100	ns
t_{CAA}	Column Address access time	(Note 7, 10)		35		40		50	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		20		20		25	ns
t_{PWA}	Access time from previous $\overline{W}$ low	(Note 7)		65		70		85	ns
t_{WRA}	Access time from $\overline{W}$ high	(Note 7)		35		40		50	ns
t_{CLZ}	Output low impedance time from $\overline{CS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CS}$ high	(Note 11)	0	20	0	20	0	25	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	(Note 11)	0	20	0	20	0	25	ns

Note 6 An initial pause of 500μs is required after power up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles before proper device operation is achieved
Note that $\overline{RAS}$ may be cycled during the initial pause And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved
7 Measured with a load circuit equivalent to 2TTL loads and 100pF
8 Assume that $t_{RCD} \geqq t_{RCD(max)}$, $t_{RAD} \leqq t_{RAD(max)}$
9 Assume that $t_{RCD} \leqq t_{RCD(max)}$, $t_{RAD} \leqq t_{RAD(max)}$ If t_{RCD} or t_{RAD} is greater than $t_{RCD(max)}$ or $t_{RAD(max)}$ then t_{RAC} will increase by the amount that t_{RCD} or t_{RAD} exceeds $t_{RCD(max)}$ or $t_{RAD(max)}$
10 Assume that $t_{RCD} - t_{RAD} \leqq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geqq t_{RCD(max)}$.
11 $t_{OFF(max)}$ and $t_{dis(OE)(max)}$ define the time at which the output achieves the high impedance state ($|I_{OUT}| \leqq |\pm 10\mu A|$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Static Column Mode Cycles) (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted, See notes 12, 13)

Symbol	Parameter		Limits						Unit
			M5M44258B-7		M5M44258B-8		M5M44258B-10		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		60		70		80		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CS}$ low	(Note 14)	20	50	25	60	25	75	ns
t_{CRP}	Delay time, $\overline{CS}$ high to $\overline{RAS}$ low	(Note 15)	10		10		10		ns
t_{CPN}	$\overline{CS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	35	20	40	20	50	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CS}$ low or $\overline{W}$ low		0		0		0		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		15		ns
t_{CAH}	Column address hold time after $\overline{CS}$ low or $\overline{W}$ low		15		20		20		ns
t_T	Transition time	(Note 17)	3	50	3	50	3	50	ns

Note 12 The timing requirements are assumed t_T = 5ns
13 $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals
14 $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC} If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled by exclusively t_{CAC} $t_{RCD(min)}$ is specified as $t_{RCD(min)} = t_{RAH(min)} + 2t_T + t_{ASC(min)}$
15 t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CS}$ cycles
16 $t_{RAD(max)}$ is specified as a reference point only If $t_{RAD} \geqq t_{RAD(max)}$, access time is assumed by t_{CAA} for read cycle
17 t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$

STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	80	10000	100	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	20		20		25		ns
t_{RCS}	Read setup time before $\overline{CS}$ low	0		0		0		ns
t_{RCH}	Read hold time after $\overline{CS}$ high (Note 18)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 18)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time	35		40		50		ns
t_{AH}	Column address hold time after $\overline{RAS}$ high	10		10		10		ns
t_{RPC}	Precharge to $\overline{CS}$ active time	0		0		0		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CS}$ low	20		20		25		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low	0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	15		15		20		ns
$t_{h(OECH)}$	$\overline{CS}$ hold time after $\overline{OE}$ low	20		20		25		ns
$t_{h(OERH)}$	$\overline{RAS}$ hold time after $\overline{OE}$ low	20		20		25		ns

Note 18 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width	70	10000	80	10000	100	10000	ns
t_{CS}	$\overline{CS}$ low pulse width	20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low	70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	20		20		25		ns
t_{CWL}	$\overline{CS}$ hold time after write low	20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write low	20		20		25		ns
t_{WH}	Write command hold time for output disable	0		0		0		ns
t_{WCS}	Write setup time before $\overline{CS}$ low (Note 20)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CS}$ low	15		15		20		ns
t_{AH}	Column address hold time after $\overline{RAS}$ high	10		10		10		ns
t_{WP}	Write pulse width	15		15		20		ns
t_{DS}	Data setup time	0		0		0		ns
t_{DH}	Data hold time after $\overline{CS}$ low	15		15		20		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data	15		15		20		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low	15		15		20		ns

STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44258B-7		M5M44258B-8		M5M44258B-10		
			Min	Max	Min	Max	Min	Max	
t_{RWC}	Read-write/read-modify-write cycle time	(Note 19)	185		205		245		ns
t_{RAS}	$\overline{RAS}$ low pulse width		115	10000	125	10000	155	10000	ns
t_{CS}	$\overline{CS}$ low pulse width		65	10000	65	10000	80	10000	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RAS}$ low		115		125		155		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low		65		65		80		ns
t_{RCS}	Read setup time before $\overline{CS}$ low		0		0		0		ns
t_{CWD}	Delay time, $\overline{CS}$ low to write low	(Note 20)	40		40		50		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to write low	(Note 20)	90		100		125		ns
t_{CWL}	$\overline{CS}$ hold time after write low		20		20		25		ns
t_{RWL}	$\overline{RAS}$ hold time after write low		20		20		25		ns
t_{WP}	Write pulse width		15		15		20		ns
t_{DS}	Data setup time		0		0		0		ns
t_{DH}	Data hold time after write low		15		15		20		ns
t_{AWD}	Delay time, address to write low	(Note 20)	55		60		75		ns
$t_{h(CLOE)}$	$\overline{OE}$ hold time after $\overline{CS}$ low		20		20		25		ns
$t_{h(RLOE)}$	$\overline{OE}$ hold time after $\overline{RAS}$ low		70		80		100		ns
t_{DOEL}	Delay time, Data to $\overline{OE}$ low		0		0		0		ns
t_{OEHD}	Delay time, $\overline{OE}$ high to Data		15		15		20		ns
$t_{h(WOE)}$	$\overline{OE}$ hold time after write low		15		15		20		ns

Note 19 t_{RWC} is specified as $t_{RWC(min)} = t_{RAC(max)} + t_{OEHD(min)} + t_{RWL(min)} + t_{RP(min)} + 4t_T$

20 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are specified as reference points only If $t_{WCS} \geqq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle If $t_{CWD} \geqq t_{CWD(min)}$, $t_{RWD} \geqq t_{RWD(min)}$ and $t_{AWD} \geqq t_{AWD(min)}$, the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address If neither of the above conditions is satisfied, the condition of the DQ (at access time and until $\overline{CS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate

Static Column Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycles)

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t_{RSC}	SC read cycle time	40		45		55		ns
t_{WSC}	SC write cycle time	40		45		55		ns
t_{RWSC}	SC R/W, R/M/W, cycle time	90		95		115		ns
t_{RAS}	$\overline{RAS}$ low pulse width	110	50000	125	50000	155	50000	ns
t_{CS}	$\overline{CS}$ low pulse width	20	10000	20	10000	25	10000	ns
t_{CP}	$\overline{CS}$ high pulse width	10		10		10		ns
t_{RSW}	Delay time, $\overline{RAS}$ to 2nd Write low	80		90		110		ns
t_{WI}	Write invalid time	10		10		10		ns
t_{PWH}	Column address hold time to previous $\overline{W}$ low	65		70		85		ns
t_{WH}	Write command hold time for output disable	0		0		0		ns
t_{AOH}	Data hold time from address change	10		10		10		ns
t_{WAD}	Delay time write to address change (Note 21)	20	30	20	30	25	35	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CS}$ low	20		20		25		ns
$t_{h(WHOE)}$	$\overline{OE}$ hold time after write high	45		50		60		ns

Note 21 $t_{WAD(max)}$ is specified as a reference point only If $t_{WAD} \geqq t_{WAD(max)}$, access time is assumed by t_{CAA}

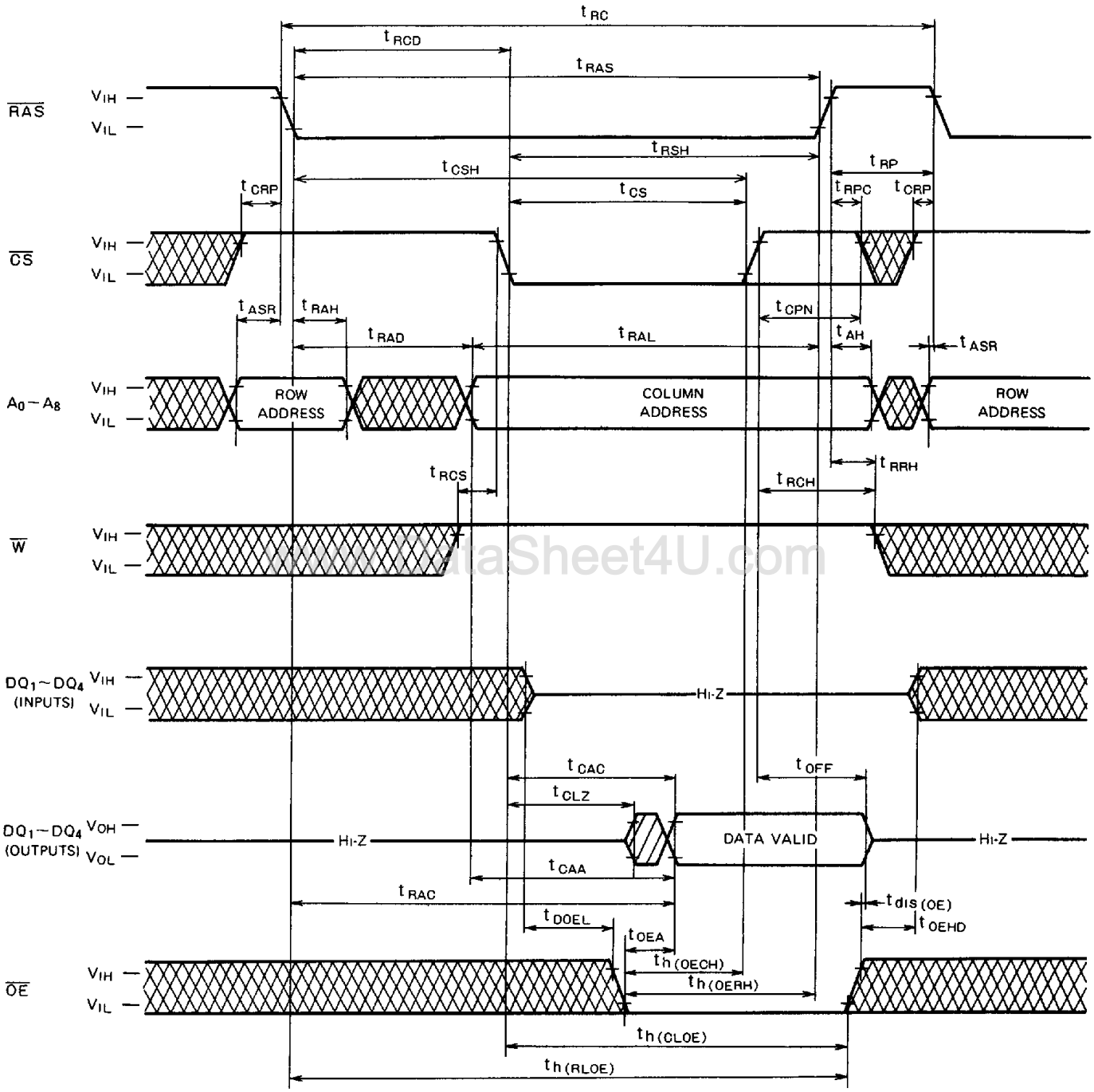
$\overline{CS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)

Symbol	Parameter	Limits						Unit
		M5M44258B-7		M5M44258B-8		M5M44258B-10		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh	15		15		20		ns
t_{RPC}	Precharge to $\overline{CS}$ active time	0		0		0		ns

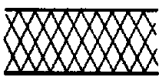
Note 22 Eight or more $\overline{CS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CS}$ before $\overline{RAS}$ refresh mode

Timing Diagrams (Note 23)

Read Cycle



Note 23

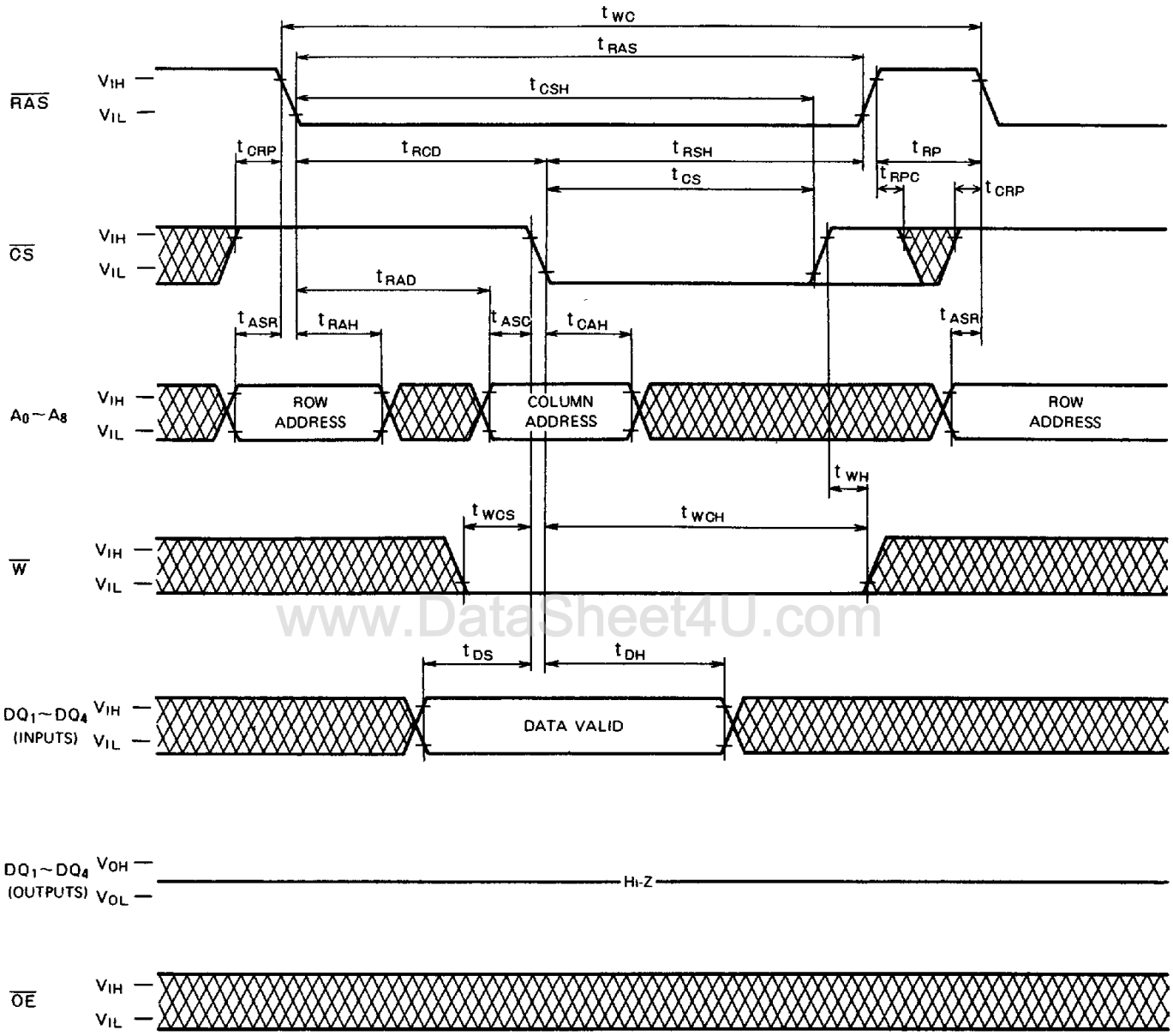


Indicates the invalid output.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

Indicates the invalid output

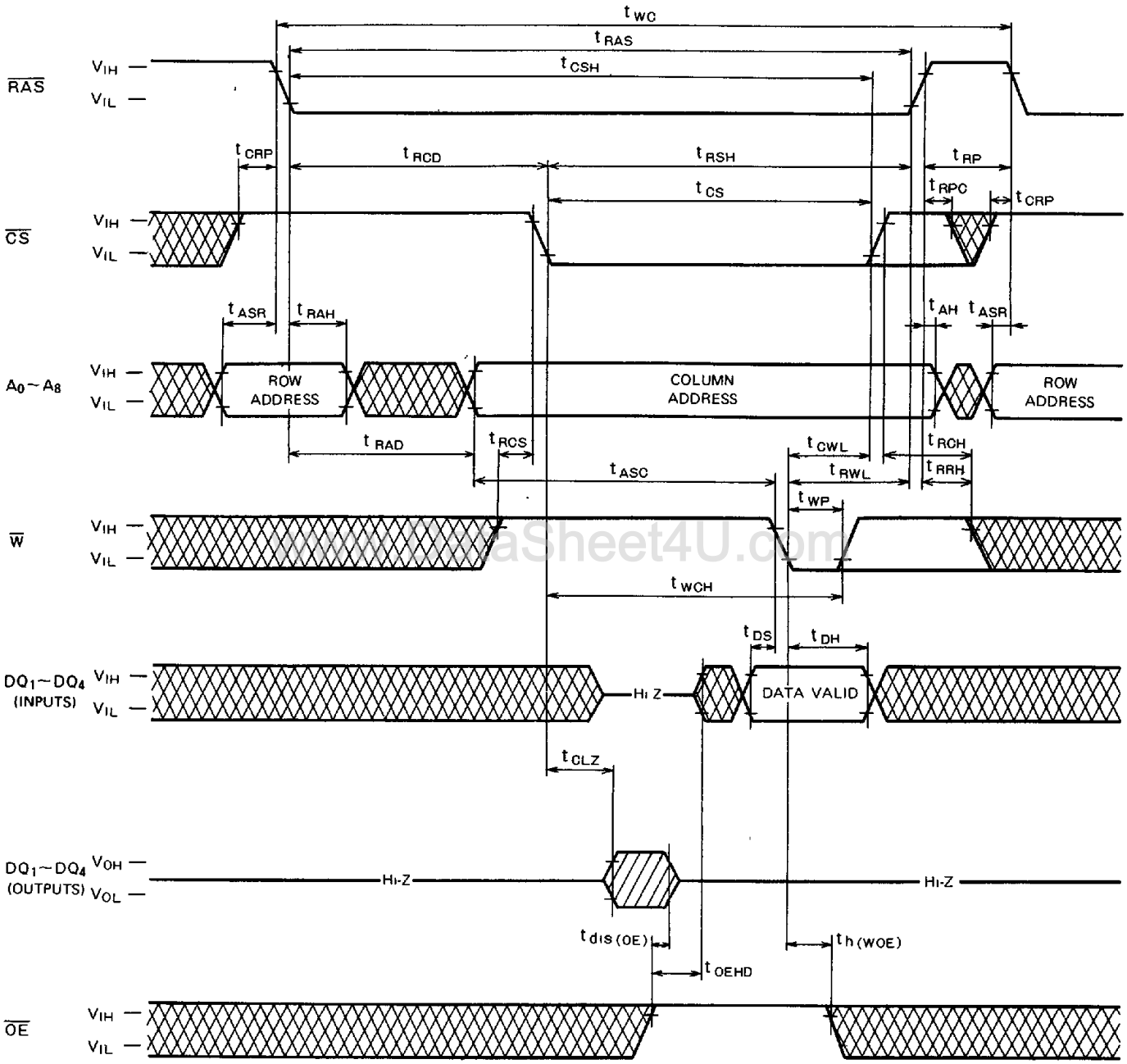
STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Write Cycle (Early write)



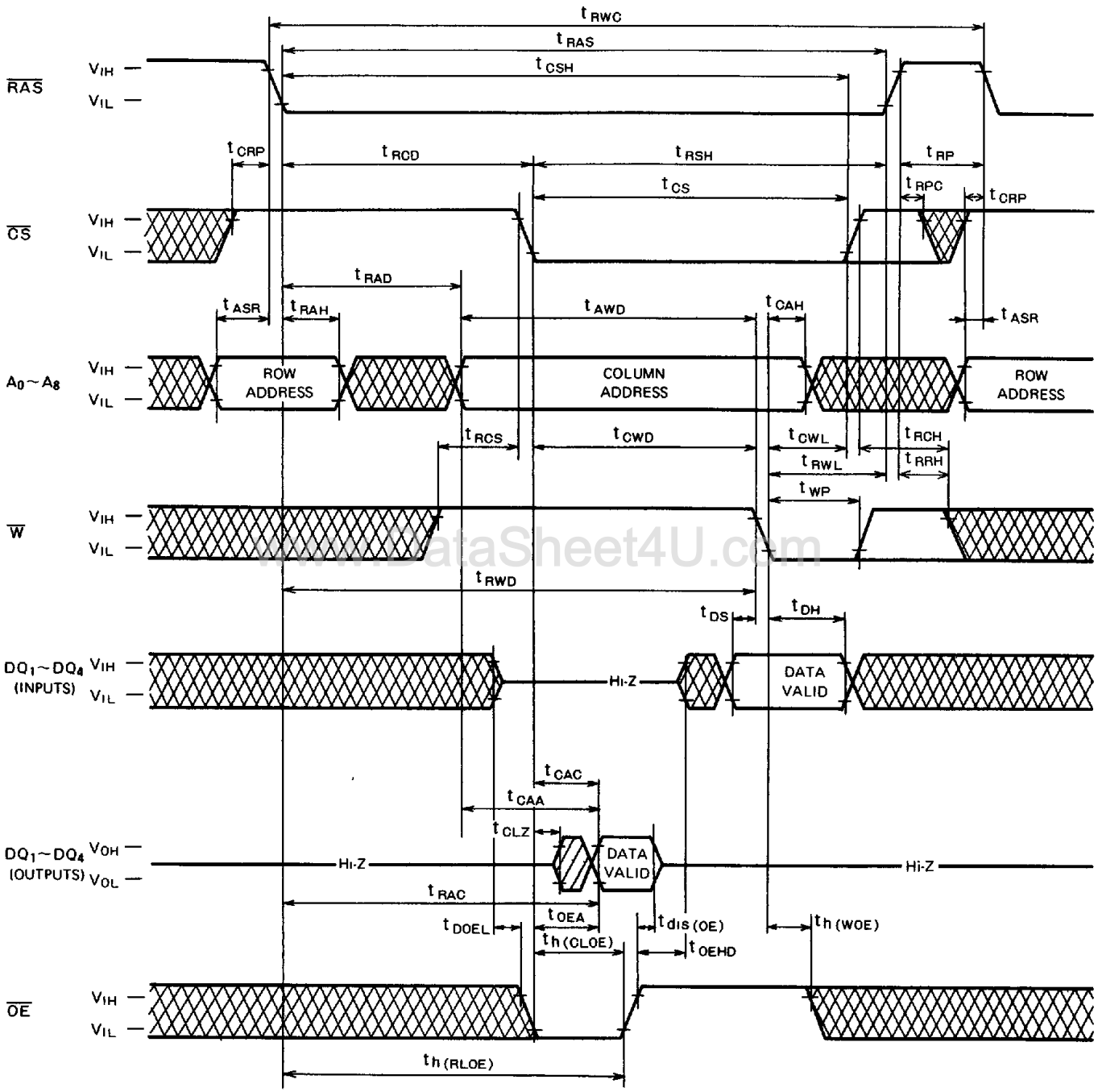
STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Write Cycle (Delayed Write)



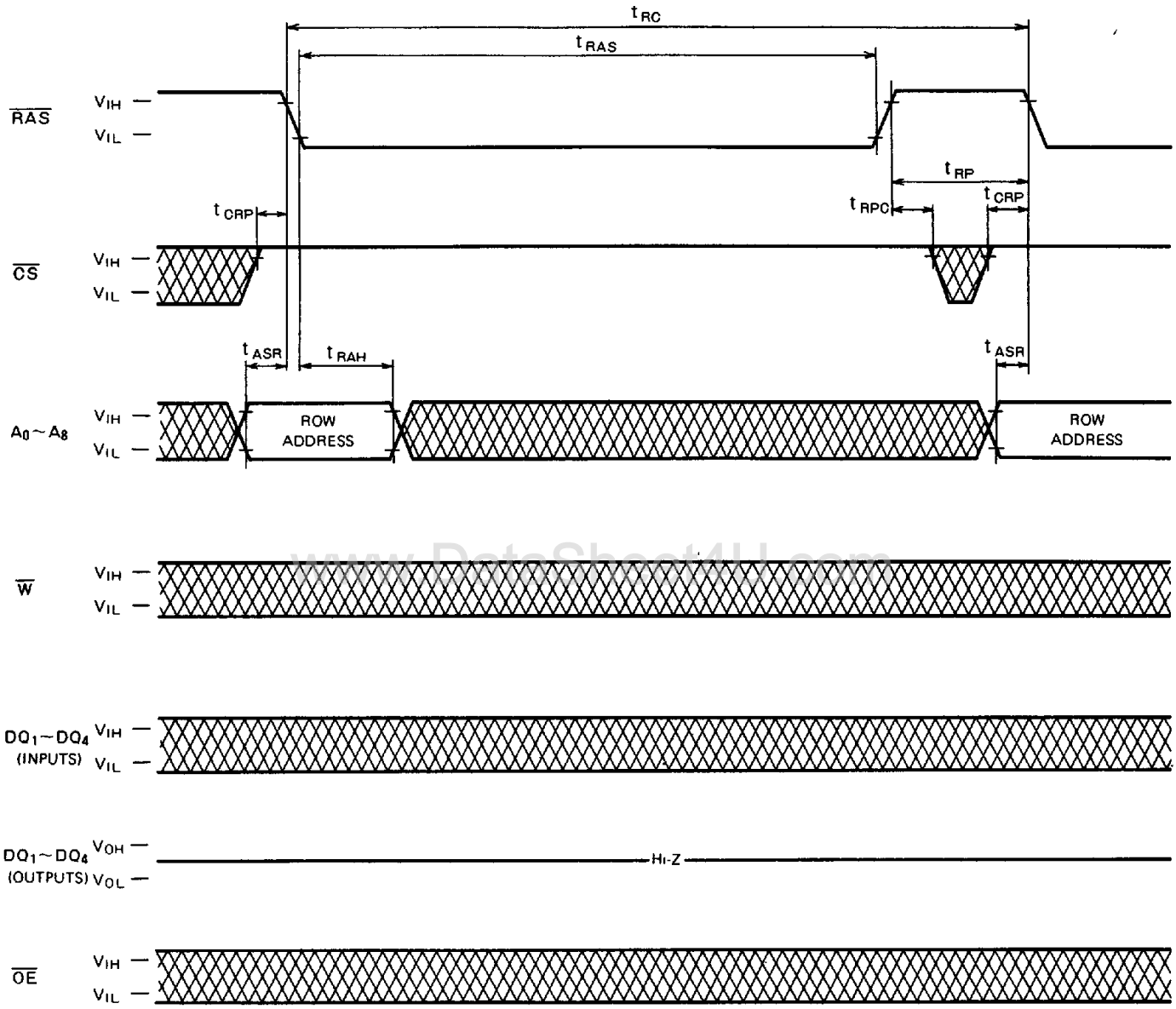
STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Read-Write, Read-Modify-Write Cycle

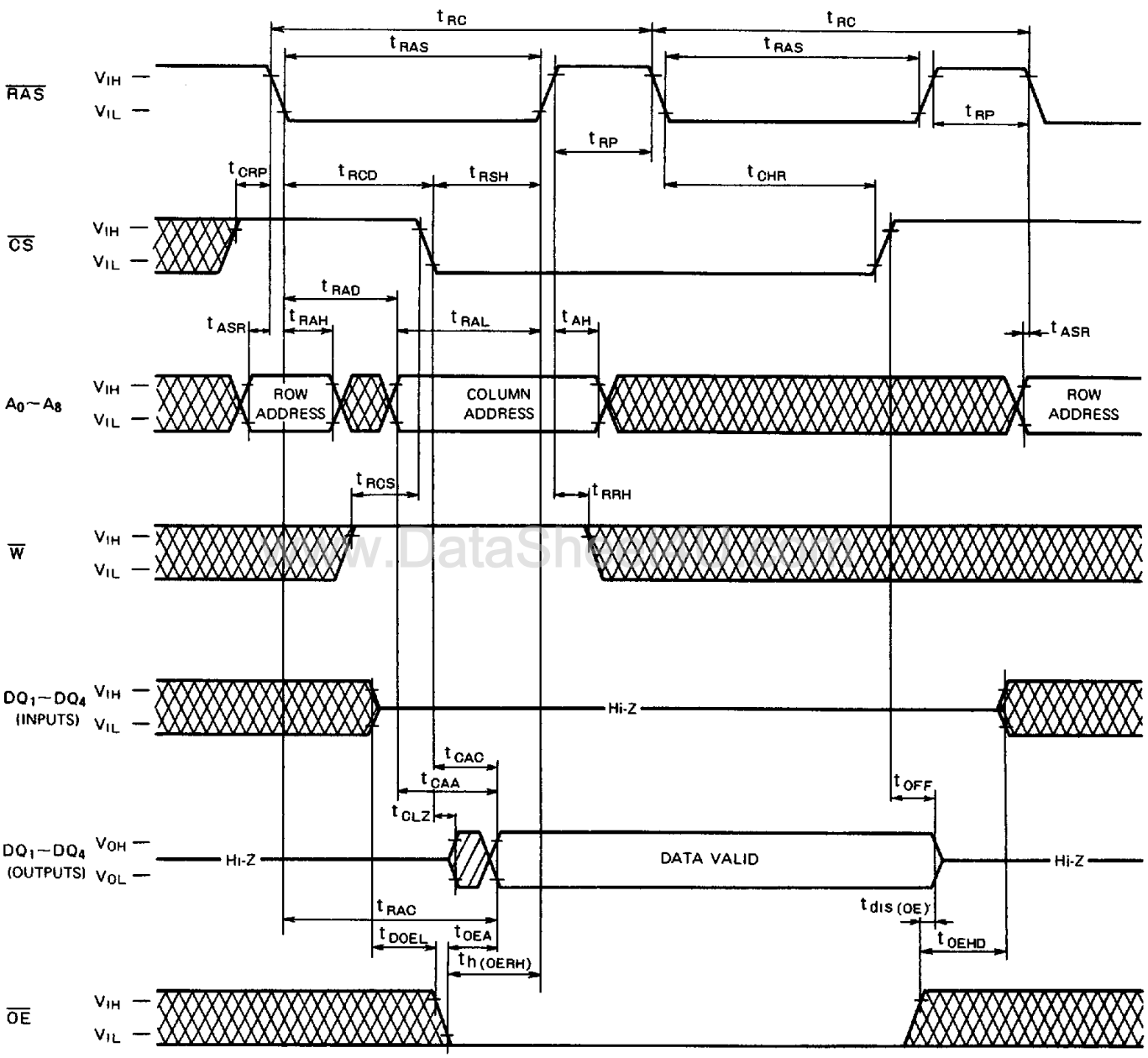


STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

$\overline{RAS}$-only Refresh Cycle



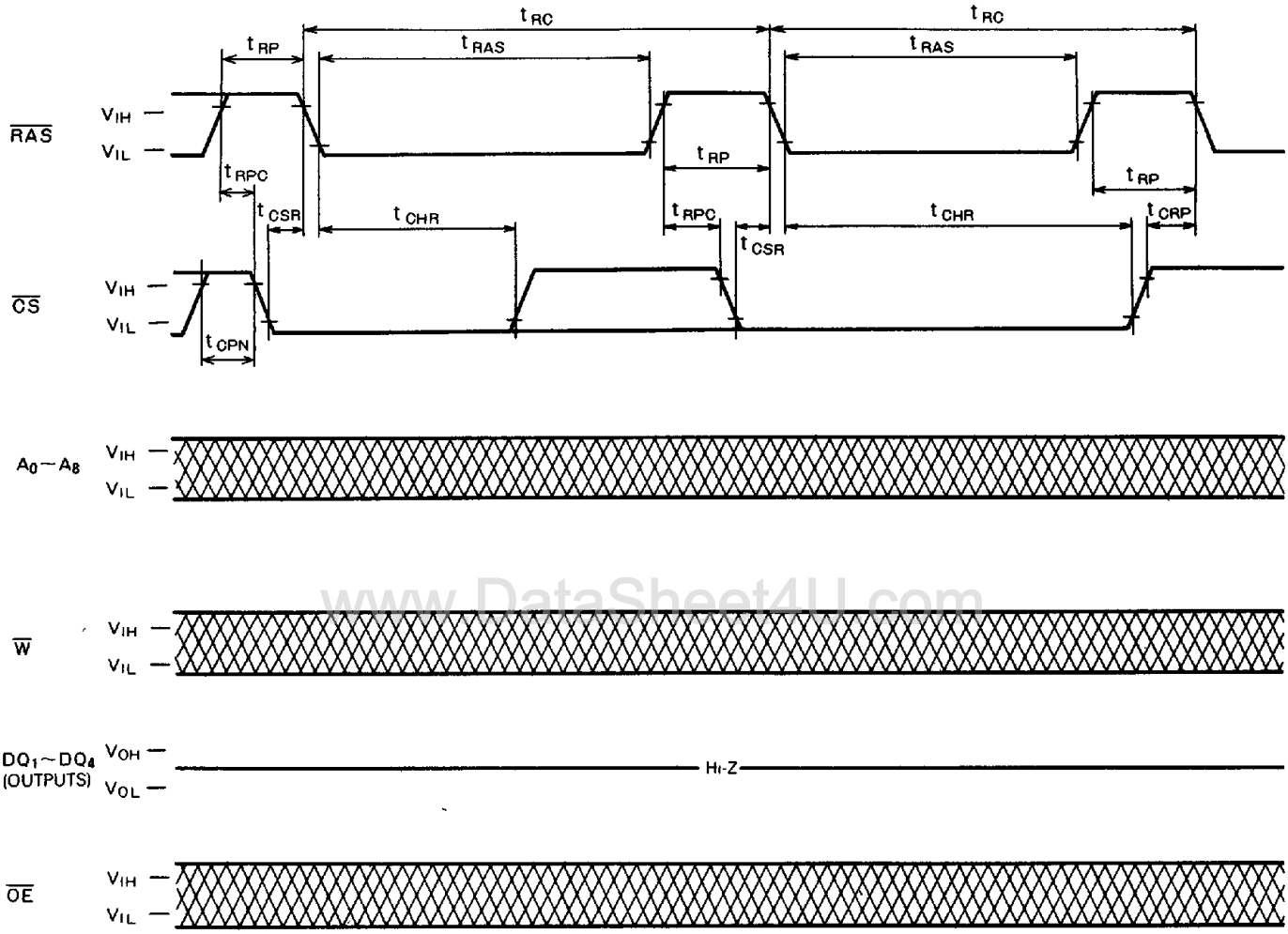
Hidden Refresh Cycle (Read) (Note 24)



Note 24. Early write, delayed write, read-write or read-modify-write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown before.

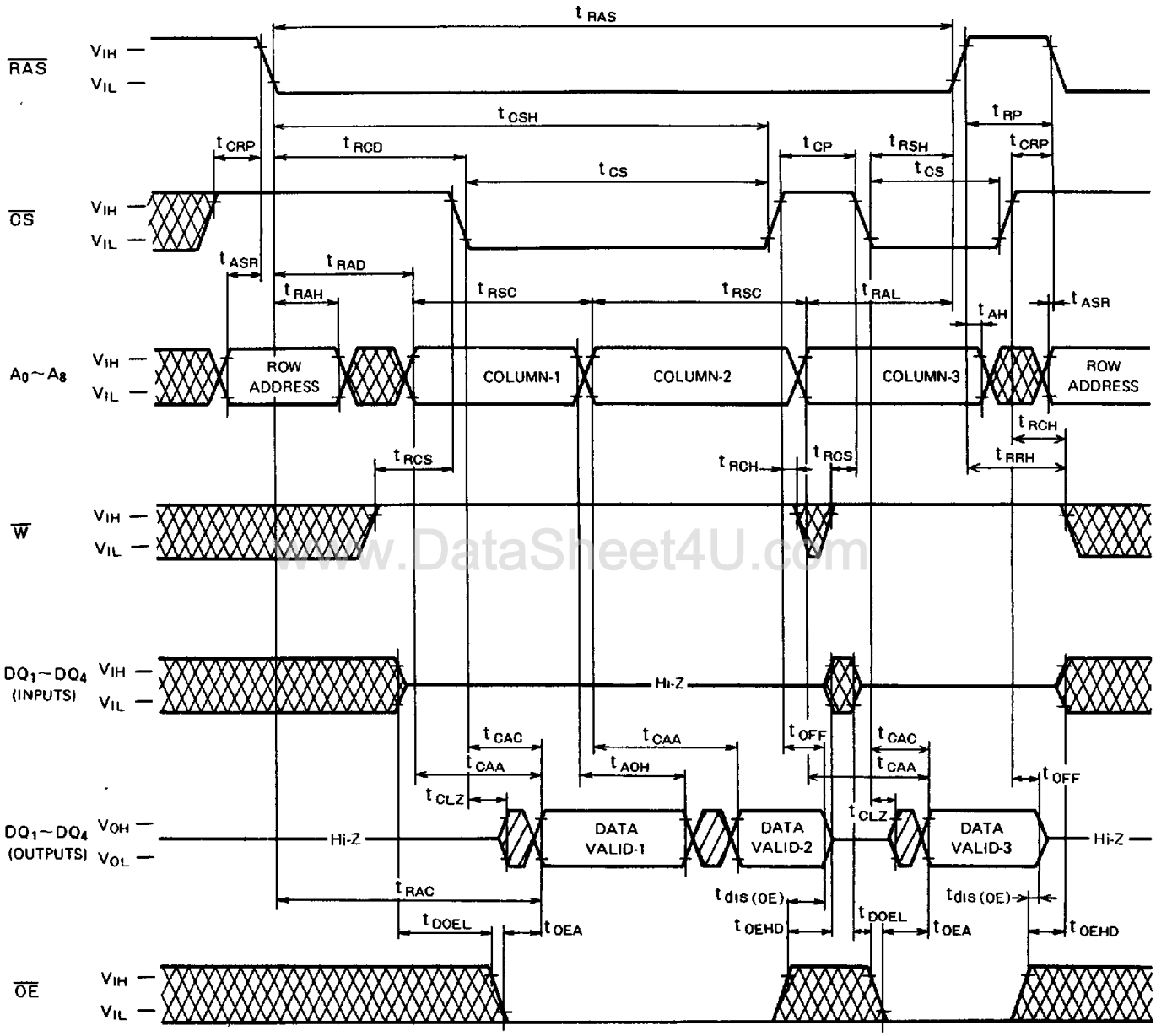
STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



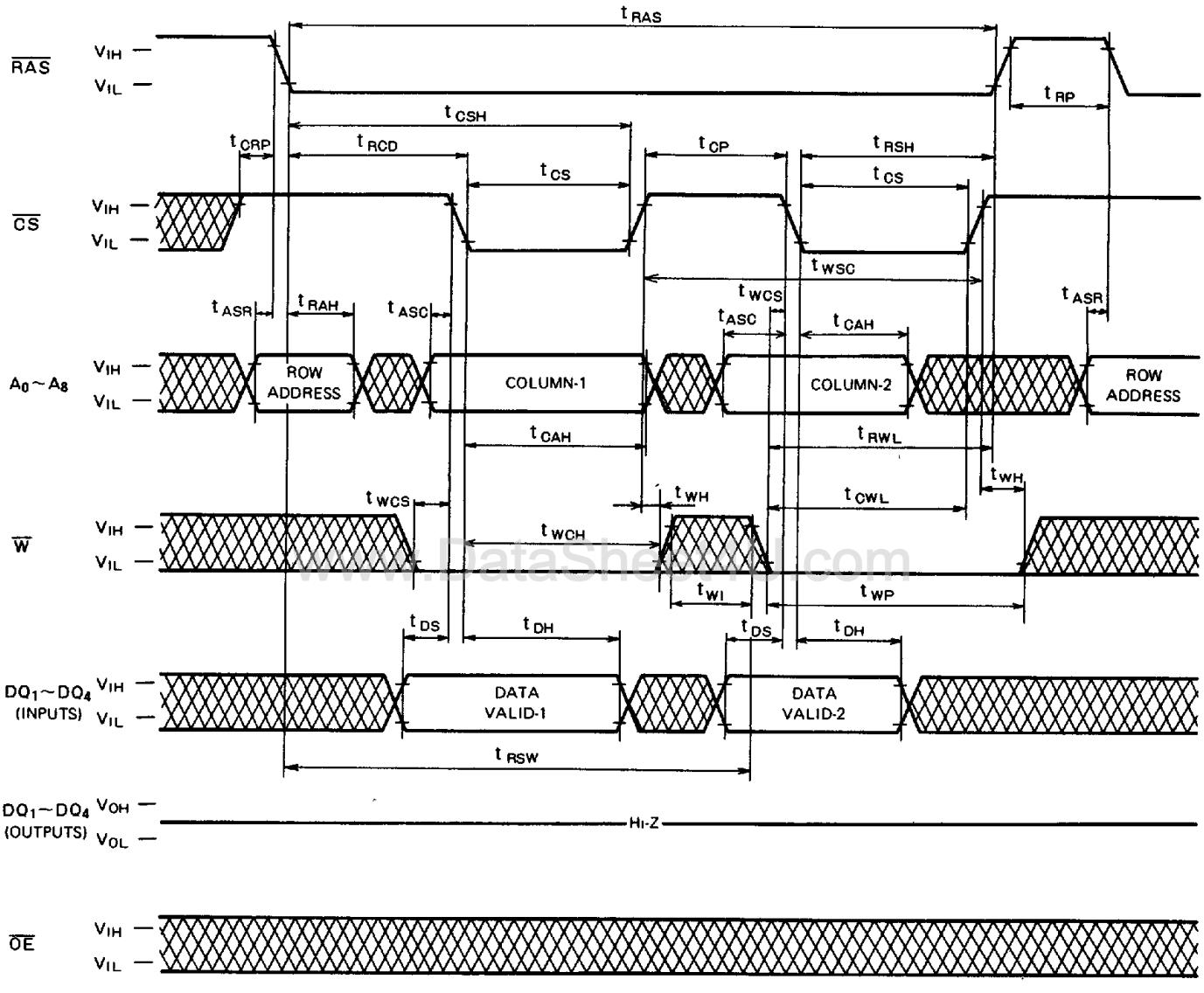
STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Static Column Mode Read Cycle



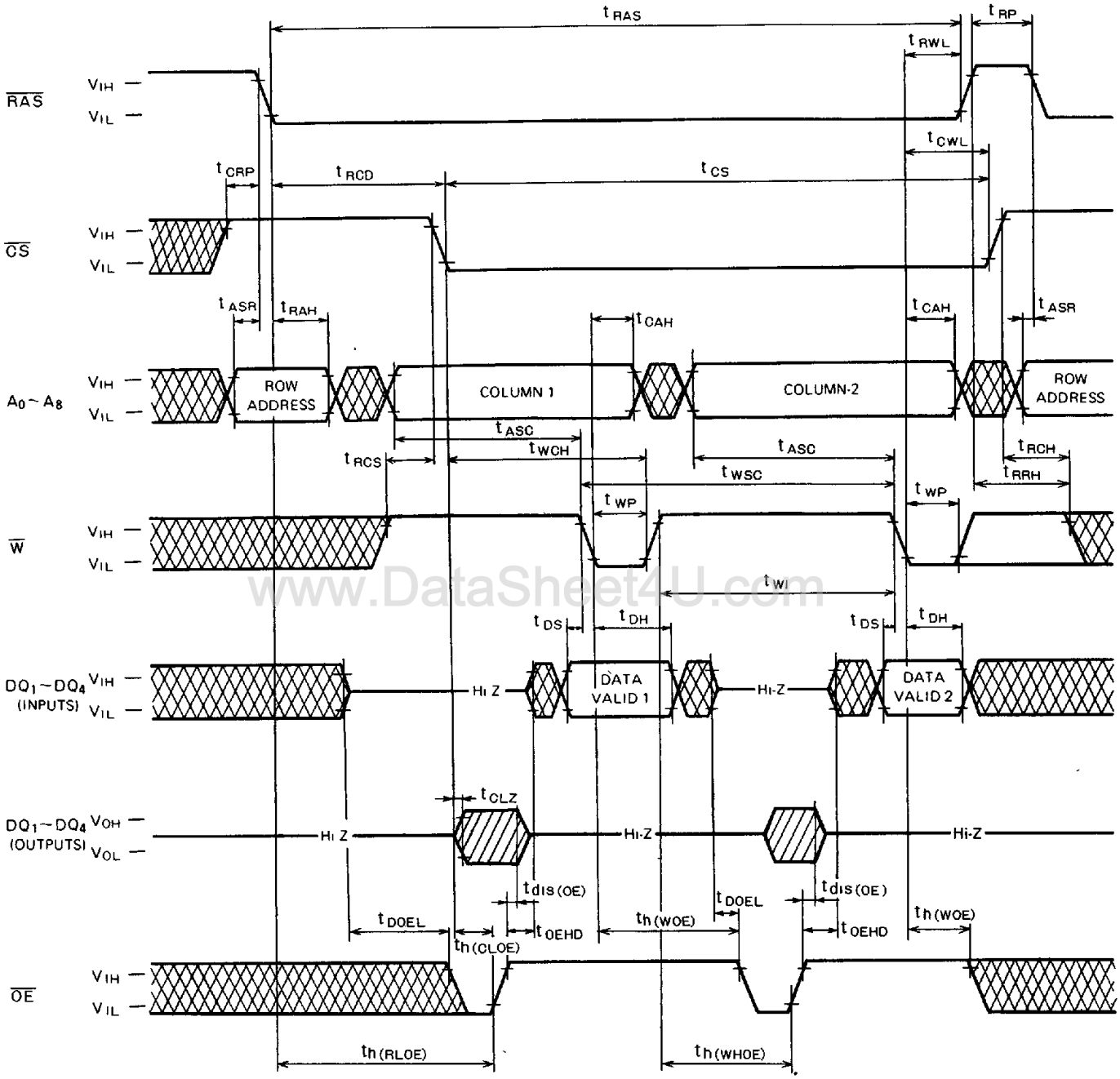
STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Static Column Mode Write Cycle (Early Write)



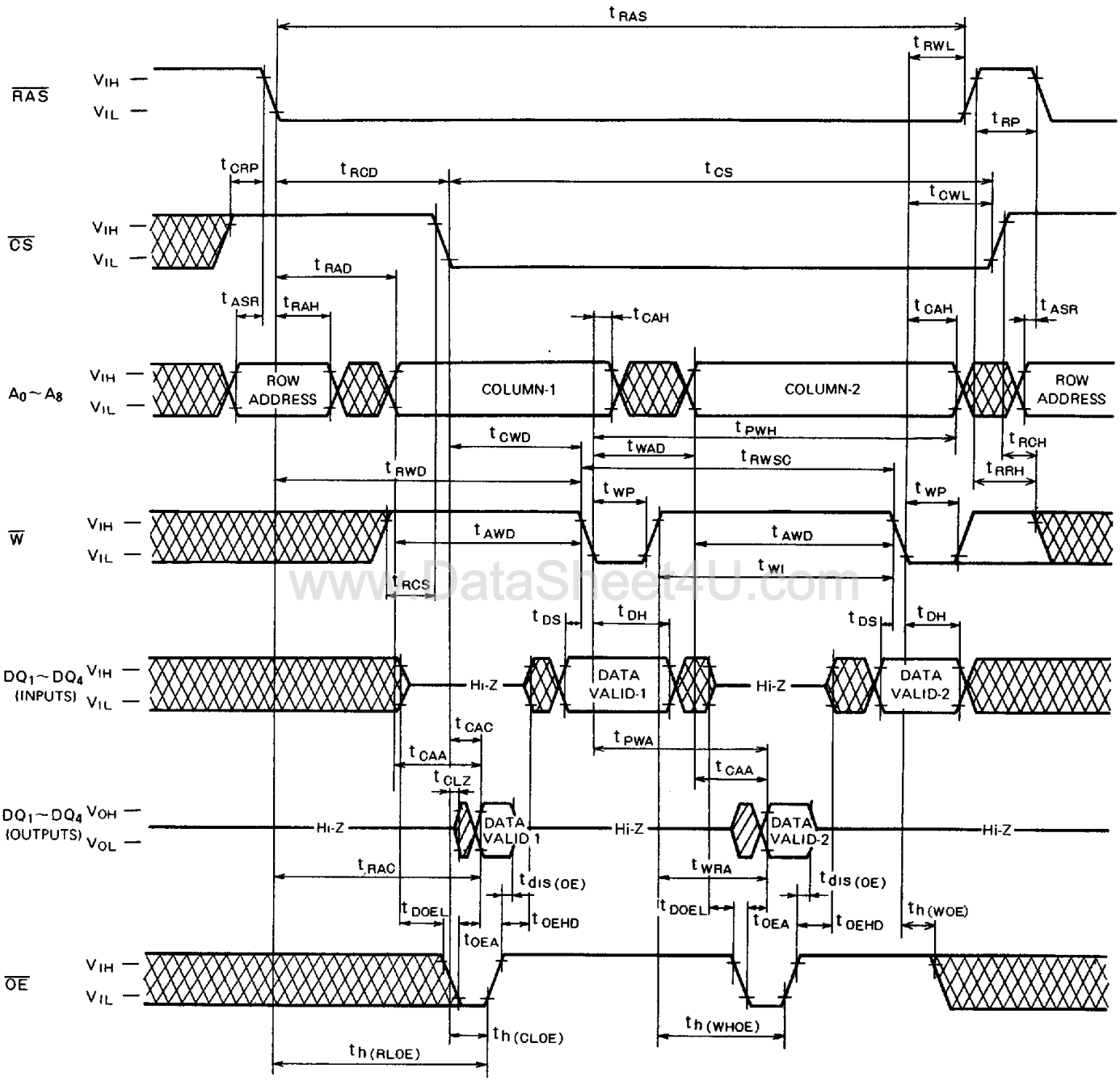
STATIC COLUMN MODE 1048576-BIT (262144-WORD BY 4-BIT) DYNAMIC RAM

Static Column Mode Write Cycle (Delayed Write)



STATIC COLUMN MODE 1048576-BIT(262144-WORD BY 4-BIT)DYNAMIC RAM

Static Column Mode Read-Write, Read-Modify-Write Cycle



STATIC COLUMN MODE 1048576-BIT (262144-WORD BY 4-BIT) DYNAMIC RAM

Static Column Mode Read-Write Mixed Cycle