CMOS DECADE COUNTER/7-SEGMENT DECODER/DRIVERS

FEATURES

- **Monolithic Construction of Bipolar Transistors on Outputs Allow Direct Display Drive**
- **Decade Counter and 7-Segment Decoder in One Package**
- **Direct Reset**
- **Display Enable Function (4426AB)**
- **Ripple Blanking and Lamp Test Functions (4433AB)**
- **Trigger from either Edge of Clock Input**
- **Carry Output for Cascading Stages**
- **Fully Static Operation - DC to 5MHz @ 10Vdc**

DESCRIPTION

These two devices each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving each stage in a numerical display. A "high" Reset signal clears the decade counter to its zero count. The counters have interchangeable Clock and Clock Enable lines for incrementing on either a positive-going or negative-going transition, respectively. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The Carry-Out (C_{OUT}) signal completes one cycle every ten clock input cycles and is used to directly clock the succeeding decade in a multi-decade counting chain.

4426AB

When the Display Enable is "low" the seven decoded outputs are forced off regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The Carry Out and ungated "C-segment" signals are not gated by the Display Enable and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

4433AB

The 4433AB has provisions for automatic blanking of the nonsignificant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight-digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the 4433AB associated with the most significant digit in the display to a "low-level" voltage and connecting the RBO terminal of that stage to the RBI terminal of the 4433AB in the next-lower significant position in the display. This procedure is continued for each succeeding 4433AB on the integer side of the display. On the fraction side of the display the RBI of the 4433AB associated with the least significant digit is connected to a "low level" voltage and the RBO of the 4433AB is connected to the RBI terminal of the 4433AB in the next more-significant-digit position. Again, this procedure is continued for all 4433AB on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a "high-level" voltage (instead of to the RBO of the next more-significant stage). For Example: optional zero - 0.7346.

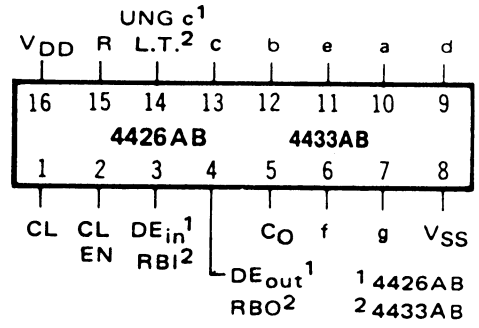
Likewise, the zero in a number such as 736.0 can be displayed by connecting the RBI of the 4433AB associated with it to a "high-level" voltage.

A "high" Lamp Test signal turns on all outputs.

BIPOLAR OUTPUTS

These devices are functionally and pin-for-pin interchangeable with all CMOS device types 4026AB and 4433AB. All counting and decoding in 4426AB and 4433AB devices is implemented with CMOS transistor circuitry. In order to furnish higher output drive for applications such as driving LED's, bipolar Darlington transistors have been furnished at each display drive output.

CONNECTION DIAGRAM
(all packages)



RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature C	T_A	-55 to +125	°C

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1, 3]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	15	–	0.2	20	–	600	
HIGH LEVEL OUTPUT VOLTAGE Decoded Outputs	V_{OH}	5	$V_{IN} = V_{SS}$ or V_{DD}	4.25	–	4.25	–	–	4.25	–	Vdc
		10		9.25	–	9.25	–	–	9.25	–	
		15	$\|I_O\| < 1\mu A$	14.25	–	14.25	–	–	14.25	–	
MINIMUM INPUT HIGH VOLTAGE	V_{IH}	5	$V_O = 0.5V$ or 4.25V	–	3.75	–	2.75	3.75	–	3.75	Vdc
		10	$V_O = 1.0V$ or 9.0V	–	7.5	–	5.5	7.5	–	7.5	
		15	$V_O = 1.5V$ or 13.5V	–	11.25	–	8.25	11.25	–	11.25	
			$\|I_O\| < 1\mu A$								
MAXIMUM INPUT LOW VOLTAGE	V_{IL}	5	$V_O = 0.5V$ or 4.25V	1.25	–	1.25	2.25	–	1.25	–	Vdc
		10	$V_O = 1.0V$ or 9.0V	2.5	–	2.5	4.5	–	7.5	–	
		15	$V_O = 1.5V$ or 13.5V	3.75	–	3.75	6.75	–	3.75	–	
			$\|I_O\| < 1\mu A$								
OUTPUT HIGH (SOURCE) CURRENT Decoded Outputs[3]	I_E	5	$V_{OH} = 2.5V$	–	–	-10	-25	–	–	–	mAdc
		10	$V_{OH} = 8.5V$	–	–	–	-60	–	–	–	
		15	$V_{OH} = 13.5V$	–	–	–	-100	–	–	–	
Carry Output	I_{OH}	5	$V_{OH} = 4.6V$	-0.10	–	-0.10	-0.4	–	-0.07	–	mAdc
		10	$V_{OH} = 9.5V$	-0.30	–	-0.30	-1.0	–	-0.20	–	
		15	$V_{OH} = 13.5V$	-0.90	–	-0.90	-4.0	–	-0.65	–	
			$V_{IN} = V_{SS}$ or V_{DD}								
Remaining Outputs		5	$V_{OH} = 4.6V$	-0.08	–	-0.08	-0.2	–	-0.06	–	mAdc
		10	$V_{OH} = 9.5V$	-0.20	–	-0.20	-0.5	–	-0.14	–	
		15	$V_{OH} = 13.5V$	-0.60	–	-0.60	-1.5	–	-0.42	–	
			$V_{IN} = V_{SS}$ or V_{DD}								
OUTPUT LOW (SINK) CURRENT	I_{OL}	5	$V_{OL} = 0.4V$	-0.10	–	-0.10	0.4	–	-0.07	–	mAdc
		10	$V_{OL} = 0.5V$	-0.30	–	-0.30	1.0	–	-0.20	–	
Carry Output		15	$V_{OL} = 1.5V$	-0.90	–	-0.90	4.0	–	-0.65	–	
			$V_{IN} = V_{SS}$ or V_{DD}								
Remaining Outputs		5	$V_{OL} = 0.4V$	0.13	–	-0.08	0.25	–	-0.06	–	mAdc
		10	$V_{OL} = 0.5V$	0.31	–	-0.20	0.6	–	-0.14	–	
		15	$V_{OL} = 1.5V$	1.43	–	-0.60	2.5	–	-0.42	–	
			$V_{IN} = V_{SS}$ or V_{DD}								

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

[2] $T_{LOW} = -55°C$ for C

$T_{HIGH} = +125°C$ for C

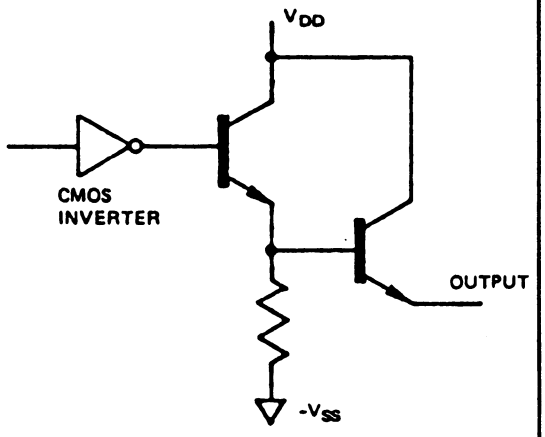
[3] Observe Package Power Dissipation rating.

ELECTRICAL CHARACTERISTICS

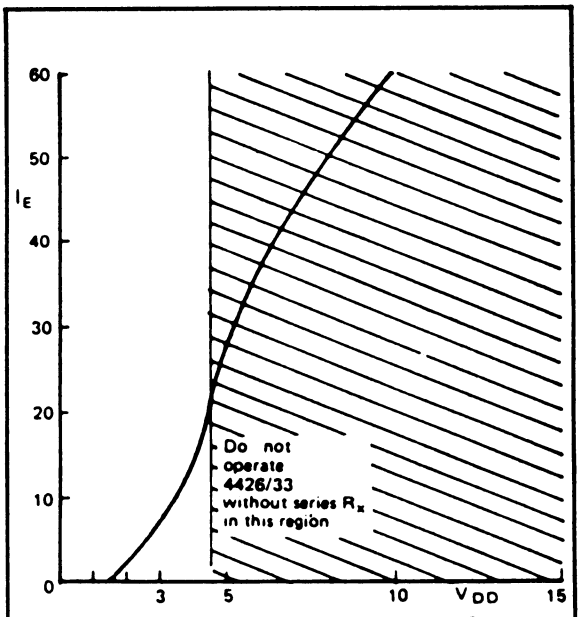
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME Clock to Decoded Outputs	t_{PLH}, t_{PHL}	5	–	850	1700	ns
		10	–	250	500	
		15	–	200	400	
Clock to Carry Out	t_{PLH}, t_{PHL}	5	–	500	1000	ns
		10	–	125	250	
		15	–	100	200	
OUTPUT TRANSITION TIME Decoded Outputs	t_{TLH}, t_{THL}	5	–	450	900	ns
		10	–	200	400	
		15	–	150	300	
Carry Output	t_{TLH}, t_{THL}	5	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
MINIMUM CLOCK OR ENABLE PULSE WIDTH	PW_{CL}, PW_{CE}	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	1.25	2.5	–	MHz
		10	2.5	5.0	–	
		15	3.0	6.0	–	
MAXIMUM CLOCK OR ENABLE RISE AND FALL TIME	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	3	–	–	
MINIMUM CLOCK OR ENABLE SETUP TIME	t_{setup}	5	–	250	500	ns
		10	–	100	200	
		15	–	80	160	
RESET OPERATION						
PROPAGATION DELAY TIME Reset to Decoded Outputs	t_{PLH}, t_{PHL}	5	–	700	1400	ns
		10	–	250	500	
		15	–	200	400	
Reset to Carry Output	t_{PLH}, t_{PHL}	5	–	500	1000	ns
		10	–	125	250	
		15	–	100	200	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	200	400	ns
		10	–	100	200	
		15	–	80	160	
RESET REMOVAL TIME	t_{rem}	5	–	375	750	ns
		10	–	150	300	
		15	–	125	250	

OUTPUT NETWORK

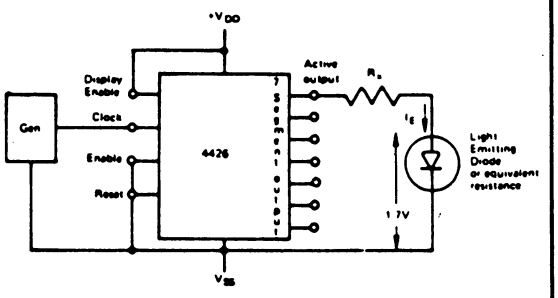


The darlington NPN transistor network shown is typical of each of seven segment drive outputs per integrated circuit.

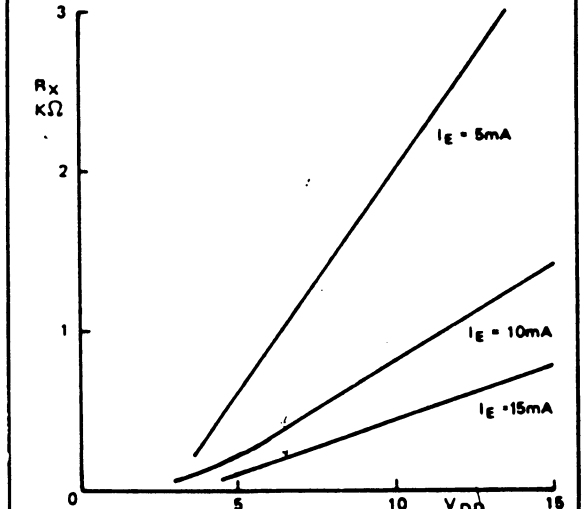


Typical Output Current per Segment vs. Supply Voltage.

DISPLAY INTERFACE

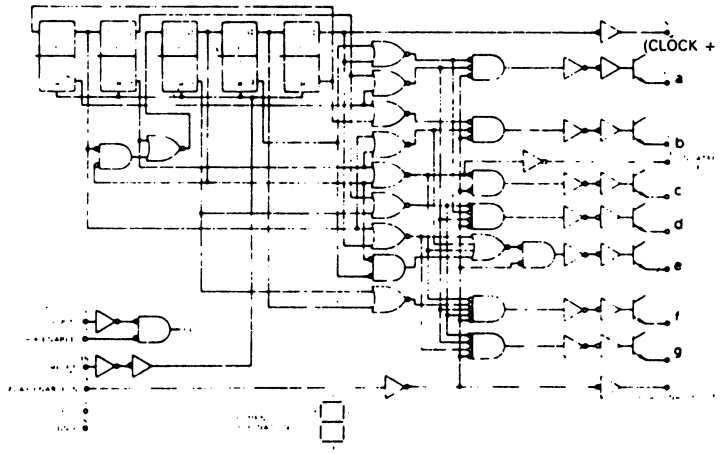


Typical Display Connection

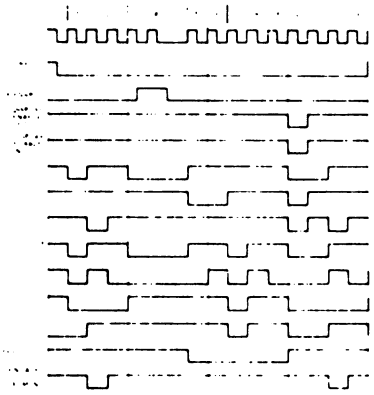


R_x required to limit LED Current

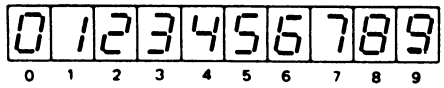
LOGIC DIAGRAM



TIMING DIAGRAM



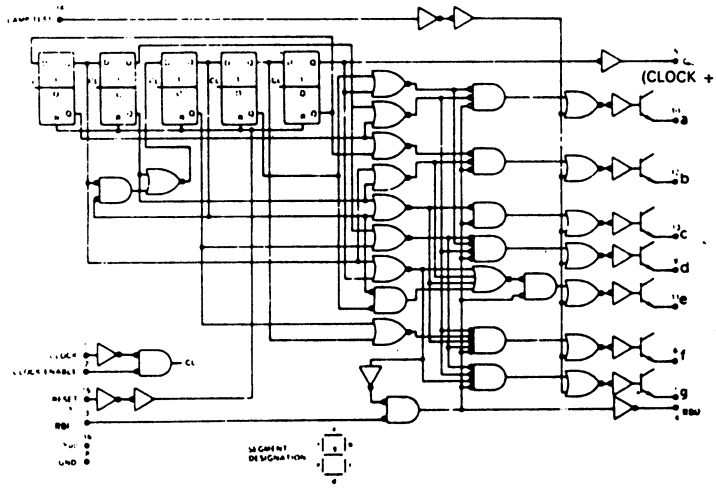
DISPLAY



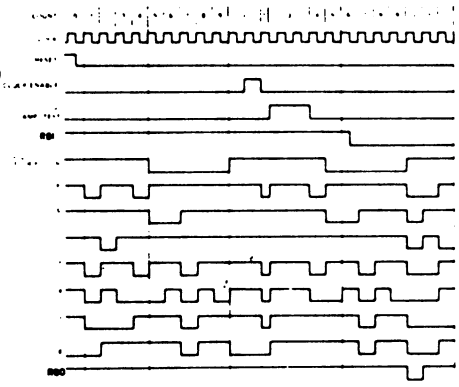
Collector of each output transistor internally tied to V_{DD}.

4426AB Decade Counter/7-Segment Decoder/Driver with Display Enable.

LOGIC DIAGRAM



TIMING DIAGRAM



DISPLAY



Collector of each output transistor internally tied to V_{DD}.

4433B Decade Counter/7-Segment Decoder/Driver with Ripple Blanking.