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AMENDENT HISTORY

Version	Date	Description
Ver 0.1	June 10, 2004	first issue
Ver 1.0	September 10, 2004	Added application circuit
Ver 1.1	November 1, 2004	Modify the 310 application circuit.
Ver 1.2	October 21, 2005	Modify Supply Voltage from Max 6V to Max 3.6V



1. INTRODUCTION

The SNR032 is a signal power, 32M-bit, read only memory. It is organized as 4M bytes, operates for single 3V power supply, support static standby mode. The SNR032 embedded two different interfaces, one is a standard 8-bit/16-bit interface bus which compatible with SNL310, another one is a special 8-bit AD (address/data) bus which compatible with SNC710.

SNR032 offers automatic power-down, with power-down controlled by the chip enable "CEB". When chip enable goes to high, SNR032 will entry power-down mode in order to save the power consumption.

2. FEATURES

- ◆ Power supply: 2.4V ~ 3.6V
- ◆ Memory Size: 32M-bit
- ◆ Totally static operation
- ◆ Embedded a standard 8-bit/16-bit bus interface compatible with SNL310 or a 8-bit AD (address/data) bus interface compatible with SNC710
- ◆ Access time: 200ns @3V

3. PIN ASSIGNMENTS

Symbol	IO	Standard Interface	AD Bus Interface
TYPE	I	Bus mode select pin "1"→AD bus "0" for 8-bit/16-bit interface	"1": AD bus mode "0": Standard mode
MODE	I	Bus mode select pin "0"→byte mode "1" word mode interface	-
A[21..8]	I	Standard ROM A[21..8]	-
A[[7]	I	Standard ROM A[7] / TESTM	TESTM
A[6]	I	Standard ROM A[6] / BS4 ~ BS2	BS4
A[5]	I	Standard ROM A[5] / BS4 ~ BS2	BS3
A[4]	I	Standard ROM A[4] / BS4 ~ BS2	BS2
A[3..2]	I	Standard ROM A[3..2]	-
A[1]	I	Standard ROM A[1]	ALECLK
A[0]	I	Standard ROM A[0]	READY
D[8..15]	I/O	Data bus D[8..15] (for word mode only)	-
D[0..7]	I/O	Data bus D[0..7]	AD-Bus D[0..7]
CEB	I	Chip enable pin	Chip enable pin
OEB	I	Output enable pin	-
VDD	P	Positive Power supply (3.3volt)	Positive Power supply (3.3volt)
GND	P	Negative Power supply (3.3volt)	Negative Power supply (3.3volt)

4. BUS INTERFACE

SNR032 provides three different bus modes to connect to host CPU, AD-bus mode, byte mode and word mode. And the switching between different modes is depended on the pin option “TYPE” and “MODE”. The following table is shown the relation ship of “TYPE”, “MODE” pins and mode switching.

Mode	TYPE pin	MODE pin
AD-Bus Interface	VDD	Don't care
Byte Mode Interface	GND	GND
Word Mode Interface	GND	VDD

4.1 AD-Bus Interface

For 8-bit AD (address/data) bus interface, all the address and data communication between SNC710 and SNR032 are through data bus D[0..7]. SNC710 allows user to connect maximum 2 external mask ROM. The option pin “TYPE” must connected to VDD then the AD-bus interface to be enable. In AD-Bus mode, SNR032 has three bank select pins BS2~BS4 to specify the memory region of SNR032. The address region setting of SNR032 is shown as bellow.

BS4~BS2	Address Region
001	0x0200000 ~ 0x03FFFFFF
010	0x0400000 ~ 0x05FFFFFF
011	0x0600000 ~ 0x07FFFFFF
100	0x0800000 ~ 0x09FFFFFF
101	0x0A00000 ~ 0x0BFFFFFF
110	0x0C00000 ~ 0x0DFFFFFF
111	0x0E00000 ~ 0x0FFFFFFF

Table-1

Note: For the address region 0x00000~0x01FFFFFF are reserved, so the setting of bank select pins BS4~BS2 CAN'T be the range 0000~0x0011.



5. ABSOLUTE MAXIMUM RATINGS

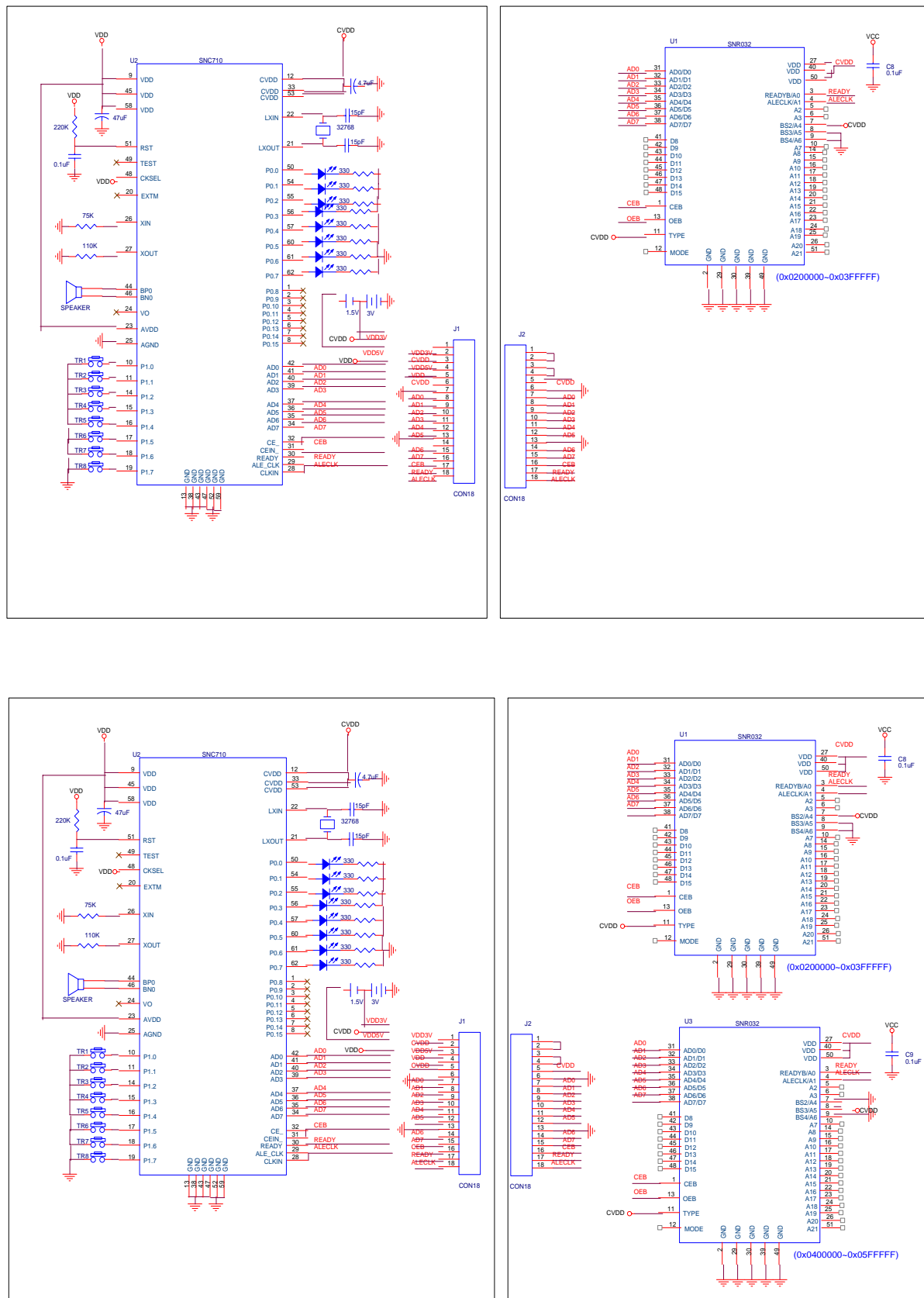
Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD-V}	-0.3	3.6	V
Input Voltage	V_{IN}	GND-0.3	$V_{DD}+0.3$	V
Operating Temperature	T_{OP}	0	55	°C
Storage Temperature	T_{STG}	-55.0	125.0	°C

6. ELECTRICAL CHARACTERISTICS

Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	-	3.6	V	
Standby current	I_{SBY}	-	1.5	2.0	uA	$V_{DD}=3V$, no load
Operating Current	I_{OPR}	-	4	-	mA	$V_{DD}=3V$, no load
Address access time	tAA	-	-	150	ns	Vdd=3V

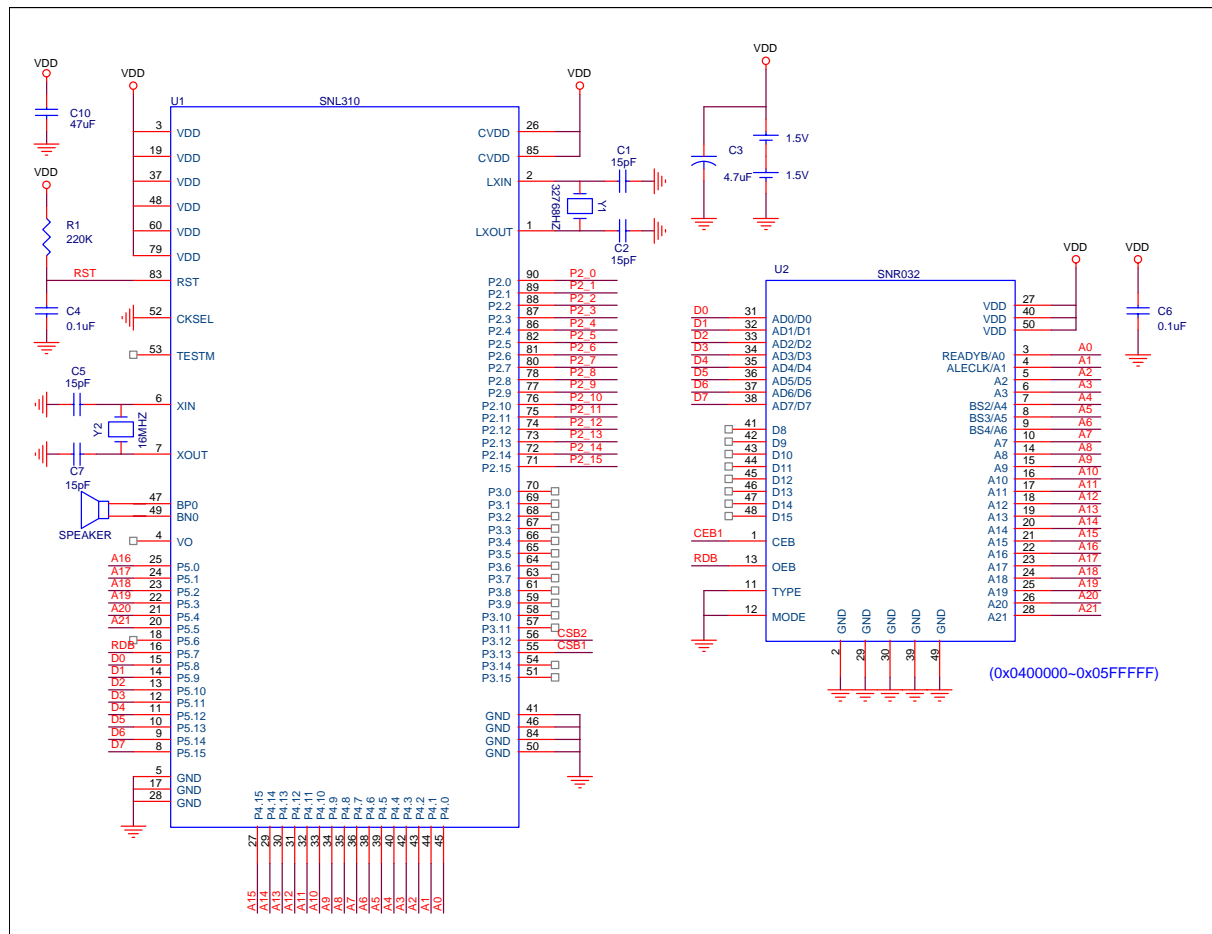


7.1 AD Bus Interface (with SNC710)





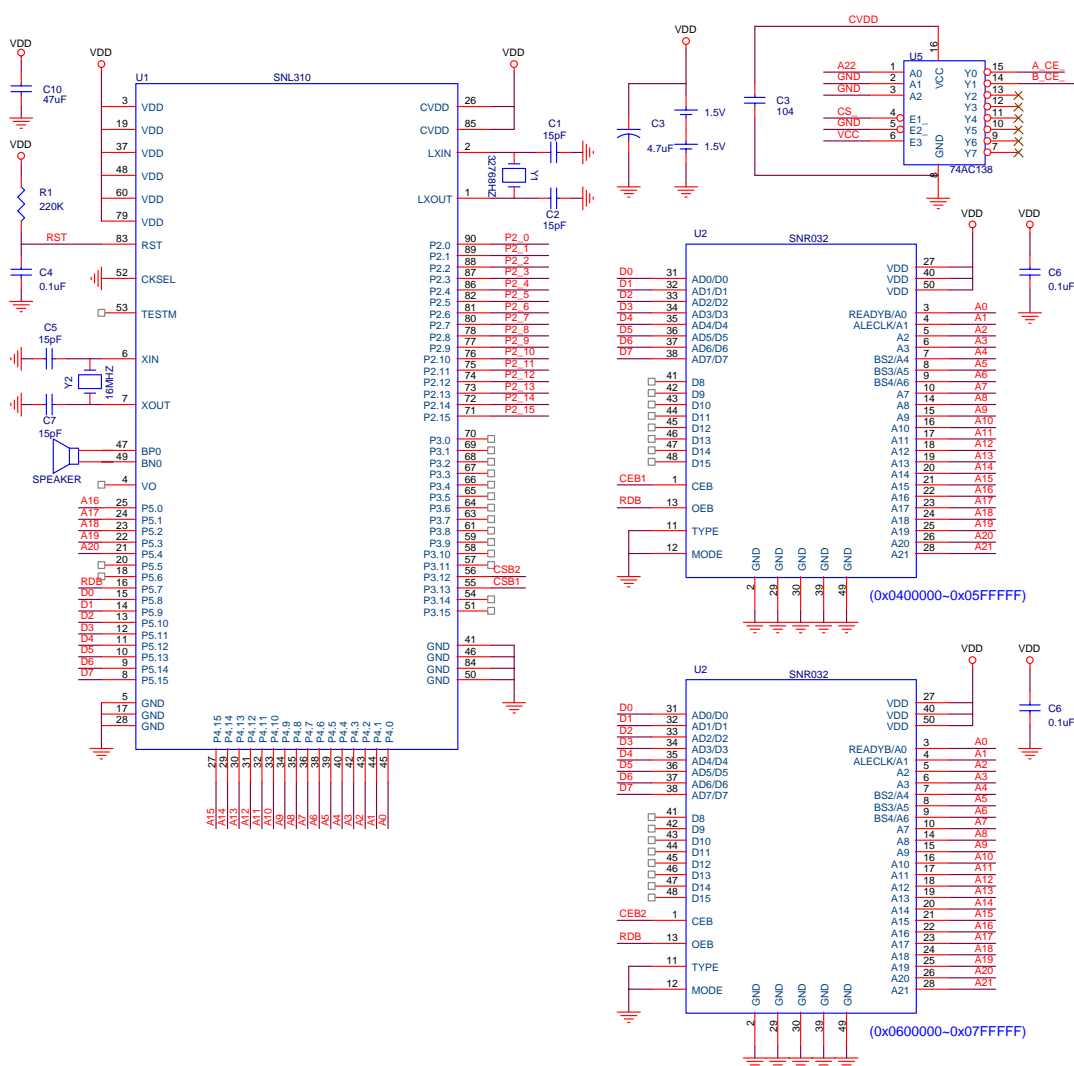
7.2 Standard ROM interface (with SNL310)





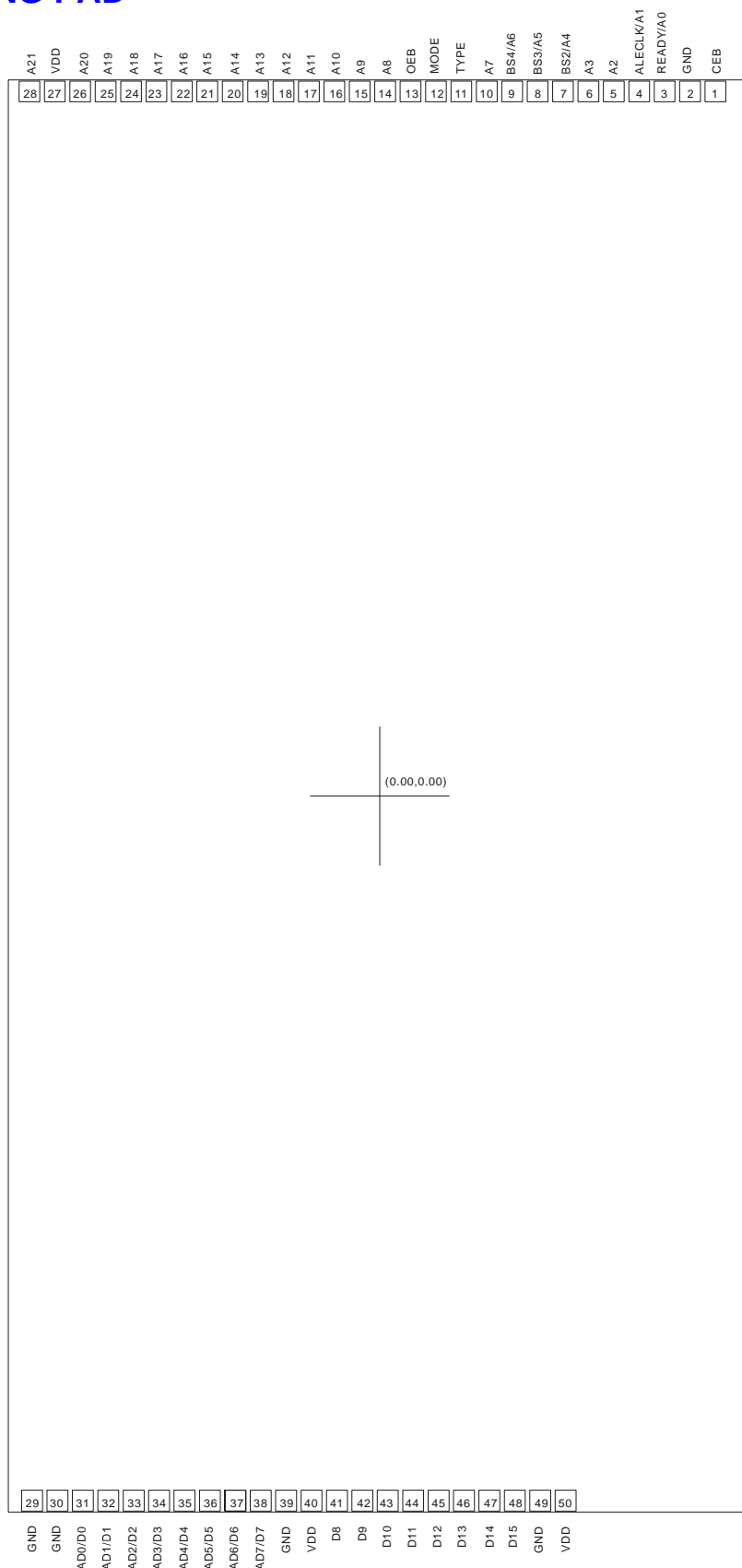
SNR032 32M-bit Mask ROM

Device No.	Start address	End Address	Memory Size
1 st external device(CS0)	0x0200000	0x03FFFFFF	2M words
2 nd external device(CS1)	0x0400000	0x07FFFFFF	4M words
3 rd external device(CS2)	0x0800000	0x0BFFFFFF	4M words
4 th external device(CS3)	0x0C00000	0x0FFFFFFF	4M words





8. BONDING PAD



Note: The substrate *MUST* be connected to Vss in PCB layout.



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