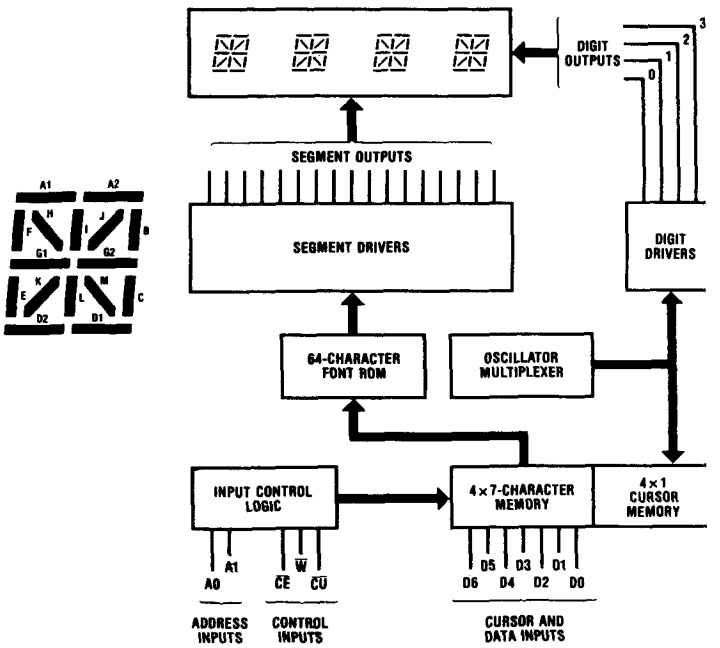
Application Notes

Using the NSM-1416 Intellisplay™

The NSM-1416 is designed for ease of application both from hardware and software points of view. Its asynchronous input architecture using only 7 data input, 2 digit selects, and 3 timing/select/enable inputs produces a device which is as simple to use as a directly addressable memory or I/O peripheral device. In brief terms the device is selected, data is presented, latched in, and then ignored by the system until the data displayed needs to be changed. This minimizes system overhead time required to display data freeing the processor for other uses. In most applications no other support chips are needed.

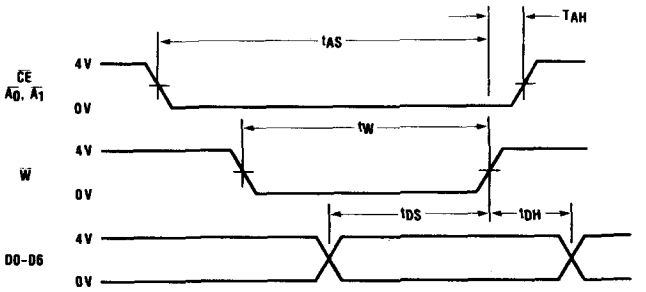
Block Diagram



Inputs

Symbol	Name	Function
D0-D6	Data Lines	Seven input lines—input for ASCII coded characters
A_0-A_1	Digit Select	Binary coded selection of digit 1 through 4 within a device
$\overline{CE}$	Chip Enable	Active Low-Signal selects device for accepting input. High signal disables all input lines
$\overline{CU}$	Cursor	Active Low-Signal enable writing/erasing of cursor in any digit position selected by D0-D3 lines
$\overline{W}$	Write	Active Low-Signal times latching of data from D0-D6 into the digit memory location selected by A_0-A_1
V+ (V_{CC})	Positive Supply	+5V ± .5V TTL/CMOS compatible
V−	Negative Supply	Ground

Timing Diagram



USING THE NSM-1416 INTELLISPLAY™ (cont)

oading Data

ata entry is asynchronous and random. $\overline{CE}$ must e held low and $\overline{CU}$ must be held high to enable ata entry. The data code (D0-D6), which selects ne of the 64 character set, and digit address A_0, A_1), are held stable while $\overline{W}$ is held low. nis stores the appropriate character from the naracter set into the digit specified by A_0 and $_1$. This data is maintained for that digit until ew data is entered.

oading Cursor

or loading of the cursor (all 16 segments on), E and $\overline{CU}$ must be held low. DO, D1, D2, and 3 are used to specify which of the digits are to ceive cursor loading. A cursor will appear for gits 0, 1, 2, or 3 corresponding to a high state r D0, D1, D2, or D3, respectively, occurring with low state for $\overline{W}$. Simultaneously loading D0-D3 gh achieves the display test function. The cursor ill remain loaded until cleared. The cursor is eared with the same procedure except that a low ate is used for D0, D1, D2, or D3.

legal Code

an illegal ASCII code is entered as the data ode (i.e., D6 = D5) the display will automatically e blanked for the corresponding digit.

itializing

o initialize the device after power-up, enter a gal data code set (D6≠D5), and then clear ursors for each digit.

igit Selection

sing positive logic, digit selection is from right left. Using either hardware or software inversion logical complementing of A_0-A_1 signals the der is reversed to left to right.

ystem Interface

ne NSM-1416 can be directly interfaced to many icroprocessors using the parallel I/O parts for ata and digit selects and flags for enable.select/ rite functions. Attention must be given to the ning relationships between the microprocessor nd the NSM-1416.

Loading Data

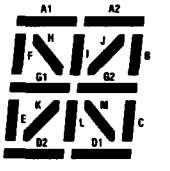
$\overline{CE}$	$\overline{CU}$	$\overline{W}$	Address A_1	Address A_0	D6	D5	D4	D3	D2	D1	D0	Digit 3	Digit 2	Digit 1	Digit 0
H	X	X	X	X	X	X	X	X	X	X	X	No Change	No Change	No Change	No Change
L	H	L	L	L	H	L	L	L	L	L	H	No Change	No Change	No Change	A
L	H	L	L	H	H	L	L	L	L	H	L	No Change	No Change	B	A
L	H	L	H	L	H	L	L	L	L	H	H	No Change	C	B	A
L	H	L	H	H	H	L	L	L	H	L	L	D	C	B	A
L	H	L	L	L	H	L	L	L	H	L	H	D	C	B	E
L	H	L	H	L	H	L	L	H	L	H	H	D	K	B	E
L	H	L	—	—	—	—	—	—	—	—	—	See character set			

X = Don't care

Loading Cursor

$\overline{CE}$	$\overline{CU}$	$\overline{W}$	Address A_1	Address A_0	D6	D5	D4	D3	D2	D1	D0	Digit 3	Digit 2	Digit 1	Digit 0
H	X	X	X	X	X	X	X	X	X	X	X	D	K	B	E
L	L	L	X	X	X	X	X	L	L	L	H	D	K	B	⁘
L	L	L	X	X	X	X	X	L	L	L	L	D	K	B	E
L	L	L	X	X	X	X	X	L	L	H	L	D	K	⁘	E
L	L	L	X	X	X	X	X	L	H	L	L	D	⁘	B	E
L	L	L	X	X	X	X	X	H	L	L	L	⁘	K	B	E
L	L	L	X	X	X	X	X	H	H	H	H	⁘	⁘	⁘	⁘
L	L	L	X	X	X	X	X	L	L	L	L	D	K	B	E

X = Don't care



CHARACTER SET

D6	D5	D4	D3	D0 L	D0 H	D1 L	D1 L	D1 H	D1 H	D2 L	D2 L	D2 L	D2 L	D2 H	D2 H	D2 H	D2 H
L	H	L	L														
L	H	L	H														
L	H	H	L														
L	H	H	H														
H	L	L	L														
H	L	L	H														
H	L	H	L														
H	L	H	H														

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