Micro Circuit Engineering

MT32018
MT32028

ENCODER/DECODER

MIL-STD-1553B
THE INTERNATIONAL STANDARD

ACTUAL SIZE

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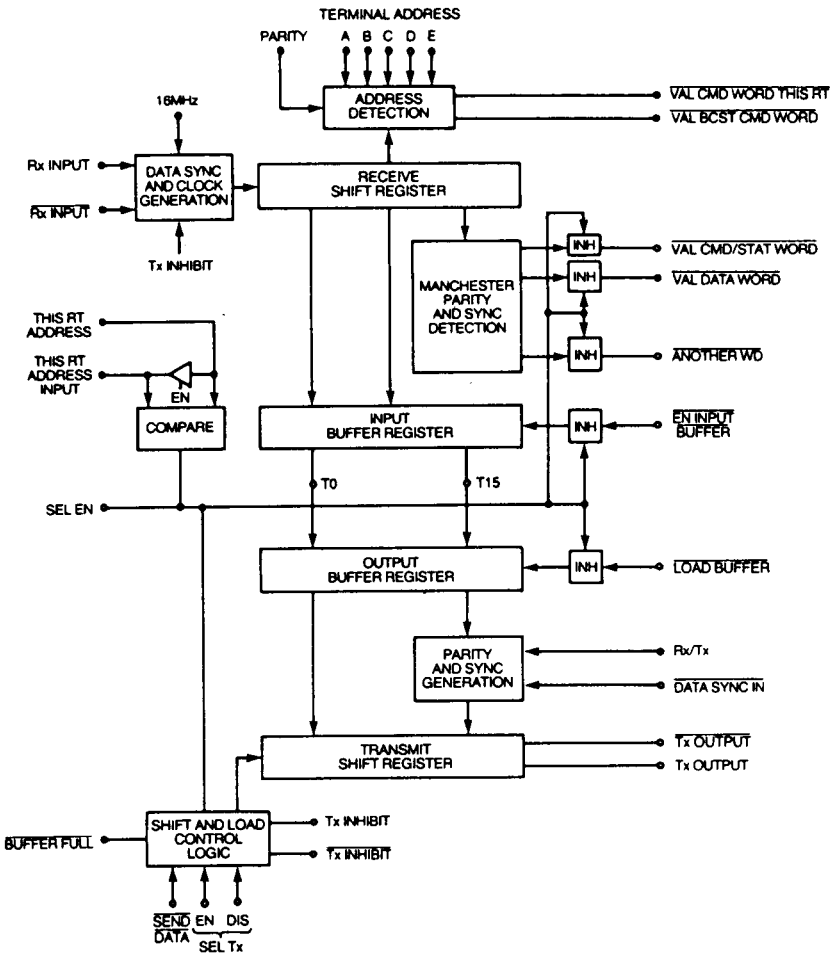
FEATURES

- COMPLIANT TO 1553
- COMPLETE WORD VALIDATION
- OPTIONAL WATCHDOG TIMER
- PARALLEL DATA INTERFACE
- LOW POWER CMOS TECHNOLOGY

SIMPLIFIED BLOCK SCHEMATIC



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GENERAL

The decoder half of this single monolithic device handles all the word validation required by 1553. It receives serial data via a transceiver, checks for valid Manchester bi-phase, parity, sync field and terminal address and provides a 16 bit parallel data output.

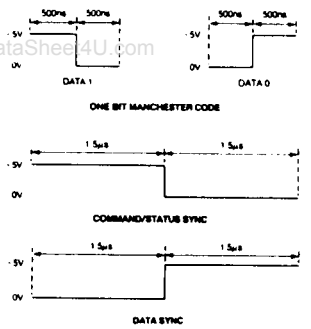
The encoder takes a 16 bit parallel input, converts it to Manchester bi-phase, adds sync and parity and transmits via a transceiver.

The MT32018 inhibits the receiver during transmission.

The MT32028 can receive its own transmissions provided the receive half of the transceiver is not inhibited.

RECEIVE MODE

The device requires an active low signal of 250ns minimum applied to $\overline{\text{RESET}}$ with POWER ON. Command/status words or data words consisting of 20 bits (Manchester code) are serially received at the RXIN and $\overline{\text{RXIN}}$ inputs ($\overline{\text{RXIN}}$ is the inverse of RXIN) via transceiver at a bit rate of 1MHz. The data is synchronised with a 16MHz free-running clock and shifted into a 40 bit shift register (2 bits of shift register for 1 Manchester code bit). The first 3 bits to be received contain either the command/status sync or data sync which are invalid Manchester code.



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The first 6 bits of the shift register (3 data bits) are being continually monitored detecting either a command/status sync or data sync. When a command/status sync or data sync is detected, the data in the shift register is checked for correct Manchester coding and odd parity. If there are no errors (i.e. valid word) the 16 data bits in the shift register (bits 4-19) are transferred to the input buffer register.

When a command word is received the most significant 5 bits of the command are compared with the hard-wired terminal address (ADDR E being the most significant bit). The 5 bit hard-wired terminal address pins and address parity pin are checked for odd parity. If the parity is correct and the address compares then a "valid RT address" has been detected.

If the most significant 5 bits of the command are all at a '1' then a "valid broadcast address" has been detected.

Output signal $\overline{\text{VAL CMD WORD THIS RT}}$ becomes valid for 500ns if a command sync has been detected along with valid word and valid RT address. If valid broadcast address was detected instead of valid RT address then the signal $\overline{\text{VALID BCST CMD WORD}}$ becomes valid for 500ns.

When $\overline{\text{VALID CMD WORD THIS RT}}$ or $\overline{\text{VALID BCST CMD WORD}}$ becomes valid the hard-wired bus address (THIS RT ADDR) is enabled to the I/O pin THIS RT ADDR IP for the same period of 500ns.

The I/O pin (THIS RT ADDR IP) is being continuously compared with the hard-wired bus address (THIS RT ADDR). If equal then SEL EN becomes valid.

To select which bus is to be used for transmitting and receiving, the input (THIS RT ADDR IP) must be set to the same logical state as the hard-wired bus address (THIS RT ADDR).

Output signal $\overline{\text{VAL CMD/STAT WORD}}$ becomes valid for 500ns if a command/status sync has been detected along with valid word, provided SEL EN is valid. If a data sync was detected instead of a command/status sync then the signal $\overline{\text{VALID DATA WORD}}$ becomes valid for 500ns.

The last 12 bits of the shift register are being continuously monitored to give early warning of a new word being received, i.e. a command/status/data sync plus 3 bits of correct Manchester coding. If this has been detected the output $\overline{\text{ANOTHER WORD}}$ becomes valid for 500ns providing SEL EN is valid.

With SEL EN valid the contents of the input buffer register can be enabled onto the 16 bit I/O highway T0-T15 (T15 being the most significant) via signal $\overline{\text{EN INPUT BUFFER}}$ being active low.

Also with SEL EN valid the transmit circuitry is enabled.

TRANSMIT MODE

To transmit data from the device the signal SEL EN must be valid. Data present on the 16 bit I/O highway to be transmitted is loaded into the output buffer register with input signal $\overline{\text{LOAD BUFFER}}$.

The command/status sync or data sync is internally generated and is also loaded into the register to be the first 3 bits of transmission. The status sync waveform is the same as the command sync waveform. From this register a parity bit is generated.

The only exception to the automatic sync generation is for a Bus Controller to issue an RT to RT transfer command (i.e. two consecutive command words). This is achieved by setting RX/TX to a zero and the type of sync is determined by the signal $\overline{\text{DATA SYNC IN}}$ ('1' = CMD SYNC, '0' = DATA SYNC) during $\overline{\text{LOAD BUFFER}}$.

To initialise transmission an active low signal on $\overline{\text{SEND DATA}}$ is required. Data will be transferred from the output buffer register, converted to Manchester code, and loaded into the 40 bit shift register and shifted out via TXOUT and $\overline{\text{TXOUT}}$ ($\overline{\text{TXOUT}}$ is the inverse of TXOUT during transmission, and both are high with no transmission) to the transceiver. If $\overline{\text{LOAD BUFFER}}$ is applied before the end of transmission, then the transmit sequence will be repeated when the full 20 bit word has been transmitted with no inter-word gap.

When transmission is taking place and there is another word waiting in the output buffer for transmission, the output signal $\overline{\text{BUFFER FULL}}$ becomes valid. If $\overline{\text{LOAD BUFFER}}$ becomes valid the contents of the buffer are overwritten.

In an RT the first word for transmission will always be the status word and the top 5 bits of status are the remote terminal address. There are two methods of loading this address along with status into the buffer register.

(a) The terminal address may be applied to the highway (T11-T15, T15 being MSB terminal address E) along with the rest of the status word and loaded into the buffer with $\overline{\text{LOAD BUFFER}}$. To initiate transmission, $\overline{\text{SEND DATA}}$ is applied along with $\overline{\text{LOAD BUFFER}}$ or any time after $\overline{\text{LOAD BUFFER}}$. (The terminal address being the same address as the transmitting device).

(b) If bits T11-T15 are left high impedance with the status enabled onto T0-T10 then the hard-wired terminal address will be internally enabled onto T11-T15 with signal $\overline{\text{SEND DATA}}$. Therefore $\overline{\text{LOAD BUFFER}}$ must be applied during $\overline{\text{SEND DATA}}$

There are 2 other inputs to the device, SEL TX EN and SEL TX DIS. When SEL EN is valid, a pulse on SEL TX DIS disables transmission and a pulse on SEL TX EN enables transmission. (Min pulse width 250ns).

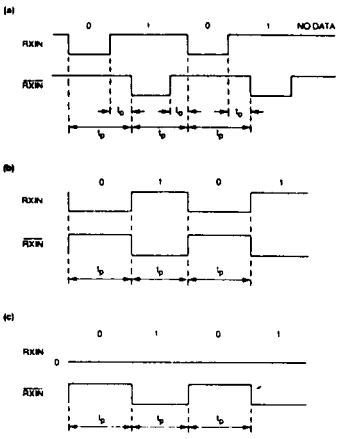
An active low signal on $\overline{\text{RESET}}$ will set the transmitter in the enable mode.

During a message transmission the output TX INHIBIT becomes not valid. Output $\overline{\text{TX INHIBIT}}$ is also available to connect an external Watchdog Timer. If the Timer is not required this pin may be left open circuit.

DETAILED TIMING

Receive Mode

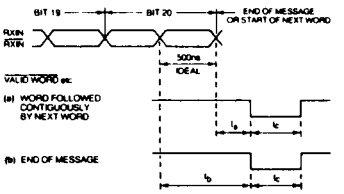
RXIN Waveform Requirements There are three variations of waveform requirements required at the RXIN and $\overline{\text{RXIN}}$ inputs.



Waveform (a) is the ideal. With waveform (b) applied, the device is less immune to noise on these inputs than waveform (a). With waveform (c) applied, the device is less immune to noise on these inputs than waveform (b).

The device will accept waveforms with tp varying from the ideal (including rise and fall times) of ± 180ns (i.e. 2.0 ± 0.18µs, 1.5 ± 0.18µs, 1.0 ± 0.18µs, 0.5 ± 0.18µs).
(The tolerance required by the 1553B standard is ±0.15µs.)
Overlap period (to) 10ns minimum 400ns maximum.

Propagation Delays Propagation delays over free air temperature range V_{DD} = 5 Volts. Propagation delays do not include rise and fall time of outputs.
Propagation delay time RXIN or $\overline{\text{RXIN}}$ to $\overline{\text{VALID DATA WORD}}$, $\overline{\text{VALID CMD WD THIS RT}}$, $\overline{\text{VALID BCST CMD WORD}}$, $\overline{\text{VALID CMD/STATUS WORD}}$

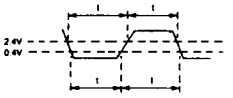


ta 300ns minimum 480ns maximum.
tb 800ns minimum 980ns maximum.
tc 460ns minimum 540ns maximum: for ideal RXIN

Propagation delay time:

	MIN	MAX
$\overline{\text{EN IP BUFFER}}$ to T0 – T15	20ns	75ns
$\overline{\text{VAL WORD}}$ to T0 – T15	15ns	50ns
$\overline{\text{VALID CMD WD THIS RT/BCST}}$ to THIS RT ADDR IP (remains enabled for half bit period, 500ns ideal)	25ns	150ns
THIS RT ADDR IP to SEL EN	65ns	200ns

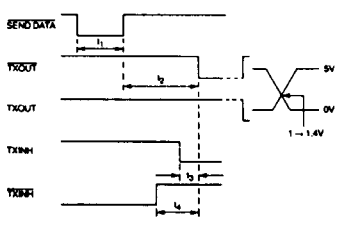
16 MHz Clock Requirement



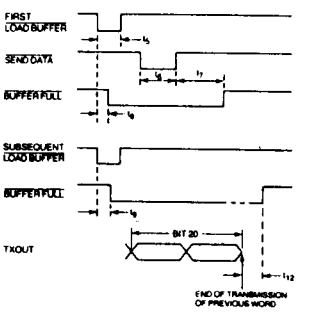
	MIN	MAX
t	40%	60% of cycle

Frequency 16MHz ± 0.01%

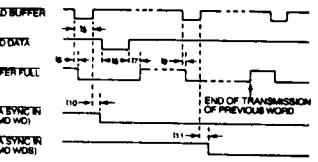
Transmit Mode
Propagation delay time $\overline{\text{SEND DATA}}$ to TXOUT, TX INH.

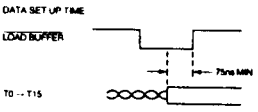


Propagation delay time $\overline{\text{LOAD BUFFER}}$ to $\overline{\text{BUFFER FULL}}$.



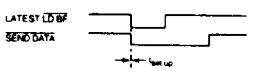
Propagation delay times for $\overline{\text{LOAD BUFFER}}$ operations (external sync generation).





	MIN	MAX
t_1	250ns	
t_2	320ns	600ns
t_3	30ns	110ns
t_4	40ns	150ns
t_5	125ns	
t_6	250ns	
t_7	280ns	500ns
t_8	30ns	100ns
t_9	30ns	100ns
t_{10}	75ns	
t_{11}	75ns	
t_{12}	230ns	370ns

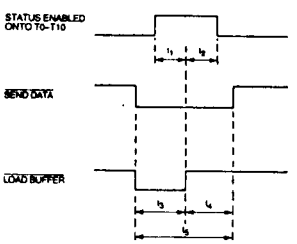
The first load buffer may occur any time before $\overline{\text{SEND DATA}}$ but no later than $\overline{\text{SEND DATA}}$ i.e.



$t_{set\ up}$ MIN = 0ns

In a BC if RXTX is high (internal sync generation) then $\overline{\text{LDBF}}$ must occur before $\overline{\text{SEND DATA}}$ and $t_{set\ up}$ will apply to rising edge of $\overline{\text{LD BF}}$.

If the device is required to internally load its own RT address to be transmitted with status, then the send data and load buffer signals must be as shown.



	MIN
t_1	75ns
t_2	75ns
t_3	125ns
t_4	125ns
t_5	250ns

OPERATING CONDITIONS

Absolute Maximum Ratings

Supply voltage V_{DD}	+ 7 Volts
Supply voltage V_{SS}	0 Volts
Low level input voltage	V_{SS} −0.5 Volts
High level input voltage	V_{DD} +0.5 Volts
Operating free air temperature range	−55°C to +125°C
Storage temperature range	−65°C to +150°C

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{DD}	4.5	5	5.5	Volts
Operating free air temperature	−55		+125	°C

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DYNAMIC ELECTRICAL CHARACTERISTICS

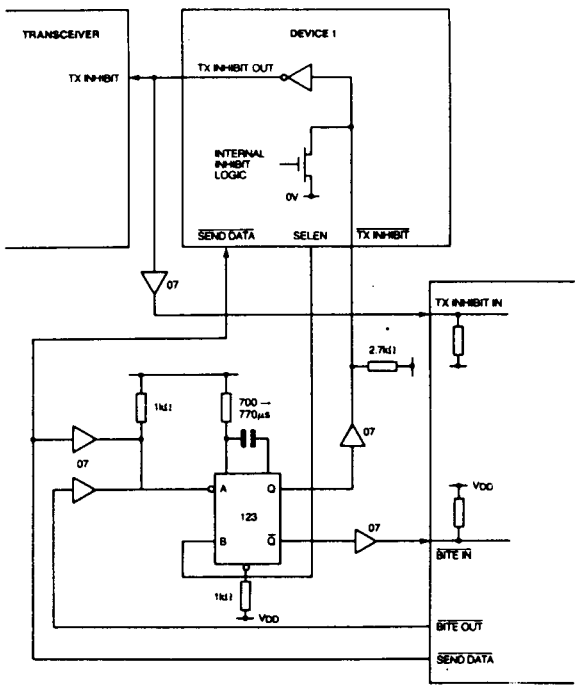
Over free air temperature range V_{DD} = 5 Volts
Rise time of output V_{SS} to 3 Volts into 20pF load = 50ns maximum.
Fall time of output V_{DD} to 0.4 Volts into 20pF load = 50ns maximum.

STATIC ELECTRICAL CHARACTERISTICS

Over recommended free air temperature range V_{DD} = 5 volts

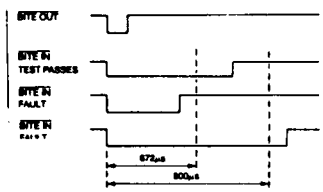
	MIN	NOM	MAX	UNIT
Input Type 'A'				
V_{IH} High level input voltage	2.4		V_{DD}	Volts
V_{IL} Low level input voltage	V_{SS}		0.8	Volts
C_{IN} Input capacitance			10	pf
Input Type 'B'				
V_{IH} High level input voltage	2.4 or OC if unused		V_{DD} or OC if unused	Volts
V_{IL} Low level input voltage	V_{SS}		0.8	Volts
I_{IL} Low level input current			0.8	mA
C_{IN} Input capacitance			10	pf
Input Type 'C'				
V_{IH} High level input voltage	2.4 or OC if unused		V_{DD} or OC if unused	Volts
V_{IL} Low level input voltage	V_{SS}		0.8	Volts
I_{IL} Low level input current			0.4	mA
C_{IN} Input capacitance			10	pf
Input Type 'D'				
V_{IH} High level input voltage	2.4		V_{DD}	Volts
V_{IL} Low level input voltage	V_{SS} or OC if unused		0.8 or OC if unused	Volts
I_{IH} High level input current			0.4	mA
C_{IN} Input capacitance			10	pf
Output Type 'E'				
V_{OH} High level output voltage	4.5		V_{DD}	Volts
V_{OL} Low level output voltage			0.4	Volts
I_{OH} High level output current	1.0			mA
I_{OL} Low level output current	−3.2			mA
Output Type 'F' (open drain)				
V_{OH} High level output voltage	OC		OC	
V_{OL} Low level output voltage			0.4	Volts
I_{OL} Low level output current	−3.2			mA
Input/Output Type 'G'				
V_{IH} High level input voltage	2.4		V_{DD}	Volts
V_{IL} Low level input voltage	V_{SS}		0.8	Volts
V_{OH} High level output voltage	4.5		V_{DD}	Volts
V_{OL} Low level output voltage			0.4	Volts
I_{OH} High level output current	1.0			mA
I_{OL} Low level output current	−3.2			mA
C_{IO} I/O Capacitance			10	pf
Supply current		2.5	5.0	mA

WATCHDOG TIMER



If a device fails in such a way as to continuously transmit, the Watchdog Timer will inhibit the transceiver from transmitting the data onto the bus.

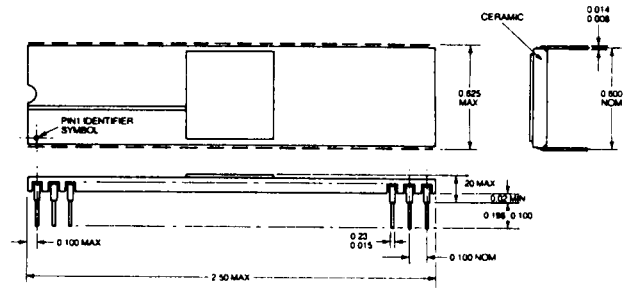
The function of the Watchdog Timer may be tested by the use of the $\overline{\text{BITEOUT}}$ and $\overline{\text{BITEIN}}$ signals.

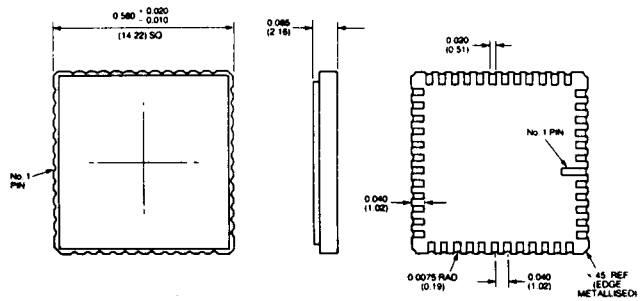


MNEMONICS

T0 → T15	16 bit bi-directional highway
ADDR A → E	Hard wired RT address (ADDR E is MSB)
ADDR PARITY	Hard wired address parity (odd)
RXIN / $\overline{\text{RXIN}}$	Manchester bi-phase input from transceiver
SEL EN	Watchdog Timer control
$\overline{\text{RESET}}$	General reset
TXOUT / $\overline{\text{TXOUT}}$	Manchester bi-phase output to transceiver
TX INHIBIT	Transmit inhibit to transceiver
$\overline{\text{TX INHIBIT}}$	Watchdog Timer input
SEL TX DIS	Disable transmitter
SEL TX EN	Enable transmitter
16MHz	16MHz Crystal Oscillator
THIS RT ADDR	Hard-wired bus address
RT/$\overline{\text{TX}}$ / $\overline{\text{DATA SYNC IN}}$	External control of sync generation
$\overline{\text{VAL CMD WORD THIS RT}}$	Signal from Encoder/Decoder – received valid command word with terminal's address.
$\overline{\text{VAL BCST CMD WORD}}$	Signal from Encoder/Decoder – received valid command word with broadcast address.
$\overline{\text{VAL CMD/STAT WORD}}$	Signal from Encoder/Decoder – received valid command/status word on selected bus.
$\overline{\text{VAL DATA WORD}}$	Signal from Encoder/Decoder – received valid data word on selected bus.
$\overline{\text{ANOTHER WORD}}$	Signal from Encoder/Decoder – received early warning of another word on selected bus.
THIS RT ADDR IP	Bi-directional signal to/from encoder/decoder – sets up bus selection.
$\overline{\text{EN IP BUFFER}}$	Control signal to encoder/decoder to enable received data onto highway.
$\overline{\text{SEND DATA}}$	Control signal to encoder/decoder to initiate transmission.
$\overline{\text{LOAD BUFFER}}$	Control signal to encoder/decoder to load data ready for transmission.
$\overline{\text{BUFFER FULL}}$	Control signal from encoder/decoder indicating that the transmit buffer register is full.

MECHANICAL CHARACTERISTICS





PIN ASSIGNMENTS

PIN NO.	SIGNAL	IO TYPE	PIN NO.	SIGNAL	IO TYPE
1	T1	G	25	T10	G
2	T2	G	26	T11	G
3	T3	G	27	T12	G
4	T4	G	28	T13	G
5	T5	G	29	T14	G
6	T6	G	30	T15	G
7	T7	G	31	TERM ADDR E	C
8	$\overline{\text{RESET}}$	A	32	TERM ADDR D	C
9	$\overline{\text{LOAD BUFFER}}$	A	33	TERM ADDR C	C
10	$\overline{\text{BUFFER FULL}}$	F	34	TERM ADDR B	C
11	SEL EN	E	35	TERM ADDR A	C
12	$\overline{\text{SEND DATA}}$	A	36	$\overline{\text{VAL CMD/STAT WORD}}$	F
13	$\overline{\text{TX OUT}}$	E	37	$\overline{\text{ANOTHER WORD}}$	F
14	TX OUT	E	38	$\overline{\text{VAL BCST CMD WORD}}$	F
15	$\overline{\text{TX INHIBIT}}$	B	39	$\overline{\text{VAL CMD WORD THIS RT}}$	F
16	TX INHIBIT	E	40	ADDR PARITY	C
17	THIS RT ADDR	A	41	$\overline{\text{RXIN}}$	A
18	RX/$\overline{\text{TX}}$	C	42	RXIN	A
19	$\overline{\text{DATA SYNC IN}}$	C	43	16MHz	A
20	THIS RT ADDR IP	G	44	$\overline{\text{VALID DATA WORD}}$	F
21	$\overline{\text{EN IP BUFFER}}$	A	45	SEL TX EN	A
22	V_{SS}		46	SEL TX DIS	A
23	T8	G	47	V_{DD}	
24	T9	G	48	T0	G

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BSI Approval No. 1267/M

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