

HAT2279H

Silicon N Channel Power MOS FET Power Switching

REJ03G1464-0200

Rev.2.00

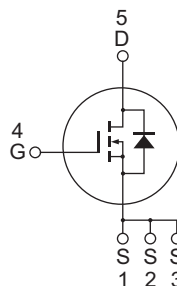
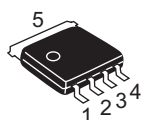
Jul 05, 2006

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 9.5 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Lead Free

Outline

RENESAS Package code: PTZZ0005DA-A)
(Package name: LFAK)



1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

| Item | Symbol | Ratings | Unit |
|----------------------------------------|----------------------------------|-------------|--------------------|
| Drain to source voltage | V_{DSS} | 80 | V |
| Gate to source voltage | V_{GSS} | ± 20 | V |
| Drain current | I_D | 30 | A |
| Drain peak current | $I_{D(pulse)}$ ^{Note 1} | 120 | A |
| Body-drain diode reverse drain current | I_{DR} | 30 | A |
| Avalanche current | I_{AP} ^{Note 2} | 25 | A |
| Avalanche energy | E_{AR} ^{Note 2} | 83 | mJ |
| Channel dissipation | P_{ch} ^{Note 3} | 25 | W |
| Channel to Case Thermal Resistance | θ_{ch-C} | 5 | $^\circ\text{C/W}$ |
| Channel temperature | T_{ch} | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
3. $T_c = 25^\circ\text{C}$

Electrical Characteristics

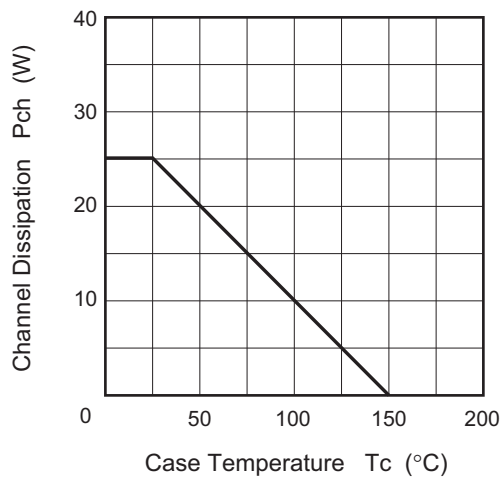
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--------------------------------------------|---------------|-----|------|-----------|------------------|----------------------------------------------------------------------------------------------------------------------------|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 80 | — | — | V | $I_D = 10 \text{ mA}$, $V_{GS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ± 0.5 | μA | $V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | 1 | μA | $V_{DS} = 80 \text{ V}$, $V_{GS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 0.8 | — | 2.3 | V | $V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 9.5 | 12 | $\text{m}\Omega$ | $I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4} |
| | $R_{DS(on)}$ | — | 11 | 15 | $\text{m}\Omega$ | $I_D = 15 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4} |
| Forward transfer admittance | $ y_{fs} $ | 42 | 70 | — | S | $I_D = 15 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4} |
| Input capacitance | C_{iss} | — | 3520 | — | pF | $V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$ |
| Output capacitance | C_{oss} | — | 410 | — | pF | |
| Reverse transfer capacitance | C_{rss} | — | 160 | — | pF | |
| Gate Resistance | R_g | — | 0.5 | — | Ω | |
| Total gate charge | Q_g | — | 60 | — | nC | $V_{DD} = 25 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 30 \text{ A}$ |
| Gate to source charge | Q_{gs} | — | 9.5 | — | nC | |
| Gate to drain charge | Q_{gd} | — | 9.0 | — | nC | |
| Turn-on delay time | $t_{d(on)}$ | — | 9.5 | — | ns | $V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$, $V_{DD} \cong 30 \text{ V}$, $R_L = 2 \Omega$, $R_g = 4.7 \Omega$ |
| Rise time | t_r | — | 14.5 | — | ns | |
| Turn-off delay time | $t_{d(off)}$ | — | 56 | — | ns | |
| Fall time | t_f | — | 9.5 | — | ns | |
| Body-drain diode forward voltage | V_{DF} | — | 0.83 | 1.08 | V | $I_F = 30 \text{ A}$, $V_{GS} = 0$ ^{Note4} |
| Body-drain diode reverse recovery time | t_{rr} | — | 50 | — | ns | $I_F = 30 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$ |

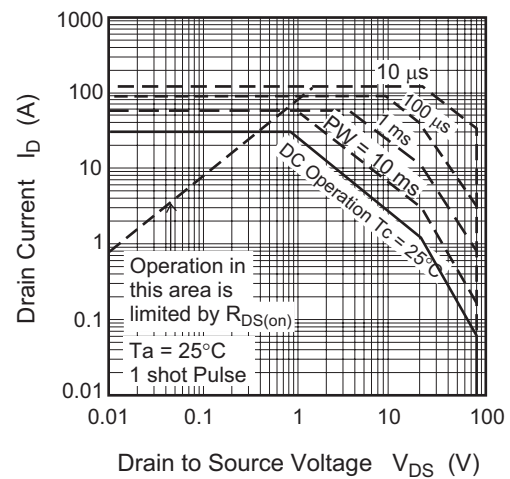
Notes: 4. Pulse test

Main Characteristics

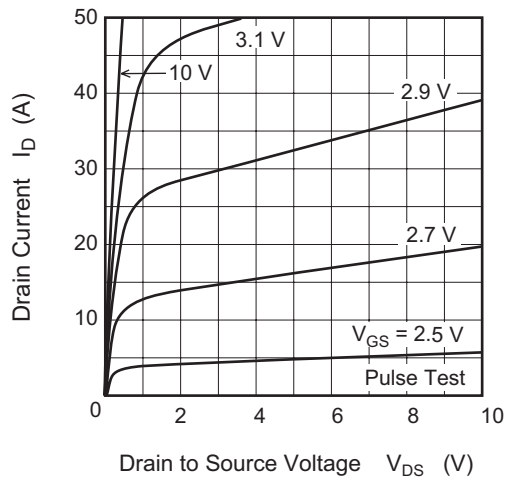
Power vs. Temperature Derating



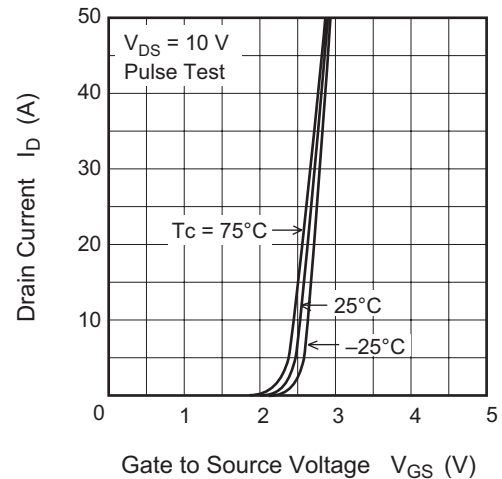
Maximum Safe Operation Area



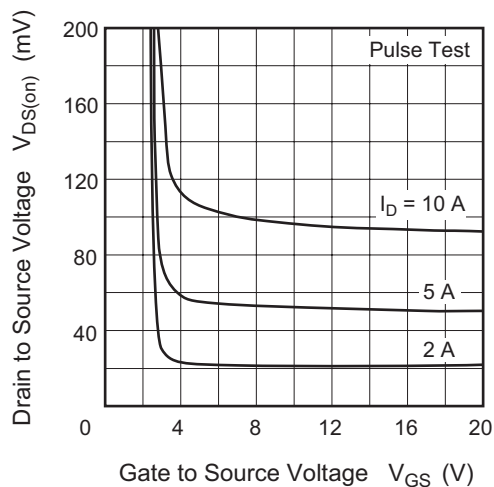
Typical Output Characteristics



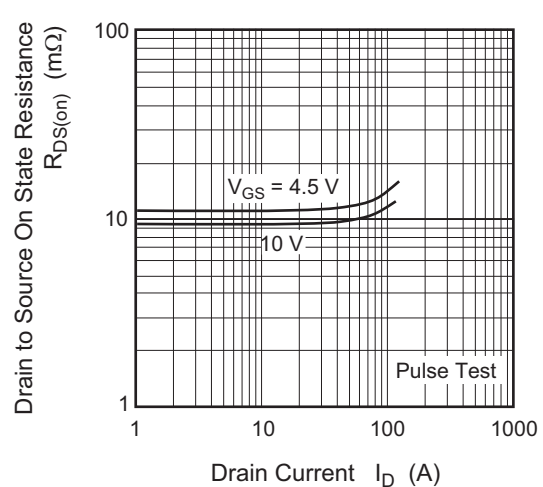
Typical Transfer Characteristics

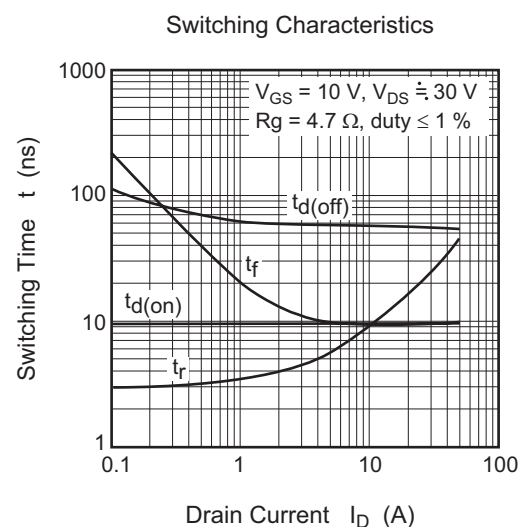
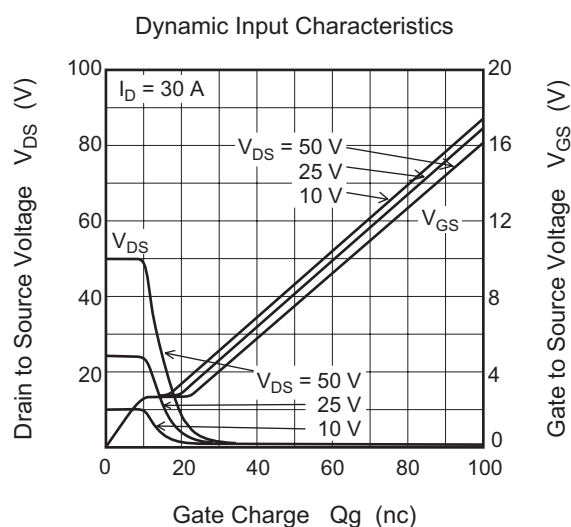
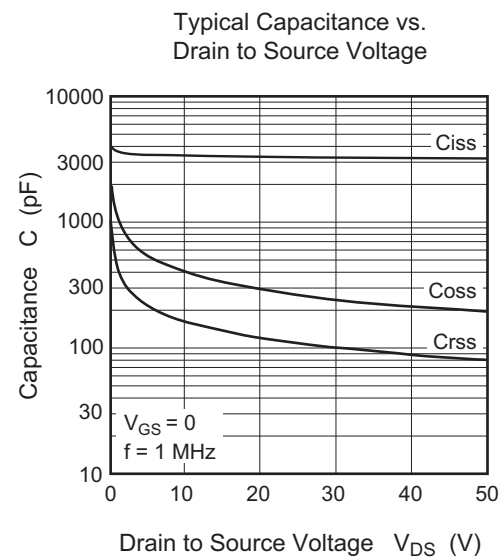
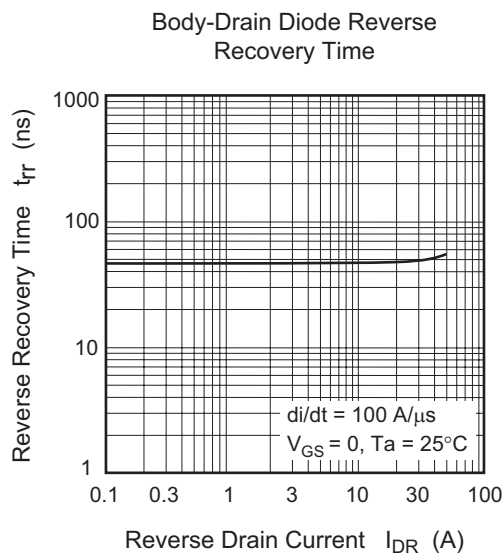
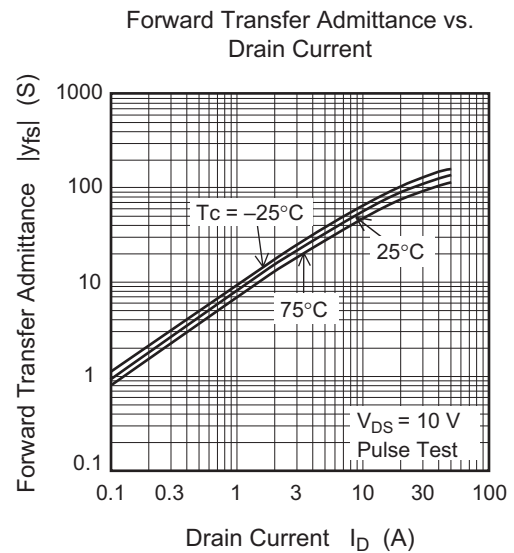
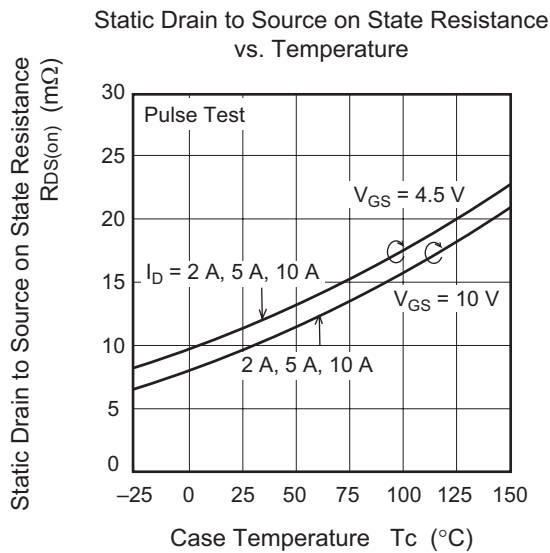


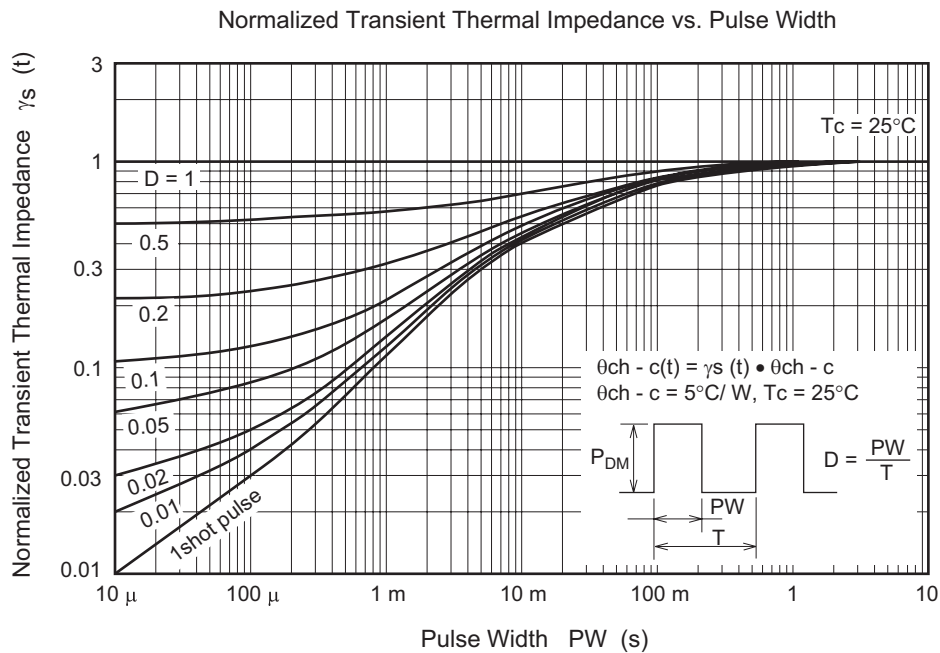
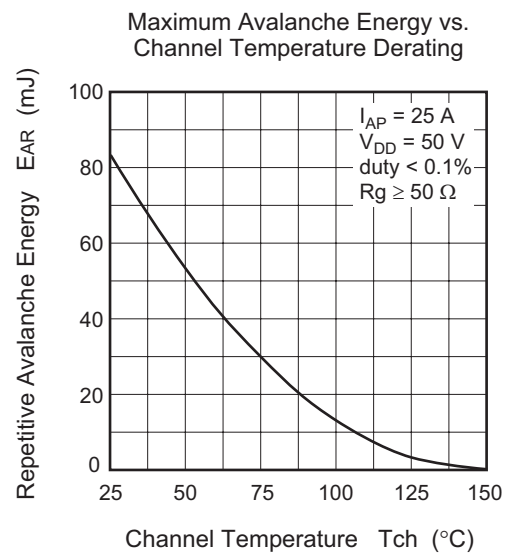
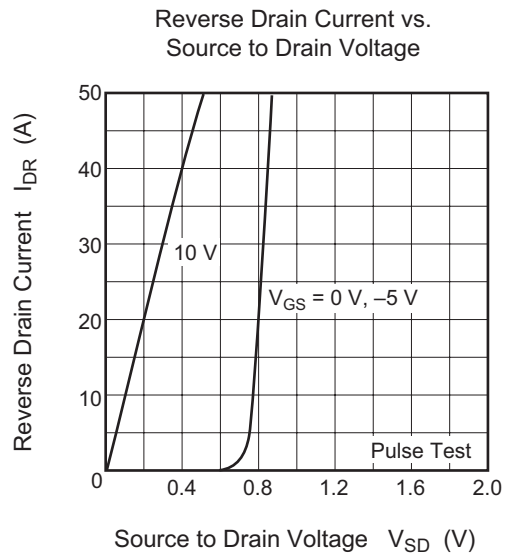
Drain to Source Saturation Voltage vs. Gate to Source Voltage



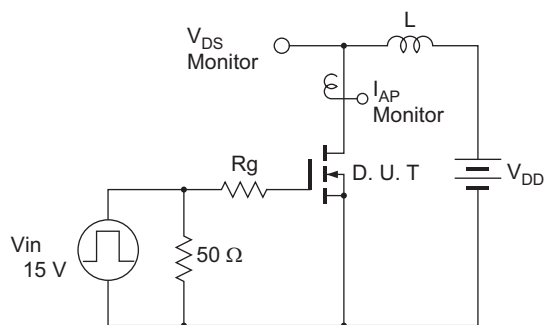
Static Drain to Source on State Resistance vs. Drain Current





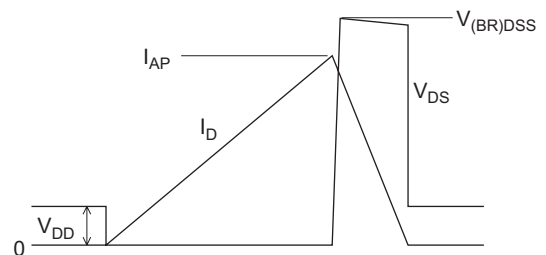


Avalanche Test Circuit

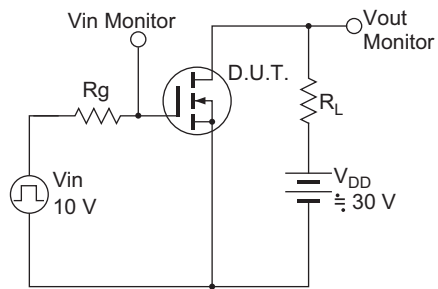


Avalanche Waveform

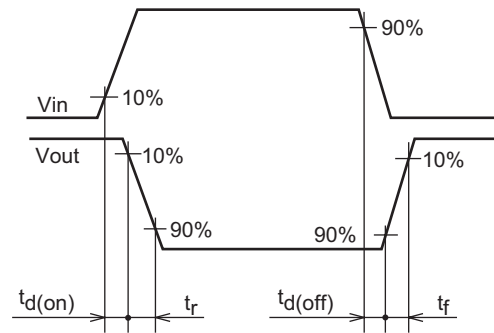
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



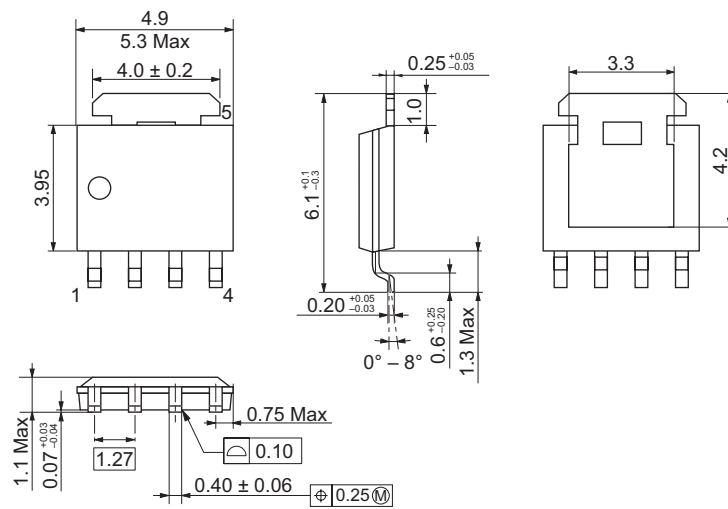
Waveform



Package Dimensions

| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|--------------|--------------------|--------------|---------------|------------|
| LPAK | SC-100 | PTZZ0005DA-A | LPAKV | 0.080g |

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

| Part Name | Quantity | Shipping Container |
|---------------|----------|--------------------|
| HAT2279H-EL-E | 2500 pcs | Taping |

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