



A027DN03 V3 Product Spec	Version	0.3
	Page	1/63

## CUSTOMER APPROVAL SHEET

<b>Company Name</b>	
<b>MODEL</b>	A027DN03 V3
<b>CUSTOMER APPROVED</b>	Title :  Name :

- ☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.3)
- ☐ APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.3)
- ☐ APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.3)
- ☐ CUSTOMER REMARK : \_\_\_\_\_

AUO PM :

P/N : 97.02A41.300

Comment :



A027DN03 V3 Product Spec	Version	0.3
	Page	2/63

Doc. version:	0.3
Total pages:	63
Date:	2009/12/22

## Product Specification

### 2.7" COLOR TFT-LCD MODULE

**Model Name : A027DN03 V3**

<b>Planned Lifetime:</b>	From 2009/Jun To 2010/Dec
<b>Phase-out Control:</b>	From 2010/Oct To 2010/Dec
<b>EOL Schedule:</b>	2010/Dec

< > Preliminary Specification

< ◆ > Final Specification

Note: The content of this specification is subject to change.

© 2010 AU Optronics  
All Rights Reserved,  
Do Not Copy.



A027DN03 V3 Product Spec	Version	0.3
	Page	3/63

## Record of Revision

Version	Revise Date	Page	Content
0.0	2009/06/03		First draft
		30~31 43~44	Update gamma table
		11	Add power consumption spec
		31 ~ 45	Delete R94 function and update R97 default value
		51	Add packing form
		52	Add outline dimension
0.1	2009/08/28	11	Add I <sub>DD(STANDBY)</sub> and VCDC spec
		30~31 43~44	Update R48~R79 define
		57~62	Update R1 register setting
0.2	2009/10/20	57~62	Add R5 global reset initial setting before global reset
		46	Update chromaticity
0.3	2009/12/22	52	Change outline dimension (add white line)



A027DN03 V3 Product Spec	Version	0.3
	Page	4/63

## Contents

A. Physical specifications .....	6
B. Electrical specifications .....	7
1. Pin assignment .....	7
2. Absolute maximum ratings .....	10
3. Electrical characteristics .....	11
3.1 Recommended operating conditions (GND=AGND=0V) .....	11
3.2 Electrical characteristics (GND=AGND=0V) .....	11
3.3 Recommended Capacitance Values of External Capacitor .....	12
3.4 Backlight driving conditions .....	12
4. Input timing AC characteristic .....	13
5. Input timing format .....	14
5.1 UPS051 timing conditions (Refer to Fig.1 Fig.2 Fig.3) .....	14
5.2 UPS052 timing .....	17
5.2.1 UPS052 (320 mode/NTSC/24.535MHz) timing specifications. (refer to Fig.4 Fig.5) .....	17
5.2.2 UPS052 (320 mode/PAL/24.375MHz) timing specifications (refer to Fig.4 Fig.5) .....	17
5.2.3 UPS052 (360 mode/NTSC/27MHz) timing specifications (refer to Fig.4 Fig.5) .....	18
5.2.4 UPS052 (360 mode/PAL/27MHz) timing specifications (refer to Fig.4 Fig.5) .....	18
5.3 CCIR656 Timing .....	21
5.3.1 CCIR656 decoding .....	21
5.3.2 CCIR656 NTSC .....	22
5.3.3 CCIR656 PAL .....	22
5.4 YUV 720 and YUV 640 timing .....	23
5.4.1 YUV 720 mode/NTSC timing specifications (refer to Fig.7 Fig.9) .....	23
5.4.2 YUV 720 mode/PAL timing specifications (refer to Fig.7 Fig.9) .....	23
5.4.3 YUV 640 mode/NTSC timing specifications (refer to Fig.8 Fig.9) .....	24
5.4.4 YUV 640 mode/PAL timing specifications (refer to Fig.8 Fig.9) .....	24
5.5 CCIR656/YUV 720/YUV 640 to RGB conversion .....	27
6. Serial control interface AC characteristic .....	28
6.1 Timing chart .....	28
6.2 The configuration of serial data at SDA terminal is at below .....	29
6.3 Register table .....	30
6.4 Register description .....	32
C. Optical specification (Note 1, Note 2, Note 3 ) .....	46
D. Reliability test items .....	49
E. Packing form .....	51
F. Outline dimension .....	52



A027DN03 V3 Product Spec	Version	0.3
	Page	5/63

G. Application note ..... 53

1. Application circuit..... 53

1.1 Internal LED drive backlight..... 53

1.2 External LED drive backlight..... 54

2. Power on/off sequence..... 55

2.1 Power on (Standby Disabling)..... 55

2.2 Power off (Standby Enabling) ..... 56

3. Recommended power on/off serial command settings ..... 57

3.1 UPS051 ..... 57

3.2 UPS052 320 mode..... 58

3.3 UPS052 360 mode..... 59

3.4 CCIR656 ..... 60

3.5 YUV 720 ..... 61

3.6 YUV 640 ..... 62

4. Power generation circuit..... 63



A027DN03 V3 Product Spec	Version	0.3
	Page	6/63

## A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution ( dot )	960(W) x 240(H)	
2	Active area ( mm )	54 x 40.5	
3	Screen size ( inch )	2.658 (Diagonal)	
4	Dot pitch ( um )	56.25 x 168.75	
5	Color configuration	R, G, B delta	
6	Overall dimension ( mm )	63.5 x 46.6 x 2.6	Note 1
7	Weight ( g )	16.2	
8	Panel surface treatment	Glare type	

Note 1: Refer to F. Outline Dimension



A027DN03 V3 Product Spec	Version	0.3
	Page	7/63

## B. Electrical specifications

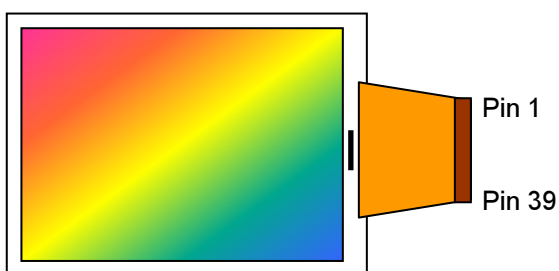
### 1. Pin assignment

Pin no	Symbol	I/O	I/O Structure	Description	Remark
1	VCOM	I	-	Panel common voltage	
2	CS	I	Type 3	Serial command enable	
3	SDA	I	Type 2	Serial command data input	
4	SCL	I	Type 1	Serial command clock input	
5	HSYNC	I	Type 1	Horizontal sync input	
6	VSYNC	I	Type 1	Vertical sync input	
7	DCLK	I	Type 1	Data clock input	
8	D7	I	Type 1	Data input; MSB	
9	D6	I	Type 1	Data input	
10	D5	I	Type 1	Data input	
11	D4	I	Type 1	Data input	
12	D3	I	Type 1	Data input	
13	D2	I	Type 1	Data input	
14	D1	I	Type 1	Data input	
15	D0	I	Type 1	Data input; LSB	
16	GND	P	-	Ground for digital circuit	
17	VDD	P	-	System power	3.0V~3.6V
18	DVDD	C	-	Power setting capacitor connect pin	
19	V1	C	-	Power setting capacitor connect pin	
20	V2	C	-	Power setting capacitor connect pin	
21	V3	C	-	Power setting capacitor connect pin	
22	V4	C	-	Power setting capacitor connect pin	
23	VDD2	C	-	Power setting capacitor connect pin	
24	V5	C	-	Power setting capacitor connect pin	
25	V6	C	-	Power setting capacitor connect pin	
26	VDD3	C	-	Power setting capacitor connect pin	
27	VDD5	C	-	Power setting capacitor connect pin	
28	V7	C	-	Power setting capacitor connect pin	
29	V8	C	-	Power setting capacitor connect pin	
30	VGH	C	-	Power setting capacitor connect pin	
31	VGL	C	-	Power setting capacitor connect pin	
32	AGND	P	-	Ground for analog circuit	

33	FRP	O	Type 4	Frame polarity output for VCOM	
34	COMDC	O	Type 5	VCOM DC voltage output pin	
35	VCAC	C	-	Power setting capacitor for VCOM AC	
36	DRV	P	-	VLED boost transistor driving signal	
37	VLED	P	Type 6	LED power anode	
38	FB	P	Type 7	LED power cathode	
39	VCOM	I	-	Panel common voltage	

I : Input, O : Output, C : Capacitor, P : Power, D : Dummy

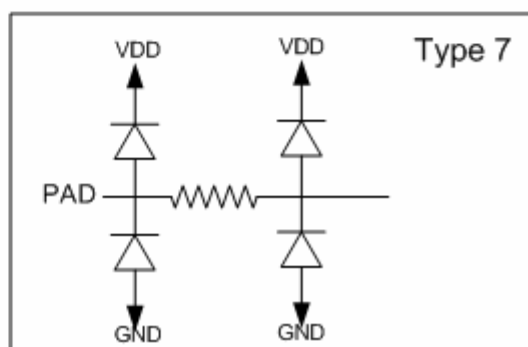
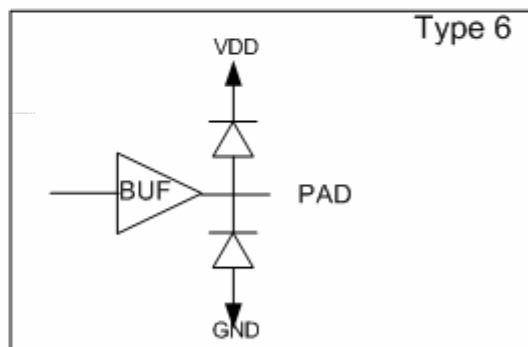
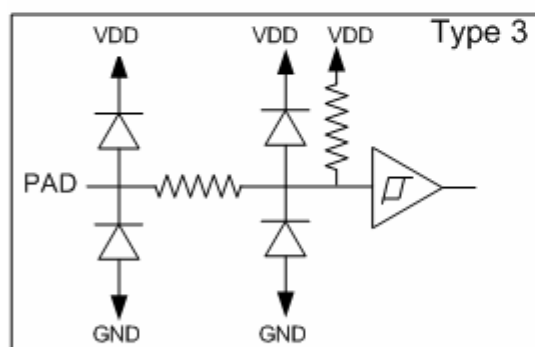
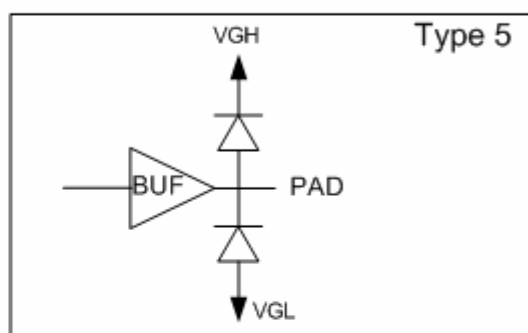
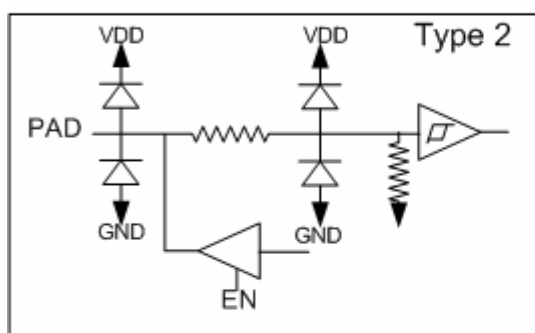
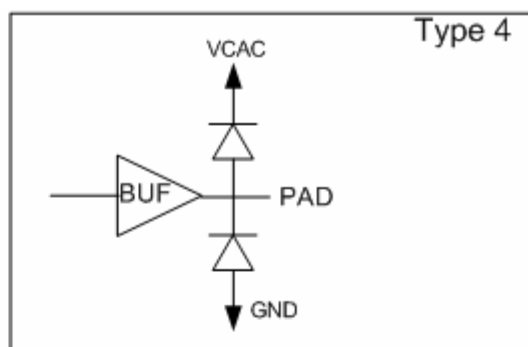
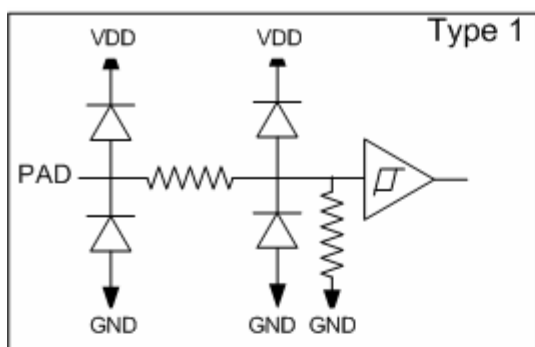
Note: Definition of scanning direction, Refer to figure as below :





# I/O Pin Structure:

Pull high/low resistor is **700k $\Omega$** .





A027DN03 V3 Product Spec	Version	0.3
	Page	10/63

## 2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VDD	AGND=GND=0V	-0.3	4.5	V	
TFT-LCD Power Voltage	VGH	AGND=GND=0V	-0.3	16	V	
	VGL	AGND=GND=0V	-16	0.3	V	
Input Signal Voltage	CS,SDA,SCL,Vsync, Hsync,DCLK,D0~D7	AGND=GND=0V	-0.3	4.5	V	
VCOM AC Output Voltage	FRP	AGND=GND=0V	-0.3	8	V	
VCOM AC Power Voltage	VCAC	AGND=GND=0V	-0.3	8	V	
VCOM DC Output Voltage	COMDC	AGND=GND=0V	-0.3	8	V	
VCOM Input Voltage	VCOM	AGND=GND=0V	-0.3	8	V	
Charge Pump Voltage	VDD2	AGND=GND=0V	-0.3	8	V	
	VDD3	AGND=GND=0V	-0.3	16	V	
	VDD5	AGND=GND=0V	-0.3	20	V	
	V1	AGND=GND=0V	-0.3	8	V	
	V2	AGND=GND=0V	-0.3	8	V	
	V3	AGND=GND=0V	-0.3	8	V	
	V4	AGND=GND=0V	-0.3	8	V	
	V5	AGND=GND=0V	-0.3	16	V	
	V6	AGND=GND=0V	-0.3	16	V	
	V7	AGND=GND=0V	-0.3	16	V	
	V8	AGND=GND=0V	-16	8	V	
Storage Temperature	Tstg	-	-25	80	°C	Ambient temperature
Operating Temperature	Topa	-	0	60	°C	Ambient temperature



A027DN03 V3 Product Spec	Version	0.3
	Page	11/63

### 3. Electrical characteristics

#### 3.1 Recommended operating conditions (GND=AGND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	VDD	3.0	3.3	3.6	V	Note 1
Input Signal	H Level	$V_{IH}$	$0.7 * VDD$	$VDD$	V	
	L Level	$V_{IL}$	GND	$0.3 * VDD$	V	

Note 1: A build-in power on reset circuit for VDD is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after VDD power on through serial control. Please refer to the register STB setting for detail.

#### 3.2 Electrical characteristics (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V <sub>DD</sub>	I <sub>DD</sub>	V <sub>DD</sub> =3.3V	-	8.2		mA	Note 1
	I <sub>DD(STANDBY)</sub>		-	0.2			Note 1
DC-DC voltage	V <sub>GH</sub>	V <sub>DD</sub> =3.3V		13		V	Note 2
	V <sub>GL</sub>	V <sub>DD</sub> =3.3V		-10		V	Note 2
VCOM voltage	V <sub>CAC</sub>	-	3.6	4.2	4.8	Vp-p	AC component, Note 3
	V <sub>CDC</sub>	-		0.5		V	DC component, Note 4

Note 1: Test Condition: 8colorbar+Grayscale pattern, UPS051 mode, DCLK=27MHz, Frame rate: 60Hz, other registers are default setting.

Note 2: V<sub>GH</sub> and V<sub>GL</sub> are output voltages of integrated LCD driver IC.

Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 4: V<sub>CDC</sub> could be adjusted, so as to minimize flicker and maximum contrast on each module.

### 3.3 Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

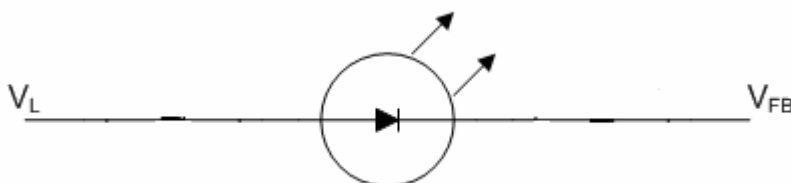
Pin name	Recommended value of capacitors ( $\mu$ F)	Withstanding voltage (V)
VGH	4.7 to 10	25
VGL	4.7 to 10	16
VDD5	4.7 to 10	25
VDD3	4.7 to 10	16
VDD2	4.7 to 10	10
DVDD	4.7 to 10	6.3
VCAC	4.7 to 10	10
V1, V2	2.2 to 10	10
V3, V4	2.2 to 10	10
V5, V6	2.2 to 10	16
V7, V8	2.2 to 10	16

### 3.4 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Backlight current			25	27.5	mA	Note 1,2
Backlight voltage	$V_L$		3.2	3.5	V	1pcs LED
Feedback voltage	$V_{FB}$	-	0.75	-	V	

Note1: To consider LED driver and feedback resistor tolerance.

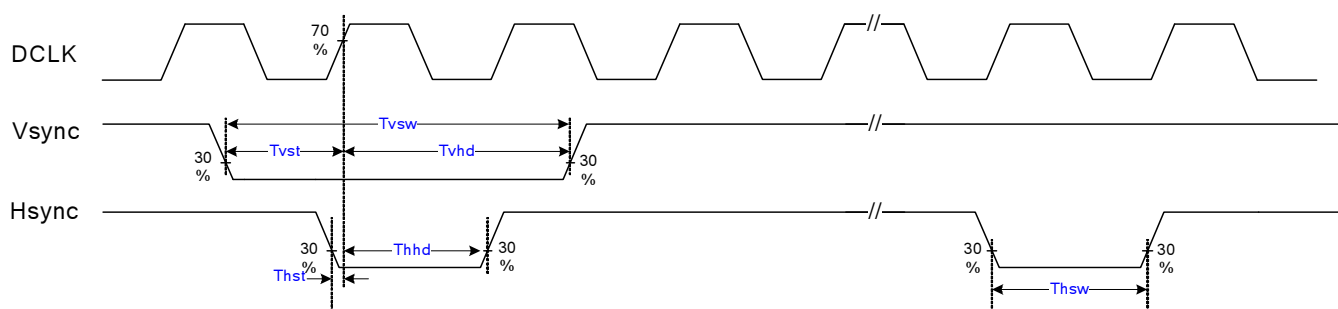
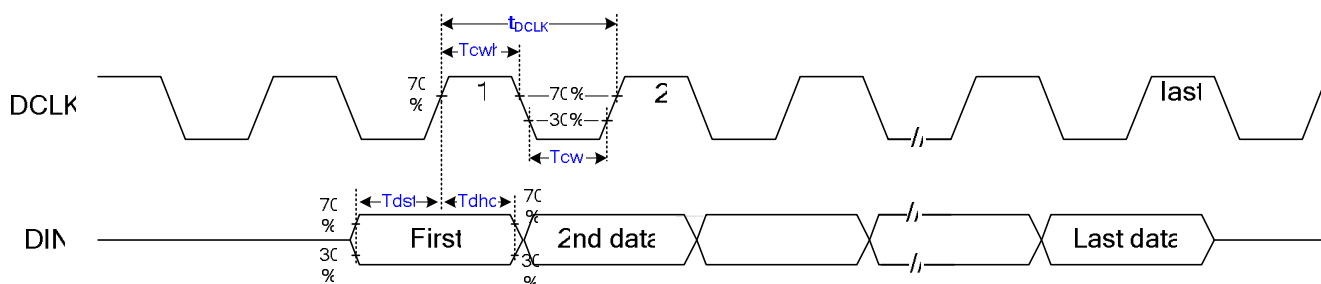
Note2: If using LCD internal LED driver controller the maximum setting should be 25mA.  $T_a=25^{\circ}\text{C}$



#### 4. Input timing AC characteristic

(VDD=3.0 ~3.6V, AGND=GND=0V, TA=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK duty cycle	T <sub>cw</sub>	40	50	60	%	
VSYNC setup time	T <sub>vst</sub>	6	-	-	ns	
VSYNC hold time	T <sub>vhd</sub>	6	-	-	ns	
HSYNC setup time	T <sub>hst</sub>	6	-	-	ns	
HSYNC hold time	T <sub>hhd</sub>	6	-	-	ns	
Data setup time	T <sub>dst</sub>	6	-	-	ns	
Data hold time	T <sub>dhd</sub>	6	-	-	ns	
HSYNC width	T <sub>hsw</sub>	1	1	254	t <sub>DCLK</sub>	
VSYNC width	T <sub>vsw</sub>	1 t <sub>DCLK</sub>	1 t <sub>DCLK</sub>	6t <sub>H</sub>		





A027DN03 V3 Product Spec	Version	0.3
	Page	14/63

## 5. Input timing format

### 5.1 UPS051 timing conditions (Refer to Fig.1 Fig.2 Fig.3)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark	
DCLK Frequency			1/t <sub>DCLK</sub>	13.5	27	27.19	MHz		
HSYNC	Period		t <sub>H</sub>	1024	1716	1728	t <sub>DCLK</sub>		
	Display period		t <sub>hd</sub>	960			t <sub>DCLK</sub>		
	Back porch		t <sub>hbp</sub>	50	70	255	t <sub>DCLK</sub>	Note 1	
	Front porch		t <sub>hfp</sub>	t <sub>H</sub> - t <sub>hd</sub> - t <sub>hbp</sub>			t <sub>DCLK</sub>		
	Pulse width		t <sub>hsw</sub>	1	1	t <sub>hbp</sub> - 1	t <sub>DCLK</sub>		
VSYNC	Period	Odd	t <sub>V</sub>	242.5	262.5	450.5	t <sub>H</sub>		
		Even							
	Display period	Odd	t <sub>vd</sub>	240			t <sub>H</sub>		
		Even							
	Back porch	Odd	t <sub>vb</sub>	1	21	31	t <sub>H</sub>	Note 2	
		Even		1.5	21.5	31.5			
	Front porch	Odd	t <sub>vfp</sub>	t <sub>V</sub> - t <sub>vd</sub> - t <sub>vb</sub>			t <sub>H</sub>		
		Even							
	Pulse width	Odd	t <sub>vsw</sub>	1 t <sub>DCLK</sub>	−1 t <sub>DCLK</sub>	6 t <sub>H</sub>			
		Even							
	1 frame				485	525	901	t <sub>H</sub>	

Note 1: The  $t_{hbp}$  time is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The  $t_{vbp}$  time is adjustable by setting register VBLK. UPS051 accepts both interlace and non-interlace vertical input timing.

Timing diagram for HSYNCP and DCLK signals. The diagram shows the relationship between HSYNCP, DCLK, and Data signals. Key timing parameters are labeled:  $t_H = t_{hbp} + t_{hd} + t_{hfp}$ ,  $t_{hsw}$ ,  $t_{hbp}$ ,  $t_{hd}$ , and  $t_{hfp}$ . The Data signal is shown as a sequence of bits (1, 2, 3, ..., 96) with "Invalid data" regions. The DCLK signal is a clock signal with a period of 1/96.

HSYNC

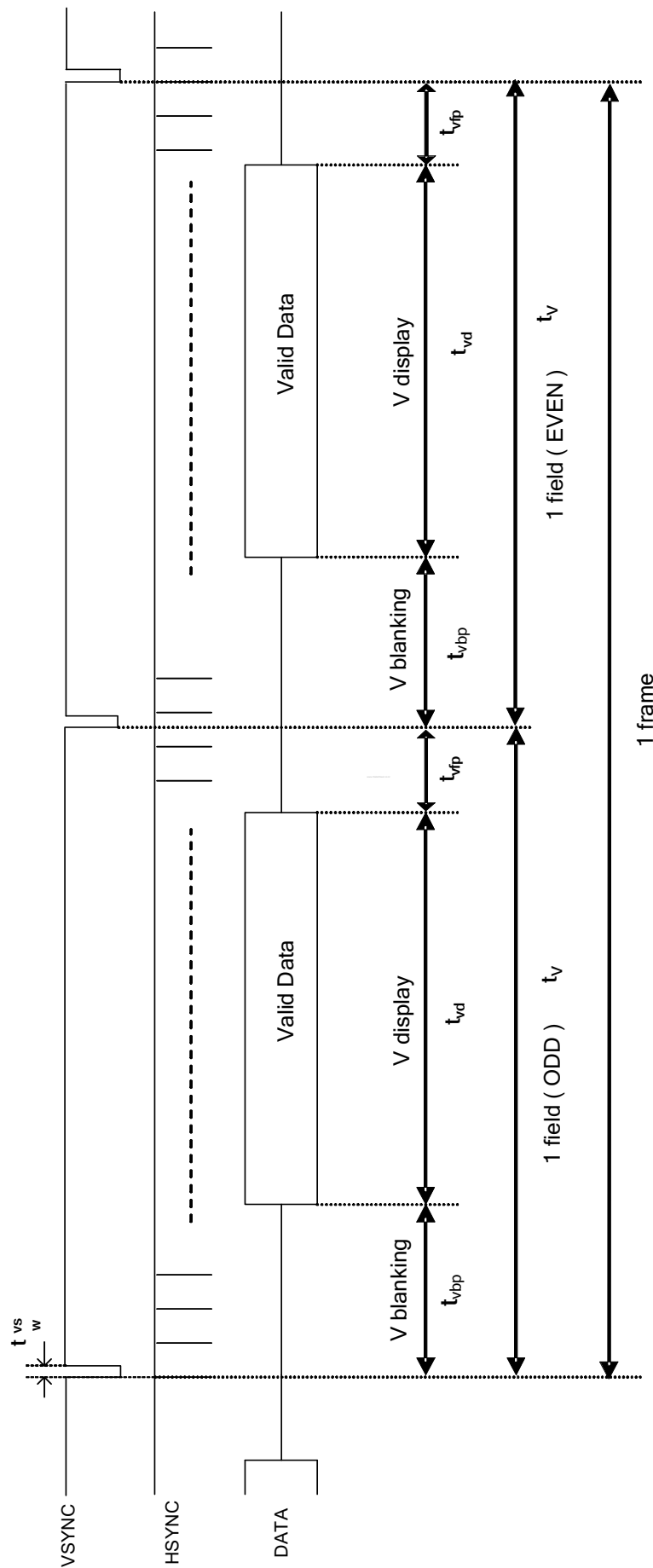
Line 1,3,5..239

R	G	B	R	G	B
---	---	---	---	---	---

Line 2,4,6..240

G	B	R	G	B	R
---	---	---	---	---	---

**Fig.3 UPS051 Input Vertical Timing Chart**





## 5.2 UPS052 timing

### 5.2.1 UPS052 (320 mode/NTSC/24.535MHz) timing specifications. (refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			1/t <sub>DCLK</sub>	20.54	24.535	30	MHz	
HSYNC	Period		t <sub>H</sub>	1306	1560	1907	t <sub>DCLK</sub>	
	Display period		t <sub>hd</sub>	-	1280	-	t <sub>DCLK</sub>	
	Back porch		t <sub>hbp</sub>	2	241	255	t <sub>DCLK</sub>	
	Front porch		t <sub>hfp</sub>	t <sub>H</sub> - t <sub>hd</sub> - t <sub>hbp</sub>			t <sub>DCLK</sub>	
	Pulse width		t <sub>hsw</sub>	1	1	200	t <sub>DCLK</sub>	
VSYNC	Period	Odd	t <sub>V</sub>	242.5	262.5	450.5	t <sub>H</sub>	
		Eve						
	Display period	Odd	t <sub>vd</sub>	-	240	-	t <sub>H</sub>	
		Eve						
	Back porch	Odd	t <sub>vbp</sub>	1	21	31	t <sub>H</sub>	
		Eve		1.5	21.5	31.5		
	Front porch	Odd	t <sub>vfp</sub>	t <sub>V</sub> - t <sub>vd</sub> - t <sub>vb</sub>			t <sub>H</sub>	
		Eve						
	Pulse width	Odd	t <sub>vsw</sub>	1	1	200	t <sub>DCLK</sub>	
		Eve						
	1 frame			485	525	901	t <sub>H</sub>	

### 5.2.2 UPS052 (320 mode/PAL/24.375MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			1/t <sub>DCLK</sub>	20.4	24.375	30	MHz	
HSYNC	Period		t <sub>H</sub>	1306	1560	1920	t <sub>DCLK</sub>	
	Display period		t <sub>hd</sub>	-	1280	-	t <sub>DCLK</sub>	
	Back porch		t <sub>hbp</sub>	3	241	255	t <sub>DCLK</sub>	
	Front porch		t <sub>hfp</sub>	t <sub>H</sub> - t <sub>hd</sub> - t <sub>hbp</sub>			t <sub>DCLK</sub>	
	Pulse width		t <sub>hsw</sub>	1	1	200	t <sub>DCLK</sub>	
VSYNC	Period	Odd	t <sub>V</sub>	292.5	312.5	450.5	t <sub>H</sub>	
		Eve						
	Display period	Odd	t <sub>vd</sub>	-	288	-	t <sub>H</sub>	
		Eve						
	Back porch	Odd	t <sub>vbp</sub>	3	24	34	t <sub>H</sub>	
		Eve		3.5	24.5	34.5		
	Front porch	Odd	t <sub>vfp</sub>	t <sub>V</sub> - t <sub>vd</sub> - t <sub>vb</sub>			t <sub>H</sub>	
		Eve						
	Pulse width	Odd	t <sub>vsw</sub>	1	1	200	t <sub>DCLK</sub>	
		Eve						
	1 frame				585	625	901	t <sub>H</sub>

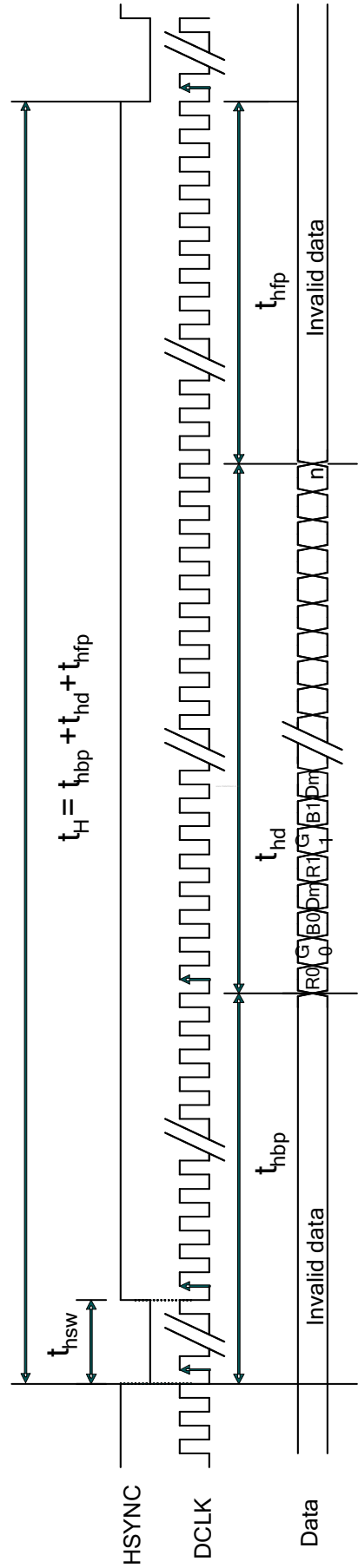
### 5.2.3 UPS052 (360 mode/NTSC/27MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			1/t <sub>DCLK</sub>	23	27	30	MHz	
HSYNC	Period		t <sub>H</sub>	1466	1716	1907	t <sub>DCLK</sub>	
	Display period		t <sub>hd</sub>	-	1440	-	t <sub>DCLK</sub>	
	Back porch		t <sub>hbp</sub>	2	241	255	t <sub>DCLK</sub>	
	Front porch		t <sub>hfp</sub>	t <sub>H</sub> - t <sub>hd</sub> - t <sub>hbp</sub>			t <sub>DCLK</sub>	
	Pulse width		t <sub>hsw</sub>	1	1	200	t <sub>DCLK</sub>	
VSYNC	Period	Odd	t <sub>V</sub>	242.5	262.5	450.5	t <sub>H</sub>	
		Even						
	Display period	Odd	t <sub>vd</sub>	-	240	-	t <sub>H</sub>	
		Even						
	Back porch	Odd	t <sub>vbp</sub>	1	21	31	t <sub>H</sub>	
		Even		1.5	21.5	31.5		
	Front porch	Odd	t <sub>vfp</sub>	t <sub>V</sub> - t <sub>vd</sub> - t <sub>vb</sub>			t <sub>H</sub>	
		Even						
	Pulse width	Odd	t <sub>vsw</sub>	1	1	200	t <sub>DCLK</sub>	
		Even						
	1 frame				485	525	901	t <sub>H</sub>

### 5.2.4 UPS052 (360 mode/PAL/27MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			1/t <sub>DCLK</sub>	23	27	30	MHz	
HSYNC	Period		t <sub>H</sub>	1466	1728	1920	t <sub>DCLK</sub>	
	Display period		t <sub>hd</sub>	-	1440	-	t <sub>DCLK</sub>	
	Back porch		t <sub>hbp</sub>	3	241	255	t <sub>DCLK</sub>	
	Front porch		t <sub>hfp</sub>	t <sub>H</sub> - t <sub>hd</sub> - t <sub>hbp</sub>			t <sub>DCLK</sub>	
	Pulse width		t <sub>hsw</sub>	1	1	200	t <sub>DCLK</sub>	
VSYNC	Period	Odd	t <sub>V</sub>	292.5	312.5	450.5	t <sub>H</sub>	
		Even						
	Display period	Odd	t <sub>vd</sub>	-	288	-	t <sub>H</sub>	
		Even						
	Back porch	Odd	t <sub>vbp</sub>	3	24	34	t <sub>H</sub>	
		Even		3.5	24.5	34.5		
	Front porch	Odd	t <sub>vfp</sub>	t <sub>V</sub> - t <sub>vd</sub> - t <sub>vb</sub>			t <sub>H</sub>	
		Even						
	Pulse width	Odd	t <sub>vsw</sub>	1	1	200	t <sub>DCLK</sub>	
		Even						
	1 frame				585	625	901	t <sub>H</sub>

**Fig.4 UPS052 Input Horizontal Timing Chart**



The diagram illustrates the timing of a video signal, showing the relationship between VSYNC, HSYNC, and DATA signals. The horizontal axis represents time, and the vertical axis represents the signal level.

**Signals:**

- VSYNC:** Vertical Sync signal, showing a pulse at the start of each field.
- HSYNC:** Horizontal Sync signal, showing pulses at the start of each line.
- DATA:** Data signal, showing a pulse at the start of each field.

**Timing Parameters:**

- $t_{vs}$ : Vertical Sync pulse width.
- $t_w$ : Vertical Sync pulse delay.
- $t_{vbp}$ : Vertical Blanking period.
- $t_{vdp}$ : Vertical Display period.
- $t_{vfp}$ : Vertical Front Porch period.
- $t_v$ : Total vertical period (1 field).

**Fields:**

- 1 field (EVEN):** The first field, starting with a VSYNC pulse.
- 1 field (ODD):** The second field, starting with a VSYNC pulse.

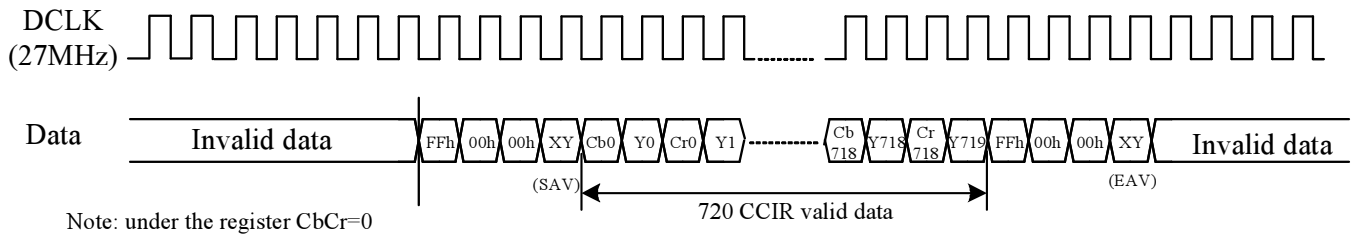
**Regions:**

- V blanking:** The period between the end of one field and the start of the next field.
- V display:** The period during which the video signal is displayed.
- Valid Data:** The period during which the data is valid and can be read.



A027DN03 V3 Product Spec	Version	0.3
	Page	21/63

### 5.3 CCIR656 Timing



**Fig.6 CCIR656 Data input format**

#### 5.3.1 CCIR656 decoding

- FF 00 00 < XY > signals are involved with HSYNC, VSYNC and Field

- <XY> encode following bits:

F=field select : F=0 for field 1, F=1 for field 2;

V=1 during vertical blanking

H=0 at SAV , H=1 at EAV ,

P3-P0=protection bits :

$P3 = V \oplus H$     $P2 = F \oplus H$     $P1 = F \oplus V$     $P0 = F \oplus V \oplus H$     $\oplus$ : represents the exclusive-OR function

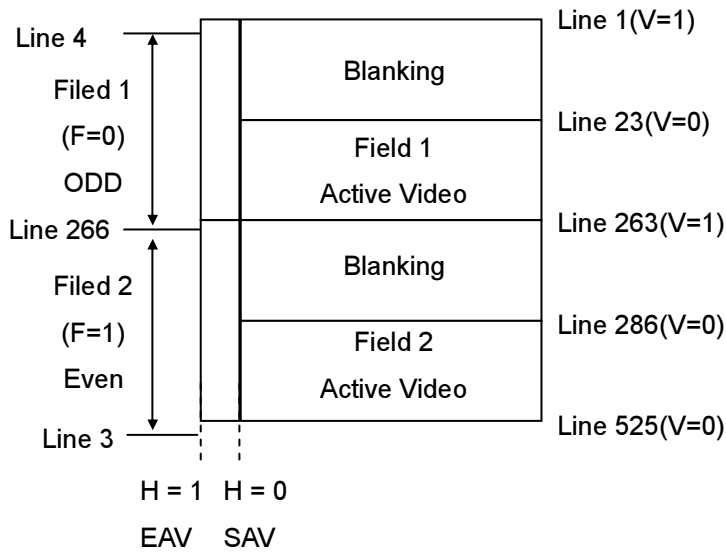
- Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.
- Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	F	V	H	P3	P2	P1	P0



A027DN03 V3 Product Spec	Version	0.3
	Page	22/63

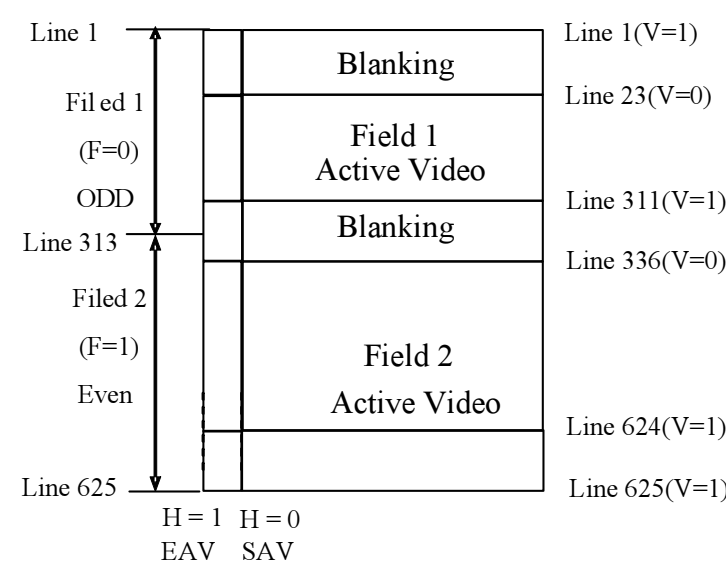
5.3.2 CCIR656 NTSC



Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

5.3.3 CCIR656 PAL



Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

## 5.4 YUV 720 and YUV 640 timing

### 5.4.1 YUV 720 mode/NTSC timing specifications (refer to Fig.7 Fig.9)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			1/t <sub>DCLK</sub>	23	27	30	MHz	
HSYNC	Period		t <sub>H</sub>	1476	1716	1907	t <sub>DCLK</sub>	
	Display period		t <sub>hd</sub>	-	1440	-	t <sub>DCLK</sub>	
	Back porch		t <sub>hbp</sub>	2	240	255	t <sub>DCLK</sub>	
	Front porch		t <sub>hfp</sub>	t <sub>H</sub> - t <sub>hd</sub> - t <sub>hbp</sub>			t <sub>DCLK</sub>	
	Pulse width		t <sub>hsw</sub>	-	1	-	t <sub>DCLK</sub>	
VSYNC	Period	Odd	t <sub>V</sub>	242.5	262.5	450.5	t <sub>H</sub>	
		Even						
	Display period	Odd	t <sub>vd</sub>	-	240	-	t <sub>H</sub>	
		Even						
	Back porch	Odd	t <sub>vbp</sub>	1	21	31	t <sub>H</sub>	
		Even		1.5	21.5	31.5		
	Front porch	Odd	t <sub>vfp</sub>	t <sub>V</sub> - t <sub>vd</sub> - t <sub>vb</sub>			t <sub>H</sub>	
		Even						
	Pulse width	Odd	t <sub>vsw</sub>	-	1	-	t <sub>DCLK</sub>	
		Even						
	1 frame				485	525	901	t <sub>H</sub>

### 5.4.2 YUV 720 mode/PAL timing specifications (refer to Fig.7 Fig.9)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	23	27	30	MHz	
	Period		$t_H$	1476	1728	1920	$t_{DCLK}$	
	Display period		$t_{hd}$	-	1440	-	$t_{DCLK}$	
	Back porch		$t_{hbp}$	3	240	255	$t_{DCLK}$	
	Front porch		$t_{hfp}$	$t_H - t_{hd} - t_{hbp}$			$t_{DCLK}$	
	Pulse width		$t_{hsw}$	-	1	-	$t_{DCLK}$	
VSYNC	Period	Odd	$t_V$	292.5	312.5	450.5	$t_H$	
		Even						
	Display period	Odd	$t_{vd}$	-	288	-	$t_H$	
		Even						
	Back porch	Odd	$t_{vbp}$	3	24	34	$t_H$	
		Even		3.5	24.5	34.5		
	Front porch	Odd	$t_{vfp}$	$t_V - t_{vd} - t_{vb}$			$t_H$	
		Even						
	Pulse width	Odd	$t_{vsw}$	-	1	-	$t_{DCLK}$	
		Even						
	1 frame				585	625	901	$t_H$

#### 5.4.3 YUV 640 mode/NTSC timing specifications (refer to Fig.8 Fig.9)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			1/t <sub>DCLK</sub>	20.65	24.535	30	MHz	
HSYNC	Period		t <sub>H</sub>	1314	1560	1907	t <sub>DCLK</sub>	
	Display period		t <sub>hd</sub>	-	1280	-	t <sub>DCLK</sub>	
	Back porch		t <sub>hbp</sub>	2	240	255	t <sub>DCLK</sub>	
	Front porch		t <sub>hfp</sub>	t <sub>H</sub> - t <sub>hd</sub> - t <sub>hbp</sub>			t <sub>DCLK</sub>	
	Pulse width		t <sub>hsw</sub>	-	1	-	t <sub>DCLK</sub>	
VSYNC	Period	Odd	t <sub>V</sub>	242.5	262.5	450.5	t <sub>H</sub>	
		Eve						
	Display period	Odd	t <sub>vd</sub>	-	240	-	t <sub>H</sub>	
		Eve						
	Back porch	Odd	t <sub>vbp</sub>	1	21	31	t <sub>H</sub>	
		Eve		1.5	21.5	31.5		
	Front porch	Odd	t <sub>vfp</sub>	t <sub>V</sub> - t <sub>vd</sub> - t <sub>vb</sub>			t <sub>H</sub>	
		Eve						
	Pulse width	Odd	t <sub>vsw</sub>	-	1	-	t <sub>DCLK</sub>	
		Eve						
1 frame				485	525	901	t <sub>H</sub>	

#### 5.4.4 YUV 640 mode/PAL timing specifications (refer to Fig.8 Fig.9)

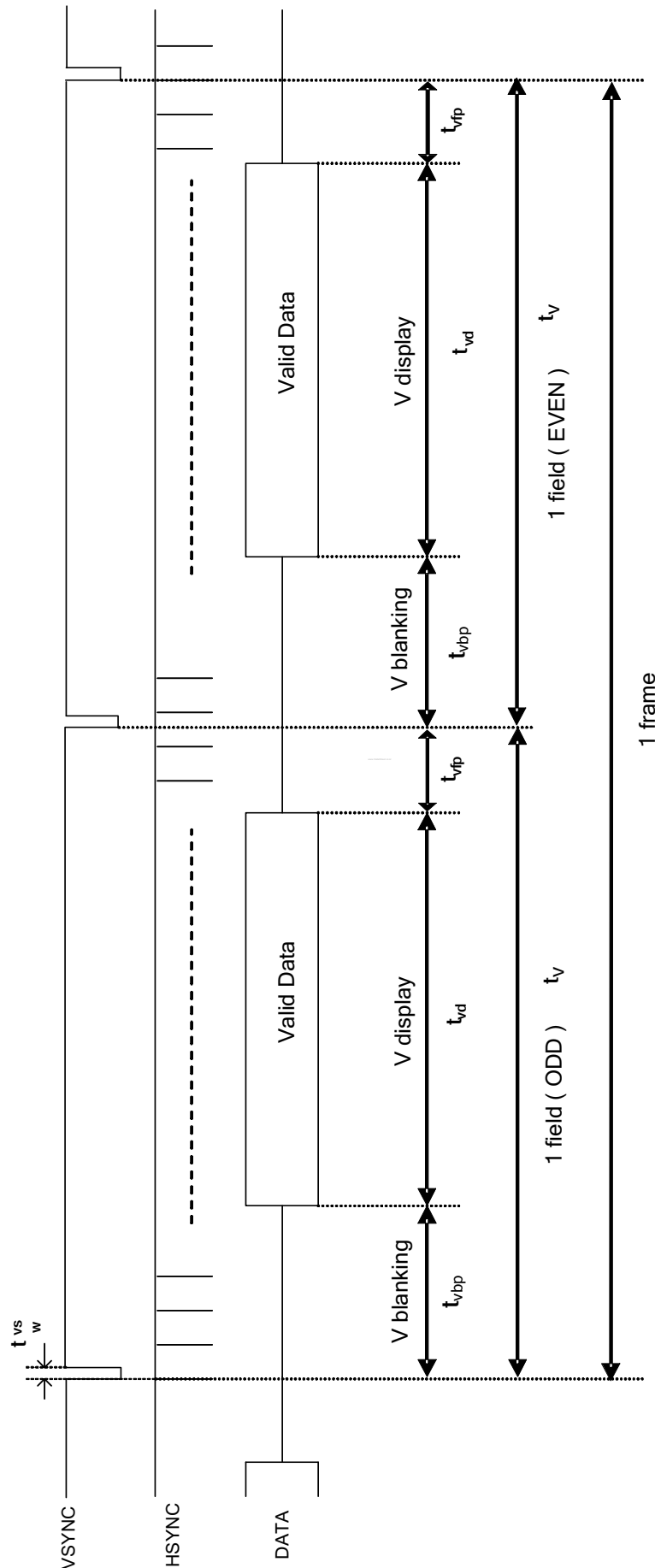
Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			1/t <sub>DCLK</sub>	20.5	24.375	30	MHz	
HSYNC	Period		t <sub>H</sub>	1314	1560	1920	t <sub>DCLK</sub>	
	Display period		t <sub>hd</sub>	-	1280	-	t <sub>DCLK</sub>	
	Back porch		t <sub>hbp</sub>	3	240	255	t <sub>DCLK</sub>	
	Front porch		t <sub>hfp</sub>	t <sub>H</sub> - t <sub>hd</sub> - t <sub>hbp</sub>			t <sub>DCLK</sub>	
	Pulse width		t <sub>hsw</sub>	-	1	-	t <sub>DCLK</sub>	
VSYNC	Period	Odd	t <sub>V</sub>	292.5	312.5	450.5	t <sub>H</sub>	
		Eve						
	Display period	Odd	t <sub>vd</sub>	-	288	-	t <sub>H</sub>	
		Eve						
	Back porch	Odd	t <sub>vbp</sub>	3	24	34	t <sub>H</sub>	
		Eve						3.5
	Front porch	Odd	t <sub>vfp</sub>	t <sub>V</sub> - t <sub>vd</sub> - t <sub>vb</sub>			t <sub>H</sub>	
		Eve						
	Pulse width	Odd	t <sub>vs<sub>w</sub></sub>	-	1	-	t <sub>DCLK</sub>	
		Eve						
1 frame				585	625	901	t <sub>H</sub>	



Timing diagram for NTSC/PAL video signals. The diagram shows the relationship between HSYNC, DCLK, and Data signals. Key parameters include  $t_H$  (horizontal sync period),  $t_{hsw}$  (horizontal sync width),  $t_{hbp}$  (horizontal blanking period),  $t_{hfp}$  (horizontal front porch period), and  $t_{hd}$  (horizontal delay). The data stream is divided into invalid data and valid data regions. The valid data region is further divided into Y, Cb, and Cr components. The diagram shows that the data is sampled at the midpoint of the horizontal sync period, ensuring that the data is valid and stable.

[illegible]

Fig.9 YUV Input Vertical Timing Chart





A027DN03 V3 Product Spec	Version	0.3
	Page	27/63

#### 5.5 CCIR656/YUV 720/YUV 640 to RGB conversion

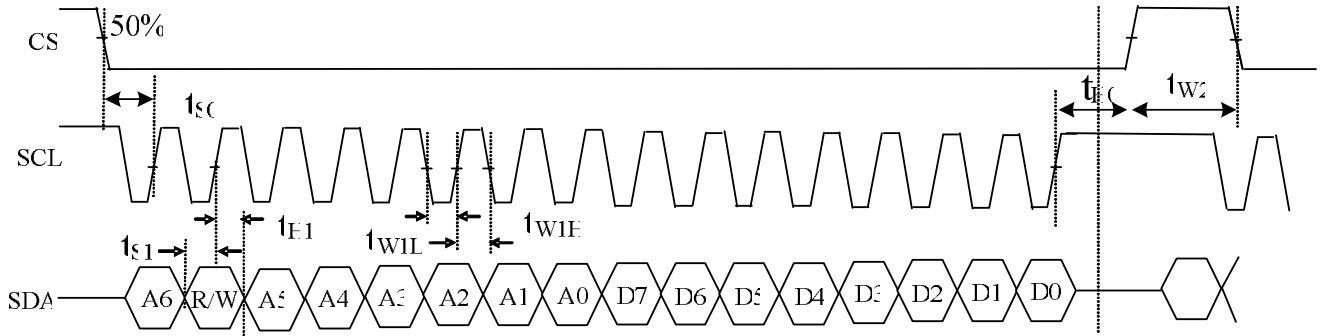
$$R_n = 1.164 * [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 1.596 * (C_{rn} - 128)$$

$$G_n = 1.164 * [(Y_{2n-1} + Y_{2n}) / 2 - 16] - 0.813 * (C_{rn} - 128) - 0.392 * (C_{bn} - 128)$$

$$B_n = 1.164 * [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 2.017 * (C_{bn} - 128)$$

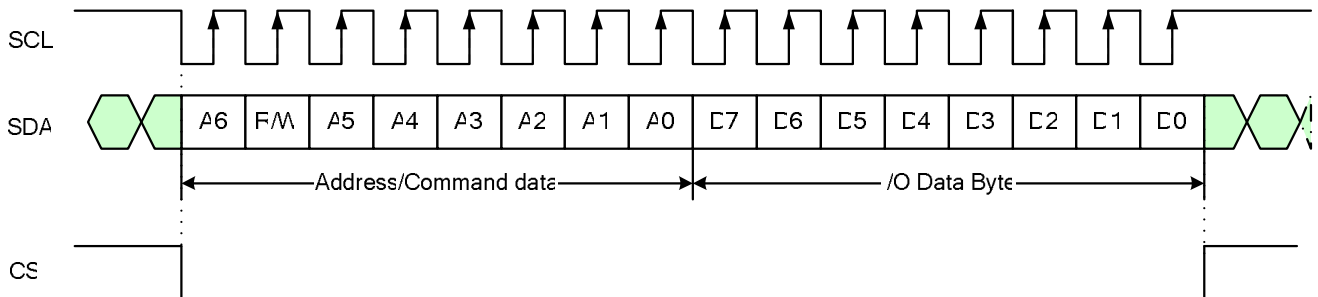
Where Y:16~235      C<sub>r</sub>:16~240      C<sub>b</sub>:16~240

## 6. Serial control interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	$t_{S0}$	50	-	-	ns
Serial data input setup Time	$t_{S1}$	50	-	-	ns
CS input hold Time	$t_{H0}$	50	-	-	ns
Serial data input hold Time	$t_{H1}$	50	-	-	ns
SCL pulse low width	$t_{W1L}$	50	-	-	ns
SCL pulse high width	$t_{W1H}$	50	-	-	ns
CS pulse high width	$t_{W2}$	400	-	-	ns

### 6.1 Timing chart



- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data after the falling edge of CS pulse are valid data.
- Serial block operates with the SCL clock.
- Serial data can be accepted in the standby (power save) mode.



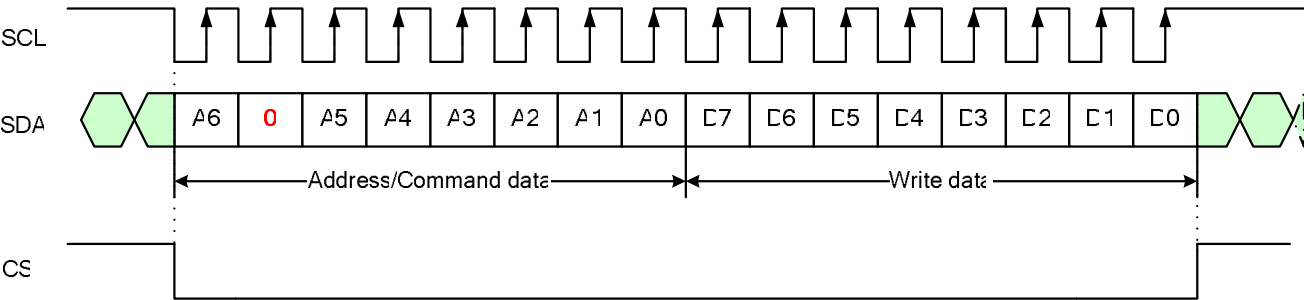
A027DN03 V3 Product Spec	Version	0.3
	Page	29/63

6.2 The configuration of serial data at SDA terminal is at below

MSB								LSB							
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Address	R/W	Address						DATA							

R/W: Establishes the Read mode when set to '1', and the Write mode when set to '0'.

Write Mode:





A027DN03 V3 Product Spec	Version	0.3
	Page	30/63

### 6.3 Register table

No.	Register address								MSB		Register data (default setting)						LSB	
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
R0	0	0	0	0	0	0	0	0	Y_CbCr (0)	CCIR601 (0)	x	x	VCAC (0)	VCOM_AC (011)				
R1	0	0	0	0	0	0	0	1	VCDCE (1)	x	VCOM_DC (0Ah)							
R3	0	0	0	0	0	0	1	1	Brightness (40h)									
R4	0	0	0	0	0	1	0	0	Narrow (0)	YUV (0)	SEL (00)	NTSC/PAL (10)		VDIR (1)	HDIR (1)			
R5	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	PFM_DUTY (011)		SHDB2 (1)	SHDB1 (1)	STB (0)			
R6	0	0	0	0	0	1	1	0	HBLK_EN (0)	LED_Current (00)	VBLK (15h)							
R7	0	0	0	0	0	1	1	1	HBLK(46h)									
R8	0	0	0	0	1	0	0	0	BL_DRV (00)		x	x	x	x	x	x		
R12	0	0	0	0	1	1	0	0	PAIR (00)		x	CbCr (0)	x	Vdpol (1)	Hdpol (1)	DCLKpol (0)		
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB (40h)									
R14	0	0	0	0	1	1	1	0	x	SUB-CONTRAST_R (40h)								
R15	0	0	0	0	1	1	1	1	x	SUB-BRIGHTNESS_R (40h)								
R16	0	0	0	1	0	0	0	0	x	SUB-CONTRAST_B (40h)								
R17	0	0	0	1	0	0	0	1	x	SUB-BRIGHTNESS_B (40h)								
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE (0111)				LED_ON_RATIO (1111)					
R48	0	0	1	1	0	0	0	0	x	x	GMA_V0+(100001)							
R49	0	0	1	1	0	0	0	1	x	x	GAM_V3+(101100)							
R50	0	0	1	1	0	0	1	0	x	x	GMA_V6+(110100)							
R51	0	0	1	1	0	0	1	1	x	x	x	GMA_V8+(01101)						
R52	0	0	1	1	0	1	0	0	x	x	x	GMA_V11+(01011)						
R53	0	0	1	1	0	1	0	1	x	x	x	GMA_V15+(10101)						
R54	0	0	1	1	0	1	1	0	x	x	x	x	GMA_V20+(1111)					
R55	0	0	1	1	0	1	1	1	x	x	x	x	GMA_V25+(1011)					
R56	0	0	1	1	1	0	0	0	x	x	x	x	GMA_V38+(0000)					
R57	0	0	1	1	1	0	0	1	x	x	x	x	GMA_V43+(1000)					
R58	0	0	1	1	1	0	1	0	x	x	x	GMA_V48+(00110)						
R59	0	0	1	1	1	0	1	1	x	x	x	GMA_V52+(01001)						



A027DN03 V3 Product Spec	Version	0.3
	Page	31/63

R60	0	0	1	1	1	1	0	0	x	x	x	GMA_V55+(01011)					
R61	0	0	1	1	1	1	0	1	x	x	GMA_V57+(010100)						
R62	0	0	1	1	1	1	1	0	x	x	GMA_V60+(001111)						
R63	0	0	1	1	1	1	1	1	x	x	GMA_V63+(000001)						
R64	1	0	0	0	0	0	0	0	x	x	GMA_V63-(100001)						
R65	1	0	0	0	0	0	0	1	x	x	GMA_V60-(110000)						
R66	1	0	0	0	0	0	1	0	x	x	GMA_V57-(110100)						
R67	1	0	0	0	0	0	1	1	x	x	x	GMA_V55-(01100)					
R68	1	0	0	0	0	1	0	0	x	x	x	GMA_V52-(01011)					
R69	1	0	0	0	0	1	0	1	x	x	x	GMA_V48-(00111)					
R70	1	0	0	0	0	1	1	0	x	x	x	x	GAM_V43-(1000)				
R71	1	0	0	0	0	1	1	1	x	x	x	x	GMA_V38-(0000)				
R72	1	0	0	0	1	0	0	0	x	x	x	x	GMA_V25-(1010)				
R73	1	0	0	0	1	0	0	1	x	x	x	x	GMA_V20-(1111)				
R74	1	0	0	0	1	0	1	0	x	x	x	GAM_V15-(10100)					
R75	1	0	0	0	1	0	1	1	x	x	x	GMA_V11-(01010)					
R76	1	0	0	0	1	1	0	0	x	x	x	GMA_V8-(01100)					
R77	1	0	0	0	1	1	0	1	x	x	GMA_V6-(010100)						
R78	1	0	0	0	1	1	1	0	x	x	GMA_V3-(001100)						
R79	1	0	0	0	1	1	1	1	x	x	GMA_V0-(000001)						
R86	1	0	0	1	0	1	1	0	x	x	x	x	0	1	VGH_SEL(11)		
R97	1	0	1	0	0	0	0	1	X	x	x	X	x	x	x	GAMMA setting (0)	

Note: 1. "x" => please set to '0'.

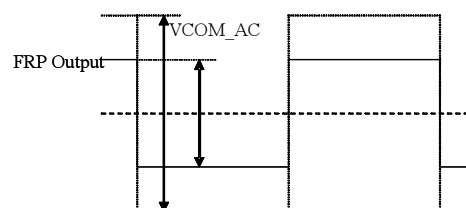
## 6.4 Register description

R0:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr(0)	CCIR601 (0)	x	x	VCAC(0)	VCOM_AC(011)		

VCOM\_AC: Common voltage AC level selection (deviation  $\pm 0.1V$ )

VCOM_AC			VCAC	Voltage (V)
D2	D1	D0	D3	
0	0	0	0	3.6
0	0	0	1	3.7
0	0	1	0	3.8
0	0	1	1	3.9
0	1	0	0	4.0
0	1	0	1	4.1
0	1	1	0	4.2(Default)
0	1	1	1	4.3
1	0	0	0	4.4
1	0	0	1	4.5
1	0	1	0	4.6
1	0	1	1	4.7
1	1	X	X	4.8



CCIR601: CCIR601 input timing selection

CCIR601	Function
0(Default)	Disable CCIR601 (Default)
1	Enable CCIR601. (Please refer to the table of R4(SEL) for detail description)

Y\_CbCr: Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

	CbCr(R12[4])='0'	CbCr(R12[4])='1'
Y_CbCr='0' (Default)	Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3	Cr0 Y0 Cb0 Y1 Cr2 Y2 Cb2 Y3
Y_CbCr='1'	Y0 Cb0 Y1 Cr0 Y2 Cb2 Y3 Cr2	Y0 Cr0 Y1 Cb0 Y2 Cr2 Y3 Cb2





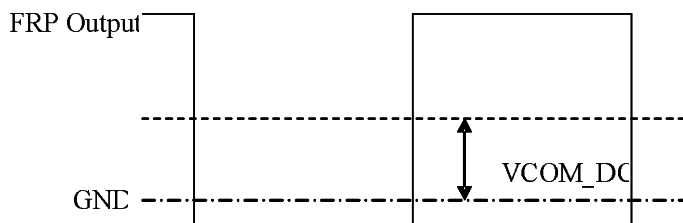
A027DN03 V3 Product Spec	Version	0.3
	Page	33/63

R1:

No	Register address								MSB	Register data								LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
R1	0	0	0	0	0	0	0	1	VCDCE (1)	x	VCOM_DC (0Ah)							

VCOM\_DC: Common voltage DC level selection (20mV/step)

D5~D0	VCOM DC level (V)
00h	0.10
:	:
0Ah(Default)	0.30(Default)
:	:
3Fh	1.36



VCDCE: VCOM\_DC function enable setting

VCDCE	Function
0	VCOM_DC function disable. The COMDC pin is Hi-Z.
1	VCOM_DC function enable. The COMDC voltage follows VCOM_DC setting. (Default)

R3:

No.	Register address								Register data								MSB	LSB						
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0								
R3	0	0	0	0	0	0	1	1	Brightness (40h)															

BRIGHTNESS: RGB bright level setting, setting accuracy: 1 step / bit

D7 ~ D0	Brightness gain
00h	Dark (-64)
40h(Default)	Center (0) (Default)
FFh	Bright (+191)



A027DN03 V3 Product Spec	Version	0.3
	Page	34/63

R4:

No.	Register address								MSB	Register data								LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
R4	0	0	0	0	0	1	0	0	Narrow(0)	YUV(0)	SEL(00)		NTSC/PAL(10)		VDIR(1)	HDIR(1)		

HDIR: Horizontal scan direction setting

HDIR	Function
0	Right to left scan
1	Left to right scan (Default)

VDIR: Vertical scan direction setting

VDIR	Function
0	Down to up scan
1	Up to down scan (Default)

NTSC/PAL: NTSC or PAL input mode selection (for UPS052 input timing)

NTSC/PAL		Mode
D3	D2	
0	0	PAL
0	1	NTSC
1	X	Auto detection (Default)

SEL: Input data timing format selection

CCIR601	YUV	SEL		INPUT TIMING FORMAT
		D5	D4	
0	0	0	0	UPS051 (Default)
0	0	0	1	UPS052 320 × 240
0	0	1	X	UPS052 360 × 240
0	1	1	0	CCIR656
1	1	0	X	YUV 640(*)
1	1	1	X	YUV 720(*)

(\*)Please refer to YUV640/YUV720 horizontal timing spec for detailed description.

A027DN03 V3 Product Spec	Version	0.3
	Page	35/63

YUV: YUV (CCIR656, YUV640, YUV720) or RGB input selection

YUV	Function
0	RGB input ( Default)
1	CCIR656 / YUV640 / YUV720 input.

When this command is sent to driver ic,it will be executed immediately

Narrow: Normal display and Narrow display selection.

Narrow	Function
0	Normal display (Default)
1	Narrow Display



Narrow=0



Narrow=1



A027DN03 V3 Product Spec	Version	0.3
	Page	36/63

R5:

No	Register address								Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5	0	0	0	0	0	1	0	1	DRV_FREQ(0)	GRB(1)	PFM_DUTY(011)		SHDB2(1)	SHDB1(1)	STB(0)	

STB: Standby (Power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

SHDB1: Shut down for back light power converter

SHDB1	Function
0	The back light power converter is off
1	The back light power converter is controlled by power on/off sequence (Default)

SHDB2: Shut down for VGH/VGL charge pump

SHDB2	Function
0	VGH/VGL charge pump is always off
1	VGH/VGL charge pump is controlled by power on/off sequence (Default)

PFM\_DUTY: PFM duty cycle selection for back light power converter

PFM_DUTY			Function
D5	D4	D3	PFM duty cycle
0	0	0	50%
0	0	1	60%
0	1	0	65%
0	1	1	70%(Default)
1	0	0	75%
1	0	1	80%
1	1	0	85%
1	1	1	90%

GRB: Register reset setting

GRB	Function
0	Reset all registers to default value
1	Normal operation (Default)

When this command is sent to driver ic, it will be executed immediately

DRV\_FREQ: DRV signal frequency setting

DRV_FREQ	DRV frequency
0(Default)	DCLK / 64
1	DCLK / 128



A027DN03 V3 Product Spec	Version	0.3
	Page	37/63

R6:

No	Register address								MSB	Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)							VBLK(15h)

VBLK: Vertical blanking setting

UPS051, UPS052, YUV640 and YUV720 NTSC mode

D4 ~ D0	VBLK	Unit
01h	1	H (line)
15h	21(Default)	
1Fh	31	

CCIR656 NTSC mode

D4 ~ D0	VBLK	Unit
01h	1	H (line)
16h	22(Default)	
1Fh	31	

UPS052, CCIR656 and YUV640 and YUV720 PAL mode(Vertical blanking + 3)

D4 ~ D0	VBLK	Unit
00h	3	H (line)
15h	24(Default)	
1Fh	34	

Note: V-blanking must be adjusted based on the input data.

LED\_CURRENT: adjust LED current

DC-DC feedback voltage

D6	D5	Feedback Threshold voltage
0	0	0.6V(20mA) (default)
0	1	0.75V(25mA)
1	0	0.45V(15mA)
1	1	0.3V(10mA)



A027DN03 V3 Product Spec	Version	0.3
	Page	38/63

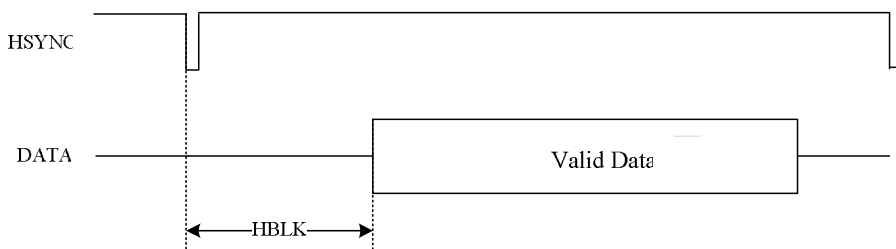
#### R6 & R7:

No	Register address								MSB	Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)							VLBK(15h)
R7	0	0	0	0	0	1	1	1									HBLK(46h)

#### HBLK\_EN & HBLK: Horizontal blanking setting

HBLK_EN	HBLK(D7~D0)	HBLK	Unit	Remark
x	32h	50	DCLK(*)	UPS051
x	46h	70(Default)		
x	FFh	255		
0	-	241(fixed)	DCLK(*)	UPS052
1	02h~FF	2~255	DCLK(*)	
0	-	240(fixed)	DCLK(*)	YUV640, YUV720
1	02h ~ FFh	2 ~ 255	DCLK(*)	

\*The frequency of DCLK is different under different input timing.



#### R8:

No.	Register address								MSB	Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		x	x	x	x	x	x	

#### BL\_DRV: Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability (Default)
0	1	2 times the Normal capability
1	0	4 times the Normal capability
1	1	8 times the Normal capability



A027DN03 V3 Product Spec	Version	0.3
	Page	39/63

#### R12:

No.	Register address								Register data								LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R12	0	0	0	0	1	1	0	0	PAIR(00)		x	CbCr(0)		x	Vdpol(1)	Hdpol(1)	DCLKpol(0)

DCLKpol: DCLK polarity selection

DCLKpol	Function
0	Positive polarity (Default)
1	Negative polarity

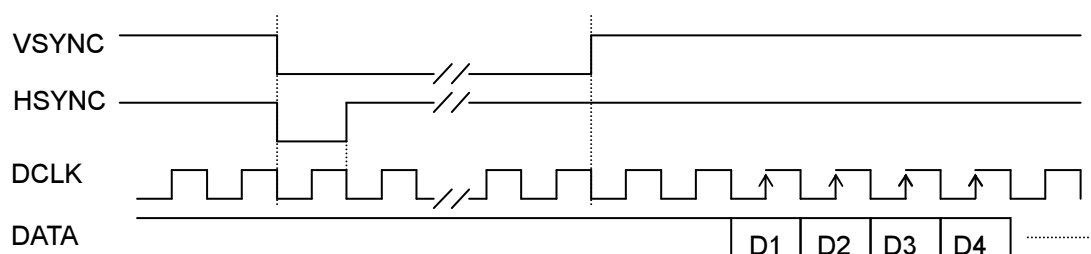
HDpol: HSYNC polarity selection

HDpol	Function
0	Positive polarity
1	Negative polarity (Default)

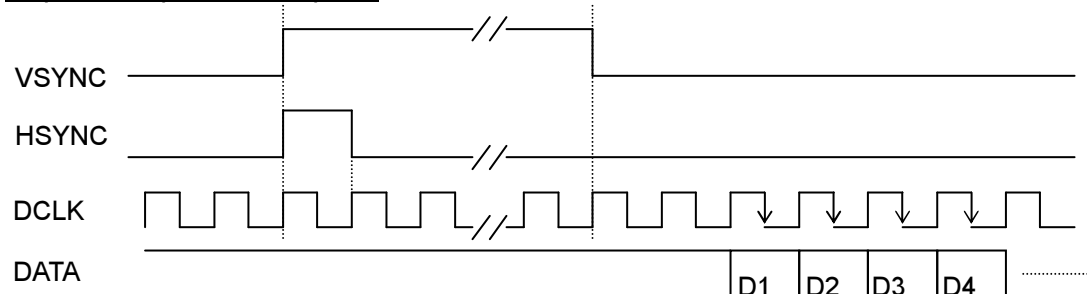
VDpol: VSYNC polarity selection

VDpol	Function
0	Positive polarity
1	Negative polarity (Default)

HDpol=1, VDpol=1, DCLKpol=0



HDpol=0, VDpol=0, DCLKpol=1





A027DN03 V3 Product Spec	Version	0.3
	Page	40/63

CbCr: Cb & Cr exchange position, (Please refer to the table of R0( Y\_CbCr) for detail description)

CbCr='0'		Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3
CbCr='1'		Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3

PAIR: Vertical start time setting for Odd/Even frame

UPS051 / UPS052 NTSC / UPS052 PAL (\*)

PAIR		VBK	Unit
D7	D6	ODD/EVEN	
x	0	21/21(Default)	H (line)
x	1	21/20	

CCIR656/YUV640/YUV720 NTSC/PAL (\*\*)

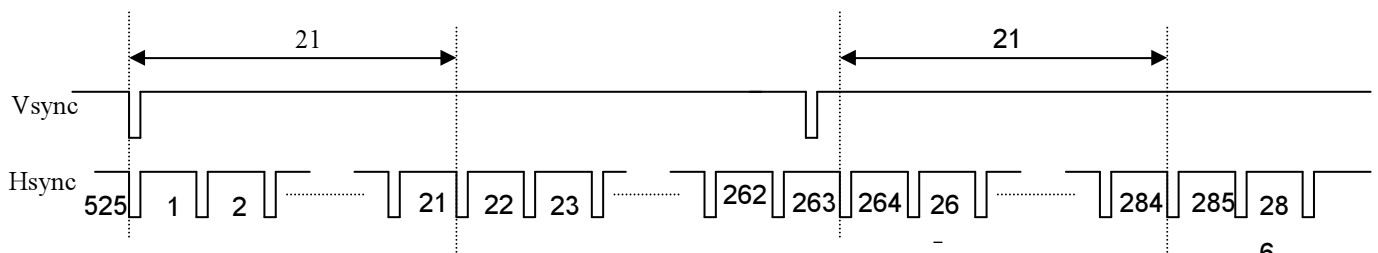
PAIR		VBK	Unit
D7	D6	ODD/EVEN	
0	0	22/22	H (line)
0	1	22/23	
1	0	23/22	
1	1	23/23	

(\*)The typical value of VBK of UPS052 PAL(24 H) is different than UPS051/UPS052 NTSC(21H).

(\*\*) The typical value of VBK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(22H).

Note: V-blanking must be adjusted based on the input data.

For example:



		PAIR=0		PAIR=1	
Field \ Line		START	END	START	END
ODD		22	261	22	261
EVEN		285	524	284	523

This table is based on VBK=21.





A027DN03 V3 Product Spec	Version	0.3
	Page	41/63

**R13:**

No.	Register address								MSB	Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB(40h)								

CONTRAST\_RGB: RGB contrast level setting, the gain changes (1/64) / bit

D7 ~ D0	Contrast gain
00h	0
40h	1(Default)
FFh	3.984

**R14~R17:**

No.	Register address								MSB	Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R14	0	0	0	0	1	1	1	0	x	SUB-CONTRAST_R(40h)							
R16	0	0	0	1	0	0	0	0	x	SUB-CONTRAST_B(40h)							

SUB-CONTRAST: R/B sub-contrast level setting, the gain changes (1/256) / bit

D6 ~ D0	Brightness gain
00h	0.75
40h	1(Default)
7Fh	1.246

No.	Register address								MSB	Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R15	0	0	0	0	1	1	1	1	x	SUB-BRIGHTNESS_R(40h)							
R17	0	0	0	1	0	0	0	1	x	SUB-BRIGHTNESS_B(40h)							

SUB-BRIGHTNESS: R/B sub-bright level setting, setting accuracy : 1 step / bit

D6 ~ D0	Brightness gain
00h	Dark (-64)
40h	Center (0)(Default)
7Fh	Bright (+63)



A027DN03 V3 Product Spec	Version	0.3
	Page	42/63

R21:

No.	Register address								MSB	Register data								LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE (0111)				LED_ON_RATIO (1111)					

LED\_ON\_RATIO: Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.

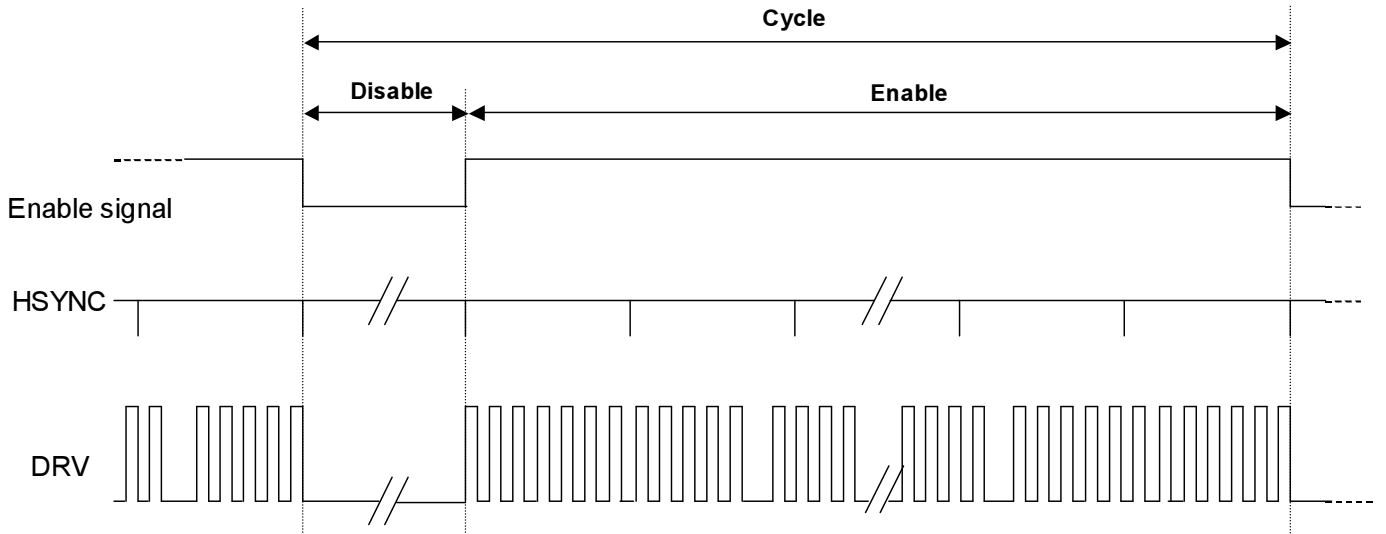
LED_ON_RATIO				Value
D3	D2	D1	D0	
0	0	0	0	1/16
0	0	0	1	2/16
0	0	1	0	3/16
0	0	1	1	4/16
0	1	0	0	5/16
0	1	0	1	6/16
0	1	1	0	7/16
0	1	1	1	8/16
1	0	0	0	9/16
1	0	0	1	10/16
1	0	1	0	11/16
1	0	1	1	12/16
1	1	0	0	13/16
1	1	0	1	14/16
1	1	1	0	15/16
1	1	1	1	16/16(Default)

LED\_ON\_CYCLE : Set the cycle of enable signal , and we can use it to adjust brightness of the LEDs.

LED_ON_CYCLE				Value
D7	D6	D5	D4	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8(Default)
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16



A027DN03 V3 Product Spec	Version	0.3
	Page	43/63



$$16 * \text{LED\_ON\_CYCLE} = \text{LED\_ON\_CYCLE} * (\text{LED\_ON\_RATIO} * 16) + \text{LED\_ON\_CYCLE} * (16 - \text{LED\_ON\_RATIO} * 16)$$

(Cycle)

(Enable)

(Disable)

Unit : HSYNC

for example:

LED\_ON\_RATIO is "1001", and LED\_ON\_CYCLE is "0111", then:

Cycle =  $16 * 8 = 128$ (HSYNC)

Enable =  $8 * ((10/16) * 16) = 80$ (HSYNC)

Disable =  $8 * (16 - (10/16) * 16) = 48$ (HSYNC) → 62.5% on

#### R48 ~ R79:

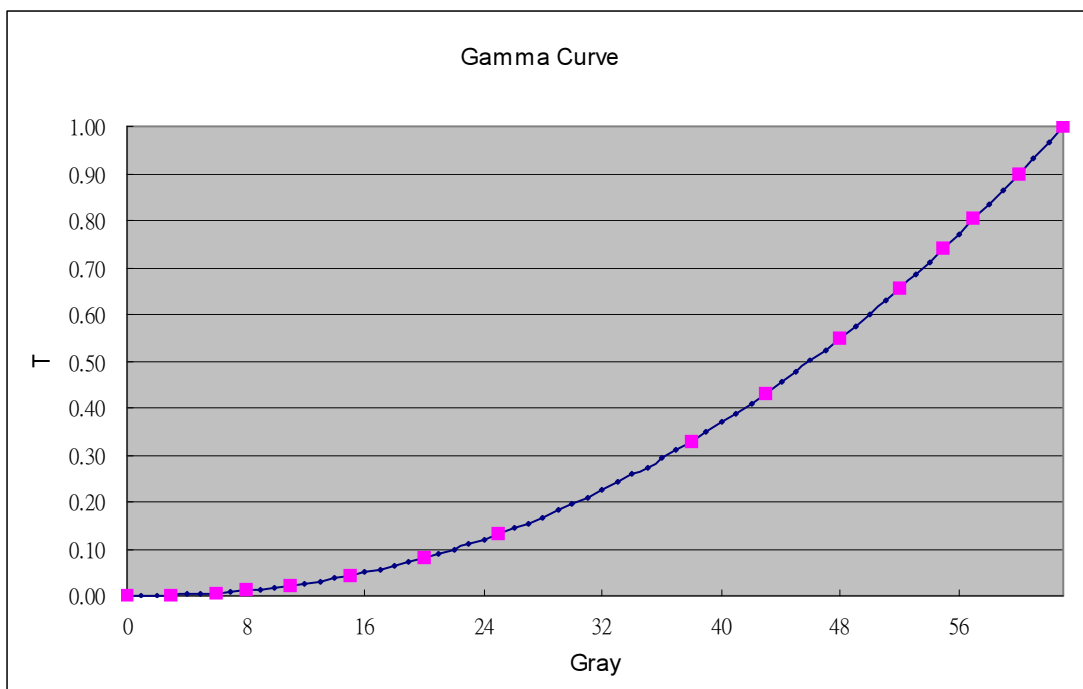
No.	Register address								MSB		Register data						LSB	
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
R48	0	0	1	1	0	0	0	0	x	x	GMA_V0+(100001)							
R49	0	0	1	1	0	0	0	1	x	x	GAM_V3+(101100)							
R50	0	0	1	1	0	0	1	0	x	x	GMA_V6+(110100)							
R51	0	0	1	1	0	0	1	1	x	x	x	GMA_V8+(01101)						
R52	0	0	1	1	0	1	0	0	x	x	x	GMA_V11+(01011)						
R53	0	0	1	1	0	1	0	1	x	x	x	GMA_V15+(10101)						
R54	0	0	1	1	0	1	1	0	x	x	x	x	GMA_V20+(1111)					
R55	0	0	1	1	0	1	1	1	x	x	x	x	GMA_V25+(1011)					
R56	0	0	1	1	1	0	0	0	x	x	x	x	GMA_V38+(0000)					
R57	0	0	1	1	1	0	0	1	x	x	x	x	GMA_V43+(1000)					
R58	0	0	1	1	1	0	1	0	x	x	x	GMA_V48+(00110)						
R59	0	0	1	1	1	0	1	1	x	x	x	GMA_V52+(01001)						
R60	0	0	1	1	1	1	0	0	x	x	x	GMA_V55+(01011)						
R61	0	0	1	1	1	1	0	1	x	x	GMA_V57+(010100)							



A027DN03 V3 Product Spec	Version	0.3
	Page	44/63

R62	0	0	1	1	1	1	1	0	x	x	GMA_V60+(001111)			
R63	0	0	1	1	1	1	1	1	x	x	GMA_V63+(000001)			
R64	1	0	0	0	0	0	0	0	x	x	GMA_V63-(100001)			
R65	1	0	0	0	0	0	0	1	x	x	GMA_V60-(110000)			
R66	1	0	0	0	0	0	1	0	x	x	GMA_V57-(110100)			
R67	1	0	0	0	0	0	1	1	x	x	x	GMA_V55-(01100)		
R68	1	0	0	0	0	1	0	0	x	x	x	GMA_V52-(01011)		
R69	1	0	0	0	0	1	0	1	x	x	x	GMA_V48-(00111)		
R70	1	0	0	0	0	1	1	0	x	x	x	x	GAM_V43-(1000)	
R71	1	0	0	0	0	1	1	1	x	x	x	x	GMA_V38-(0000)	
R72	1	0	0	0	1	0	0	0	x	x	x	x	GMA_V25-(1010)	
R73	1	0	0	0	1	0	0	1	x	x	x	x	GMA_V20-(1111)	
R74	1	0	0	0	1	0	1	0	x	x	x	GAM_V15-(10100)		
R75	1	0	0	0	1	0	1	1	x	x	x	GMA_V11-(01010)		
R76	1	0	0	0	1	1	0	0	x	x	x	GMA_V8-(01100)		
R77	1	0	0	0	1	1	0	1	x	x	GMA_V6-(010100)			
R78	1	0	0	0	1	1	1	0	x	x	GMA_V3-(001100)			
R79	1	0	0	0	1	1	1	1	x	x	GMA_V0-(000001)			

16 adjustable points





A027DN03 V3 Product Spec	Version	0.3
	Page	45/63

R86:

No.	Register address								Register data								MSB		LSB	
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0				
R86	1	0	0	1	0	1	1	0	x	x	x	x	0	1	VGH_SEL(11)					

VGH\_SEL: VGH Voltage selection

VGH_SEL		VGH Voltage (V)
D1	D0	
0	0	12
0	1	13
1	0	14
1	1	15 (Default)

R97:

No.	Register address								Register data								MSB		LSB	
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0				
R97	1	0	1	0	0	0	0	1	x	x	x	x	x		x	GAMMA2.2(0)				

GAMMA2.2 setting : Select auto or manual gamma setting

GAMMA setting	Description
1	Manual set gamma by R48~ R79.
0	Auto set to Default Gamma (Close to 2.2).

### C. Optical specification (Note 1, Note 2, Note 3 )

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	$\theta=0^\circ$	--	10	40	ms	Note 4
Fall	Tf		--	25	50	ms	
Contrast ratio	CR	At optimized viewing angle	200	300	--		Note 5,6
Viewing Angle							
Top	$\Phi_T$	$CR \geq 10$	40	50	--	deg.	Note 7
Bottom	$\Phi_B$		50	60	--		
Left	$\Phi_L$		50	60	--		
Right	$\Phi_R$		50	60	--		
Brightness	$Y_L$	$\theta=0^\circ$	200	250	--	cd/m <sup>2</sup>	Note 8
Chromaticity	White	X	$\theta=0^\circ$	0.26	0.31	0.36	
		Y	$\theta=0^\circ$	0.29	0.34	0.39	
	Red	X	$\theta=0^\circ$	0.55	0.60	0.65	
		Y	$\theta=0^\circ$	0.30	0.35	0.40	
	Green	X	$\theta=0^\circ$	0.29	0.34	0.39	
		Y	$\theta=0^\circ$	0.51	0.56	0.61	
	Blue	X	$\theta=0^\circ$	0.11	0.16	0.21	
		Y	$\theta=0^\circ$	0.10	0.15	0.20	
Uniformity	$\Delta Y_L$	%	70	75	--	%	Note 10

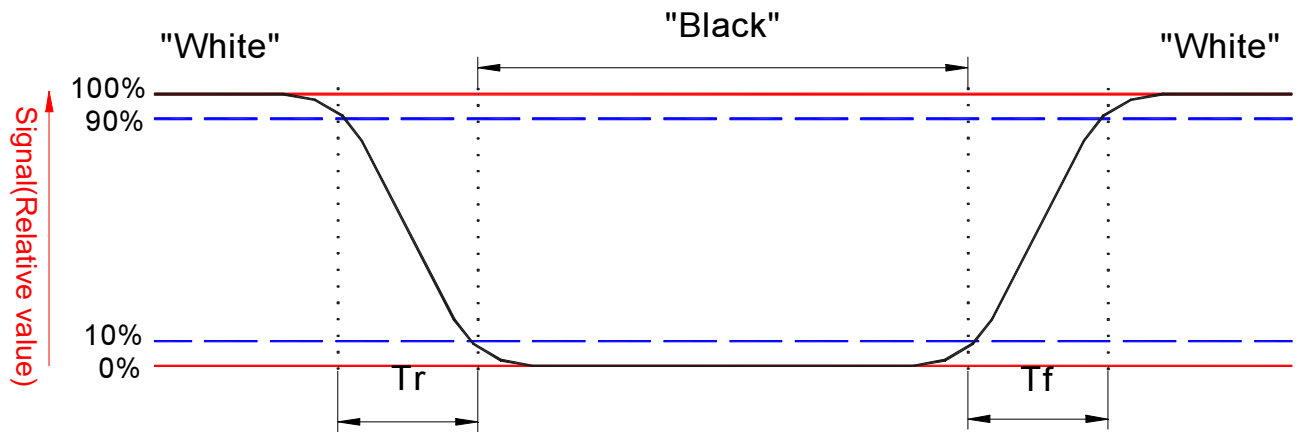
Note 1. Ambient temperature =25°C.

Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White  $V_i = V_{i50} \mp 1.5V$

Black  $V_i = V_{i50} \pm 2.0V$

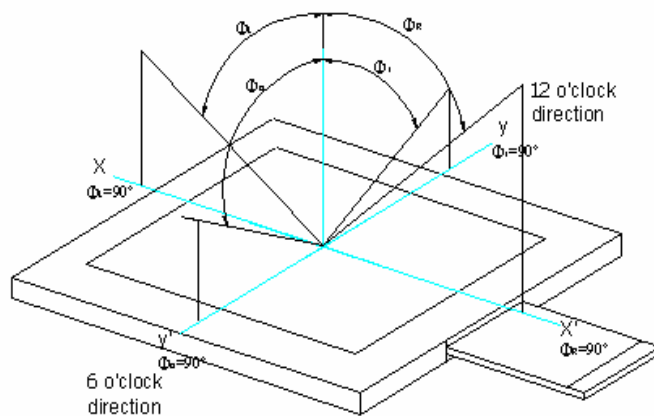
" $\pm$ " Means that the analog input signal swings in phase with COM signal.

" $\mp$ " Means that the analog input signal swings out of phase with COM signal.

$V_{i50}$  : The analog input voltage when transmission is 50%

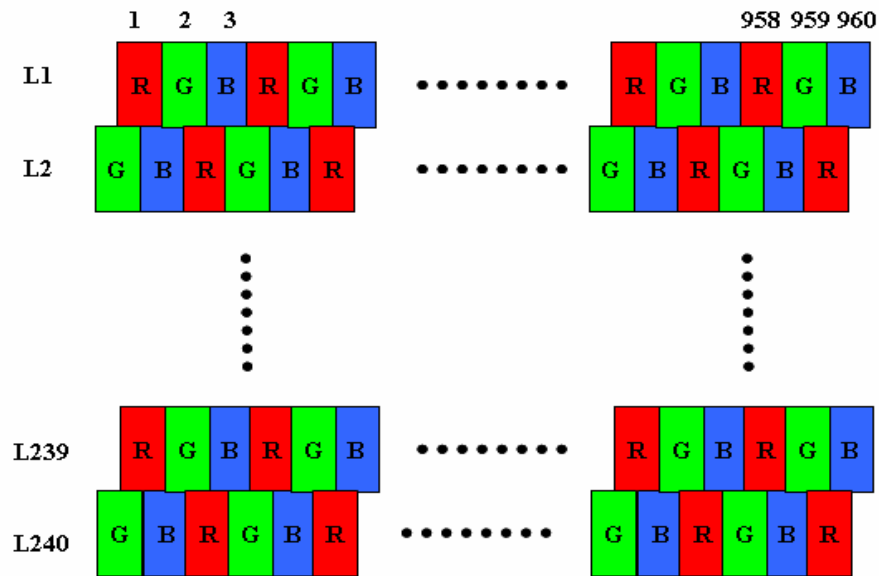
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle,  $\Phi$ , Refer to figure as below.

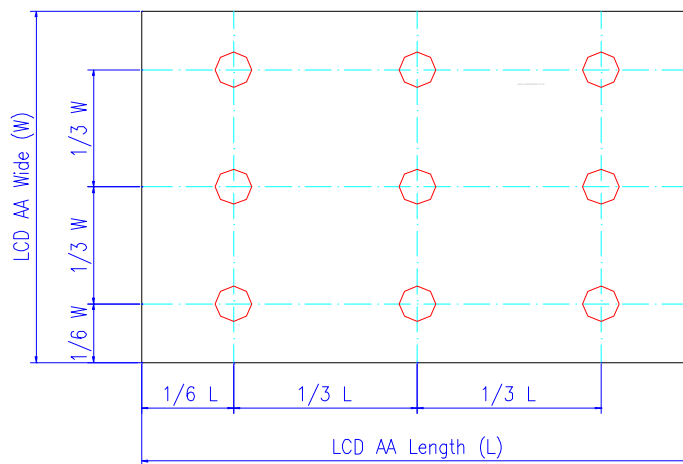


Note 8. Measured at the center area of the panel in gray level 255.

### Note 9. Color Filter Arrangement



### Note 10 Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

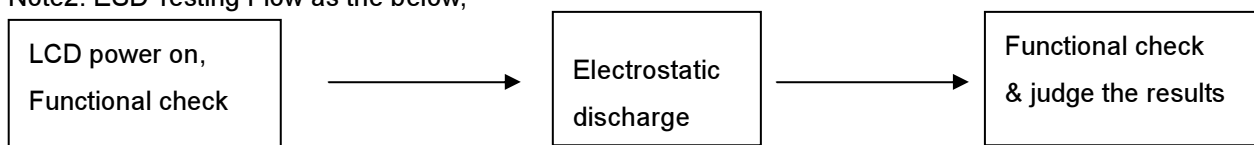


## D. Reliability test items

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃ . 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note.2, 3
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: 0.015G <sup>2</sup> /Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note1: Ta: Ambient temperature.

Note2: ESD Testing Flow as the below,

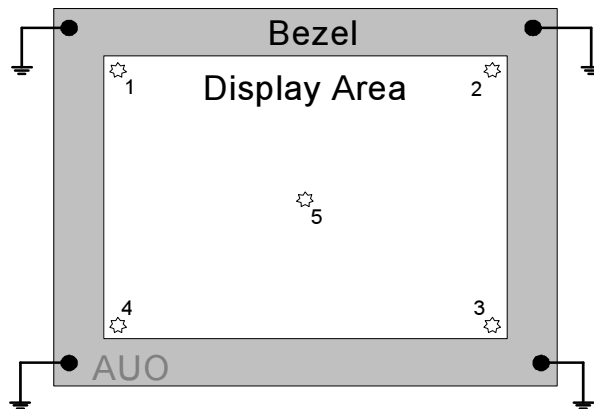


Note 3. ESD testing method.



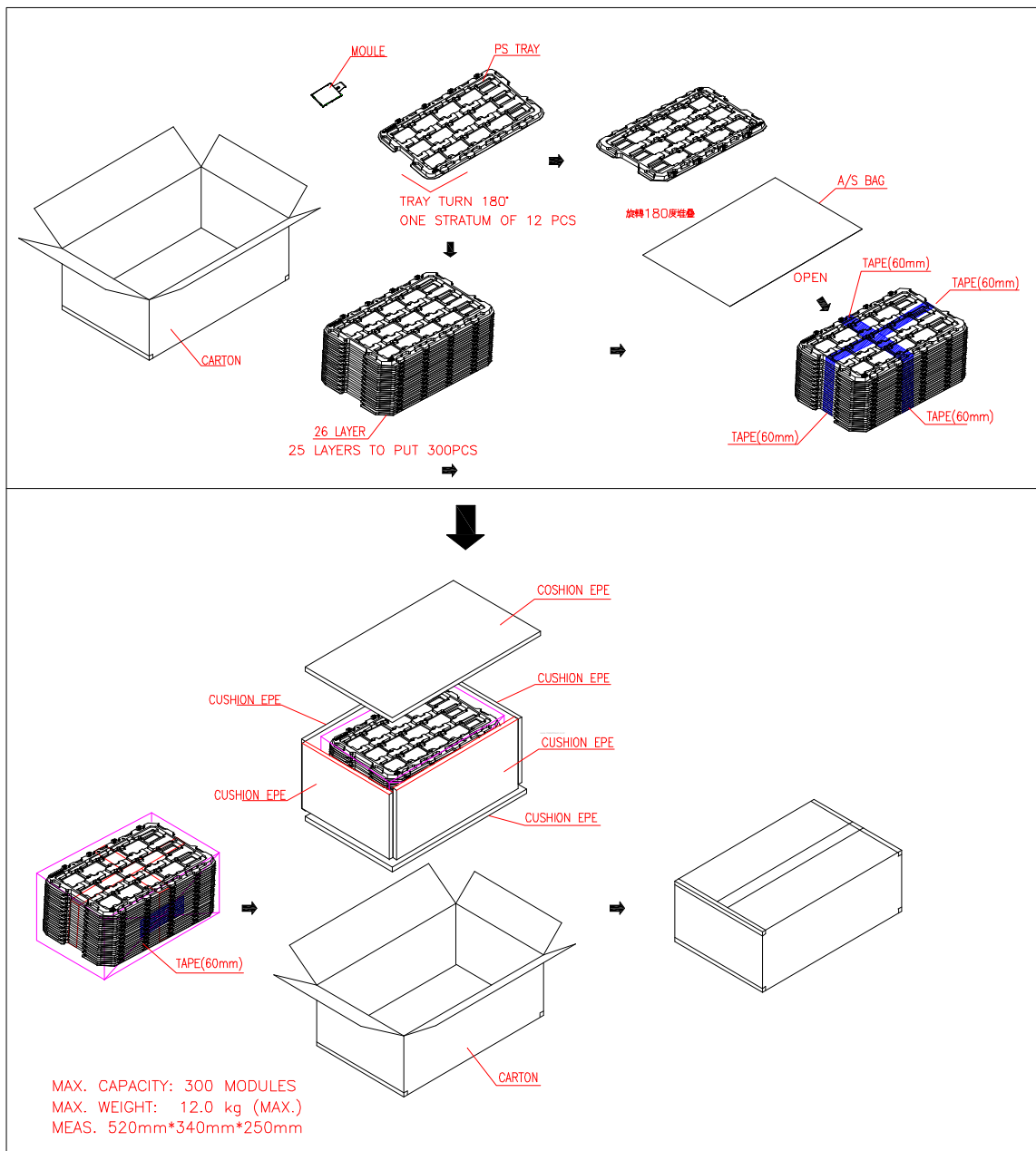
A027DN03 V3 Product Spec	Version	0.3
	Page	50/63

1. Ambient: 24~26℃, 56~65%RH
2. Instruments: Noiseken ESS-2000,
3. Operation System: “CX40FL-B” and adapter “A027DN01 V4T2”
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
  - a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
  - b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

## E. Packing form

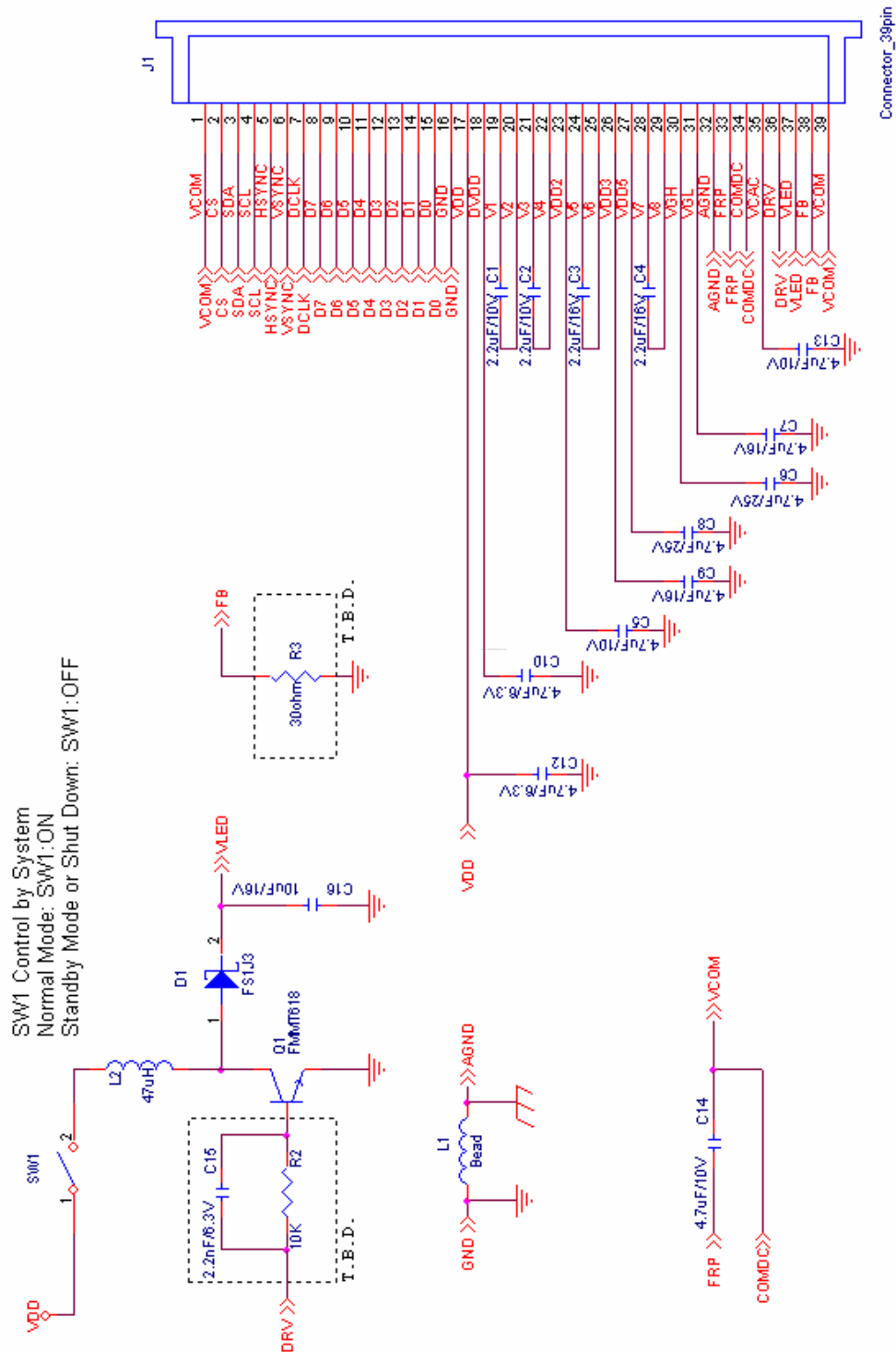


ALL RIGHTS STRICTLY RESERVED. ANY PORTION OF THIS PRPER SHALL NOT BE REPRODUCED, COPIED, OR TRANSFORMED TO ANY OTHER FORMS WITHOUT PERMISSION FROM AU OPTRONICS CORP.

## G. Application note

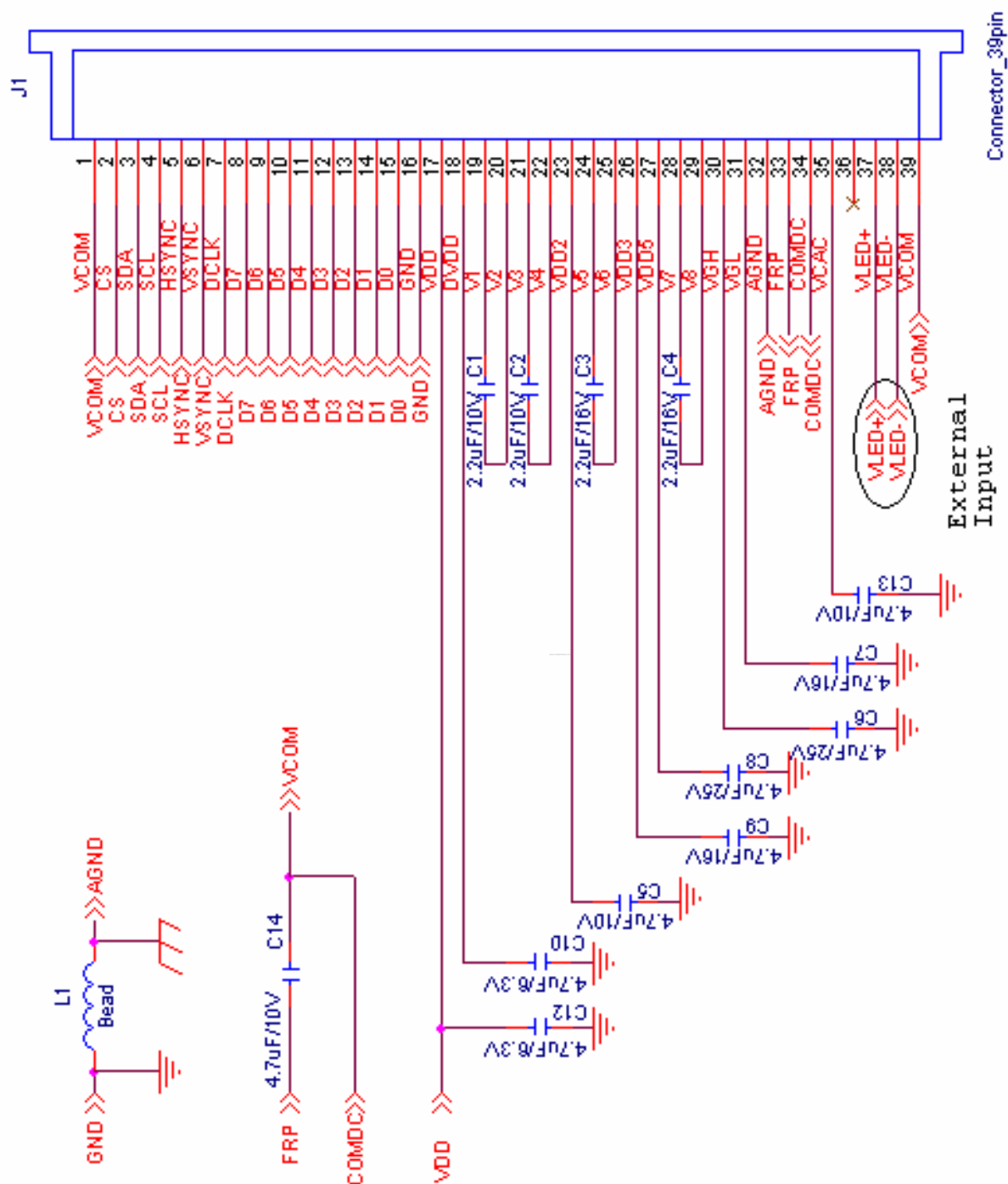
### 1. Application circuit

#### 1.1 Internal LED drive backlight



Note1: Use internal LED driver must set R5[1](SHDB1)= "1".

## 1.2 External LED drive backlight



Note2: Use external LED driver must set R5[1](SHDB1)= "0".

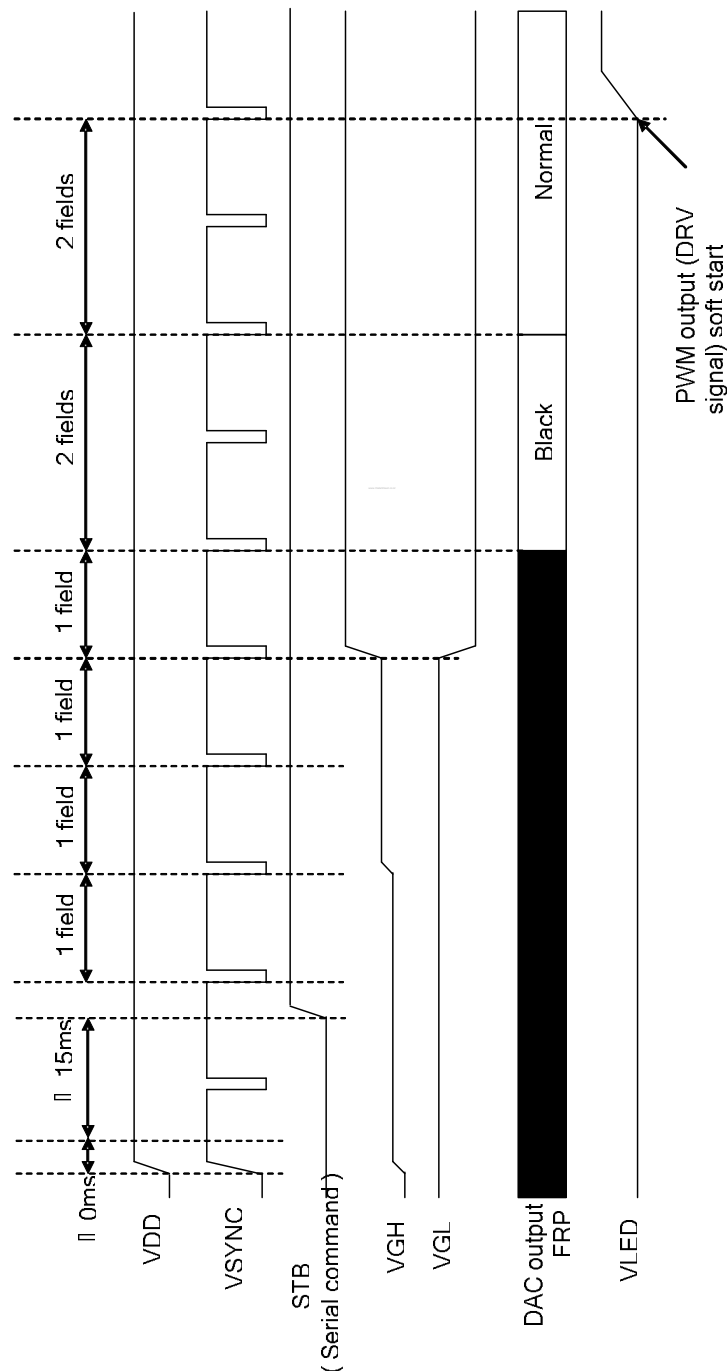
## 2. Power on/off sequence

The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

### 2.1 Power on (Standby Disabling)

After VDD power on reset, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. The LCD driver is in default standby mode after VDD power-on, and setting register R5: STB to '1' to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The LCD positive and negative power supplies VGH/VGL are pumped first, and followed by the LED power VLED. Please refer to Fig.10 for the detail timing of power on sequence.

Fig.10 Power on sequence



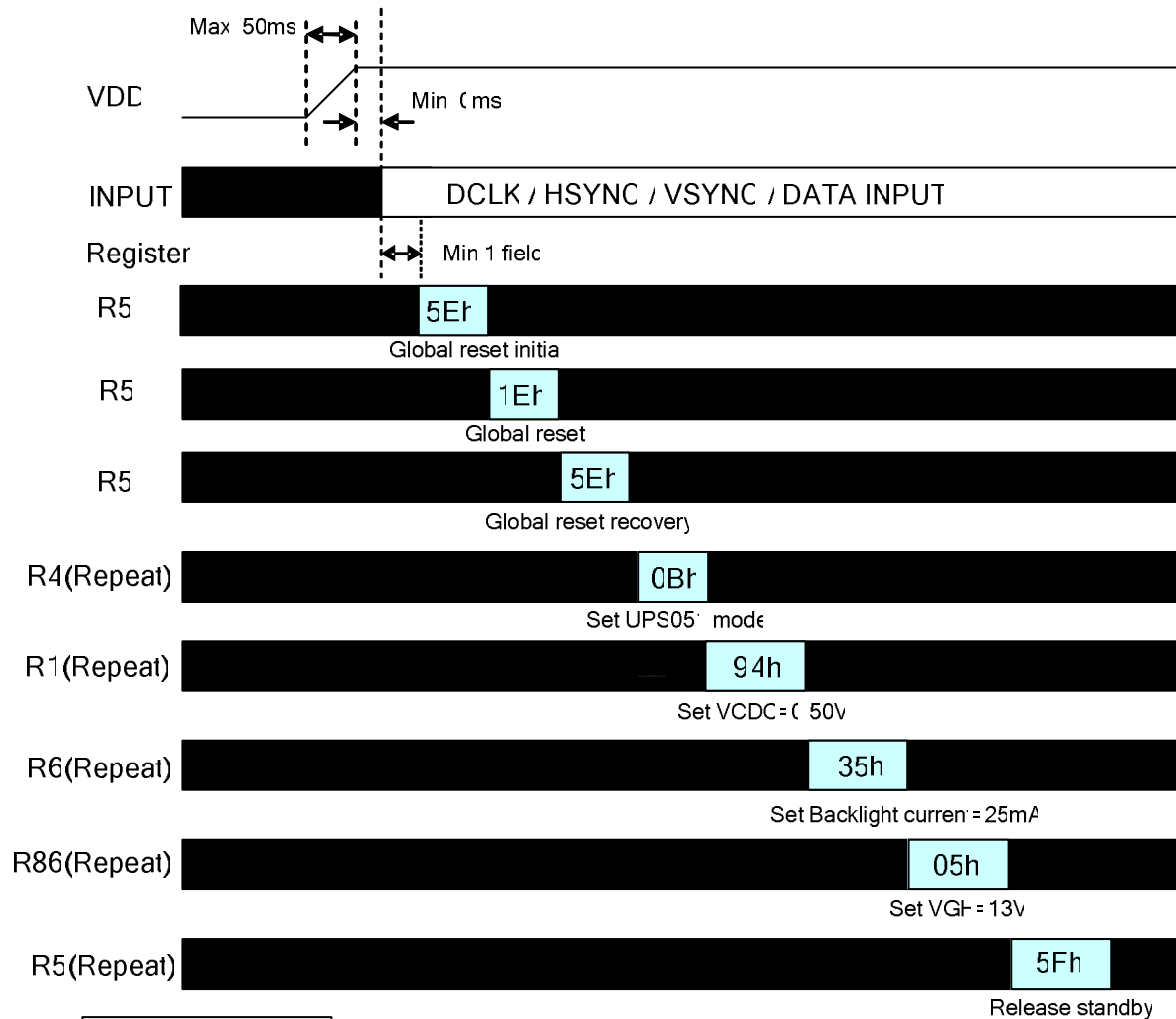
ALL RIGHTS STRICTLY RESERVED. ANY PORTION OF THIS PRPER SHALL NOT BE REPRODUCED, COPIED, OR TRANSFORMED TO ANY OTHER FORMS WITHOUT PERMISSION FROM AU OPTRONICS CORP.



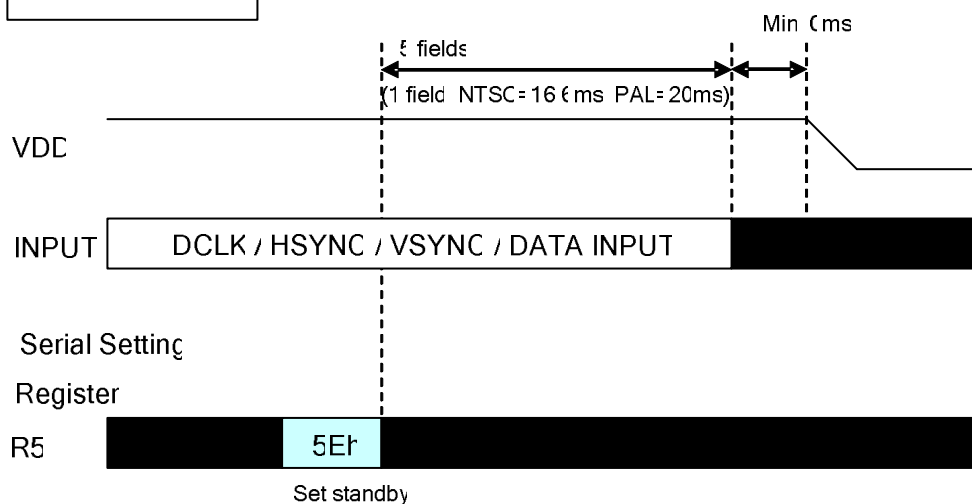
### 3. Recommended power on/off serial command settings

#### 3.1 UPS051

##### POWER ON



##### POWER OFF

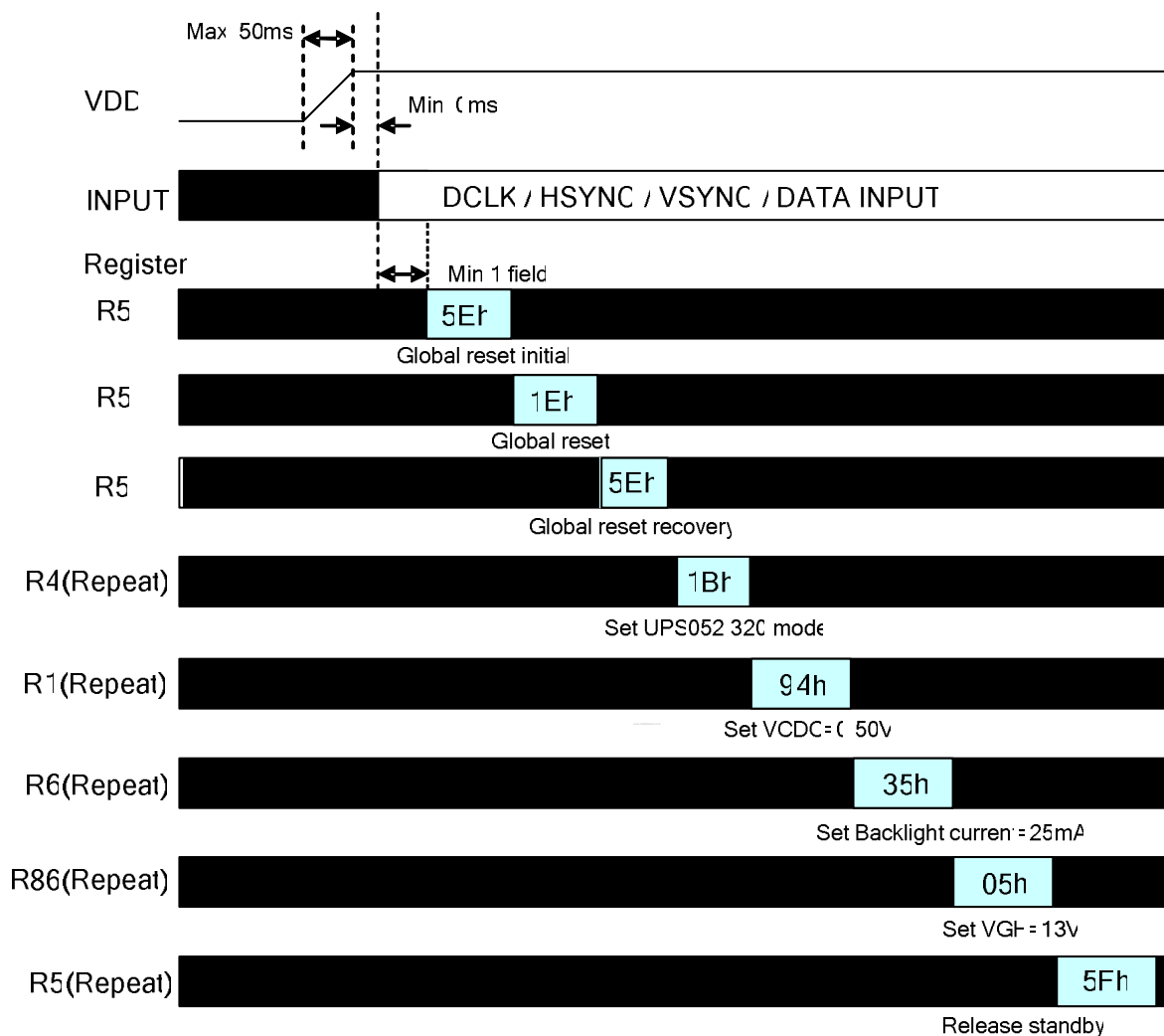




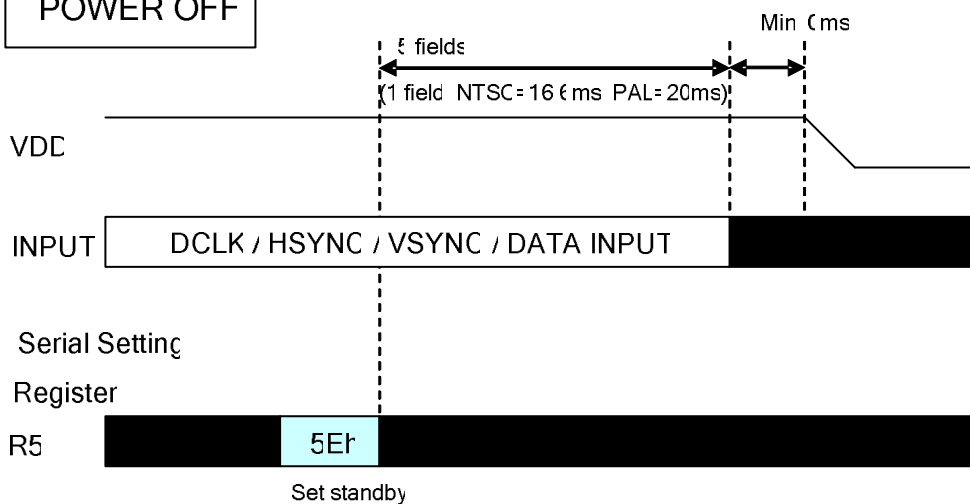
A027DN03 V3 Application Note	Version	0.2
	Page	58/63

### 3.2 UPS052 320 mode

#### POWER ON



#### POWER OFF

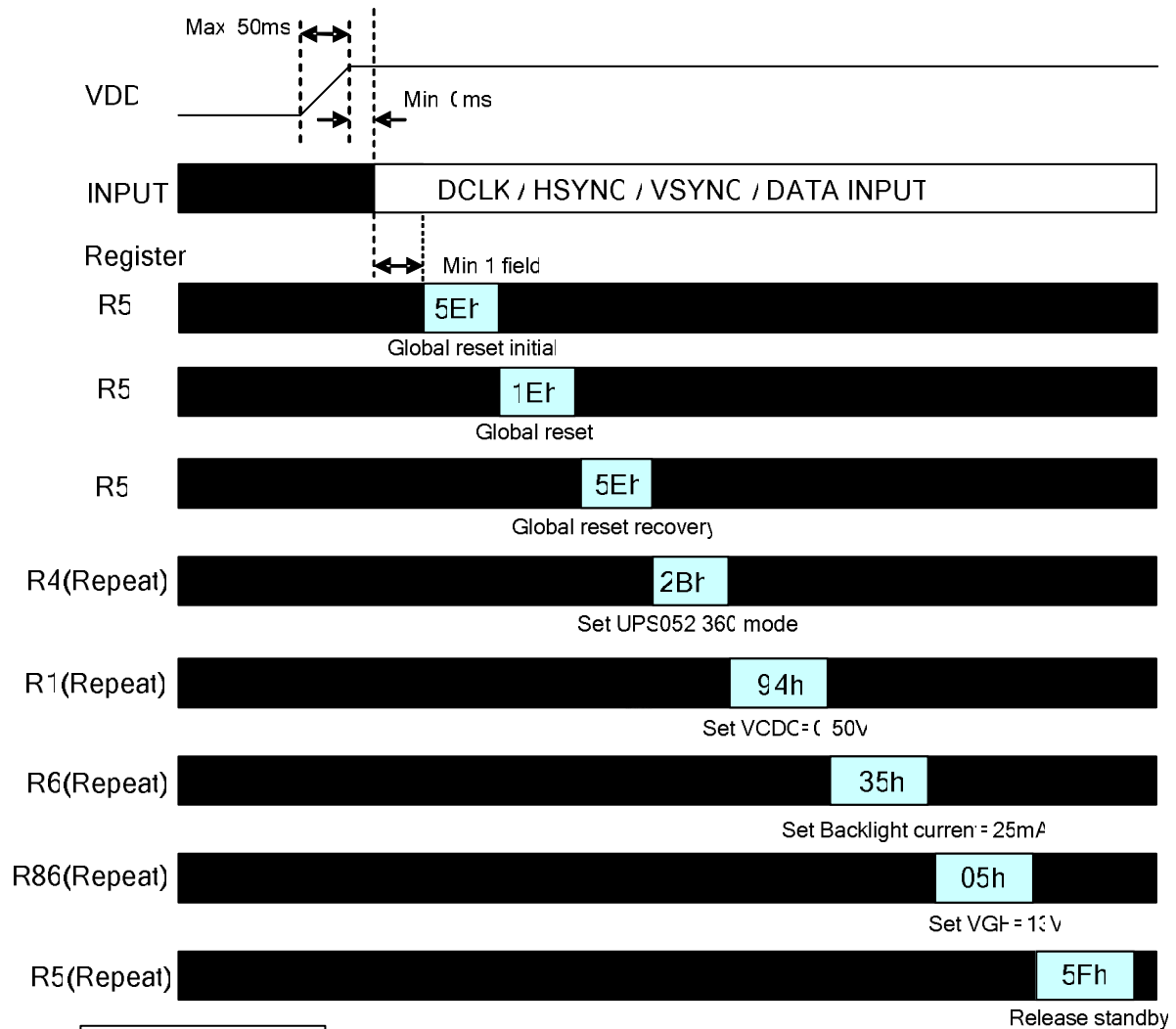




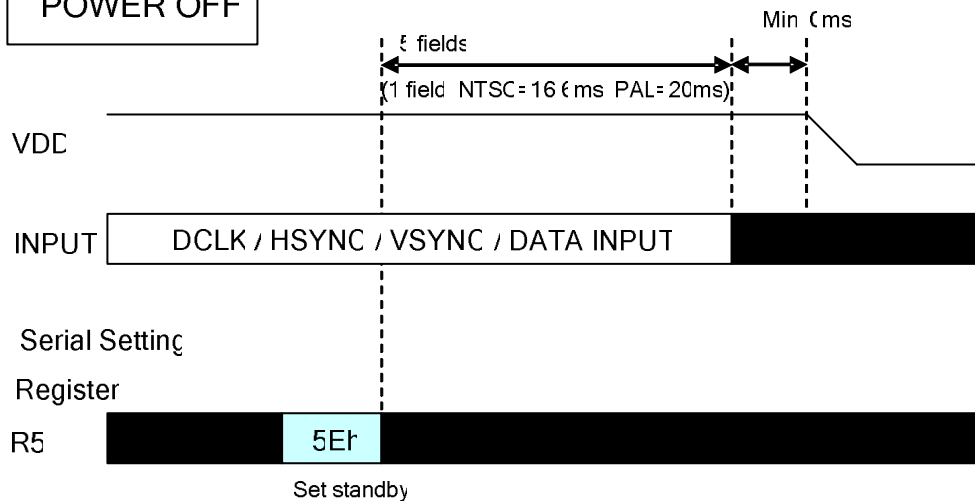
A027DN03 V3 Application Note	Version	0.2
	Page	59/63

### 3.3 UPS052 360 mode

#### POWER ON

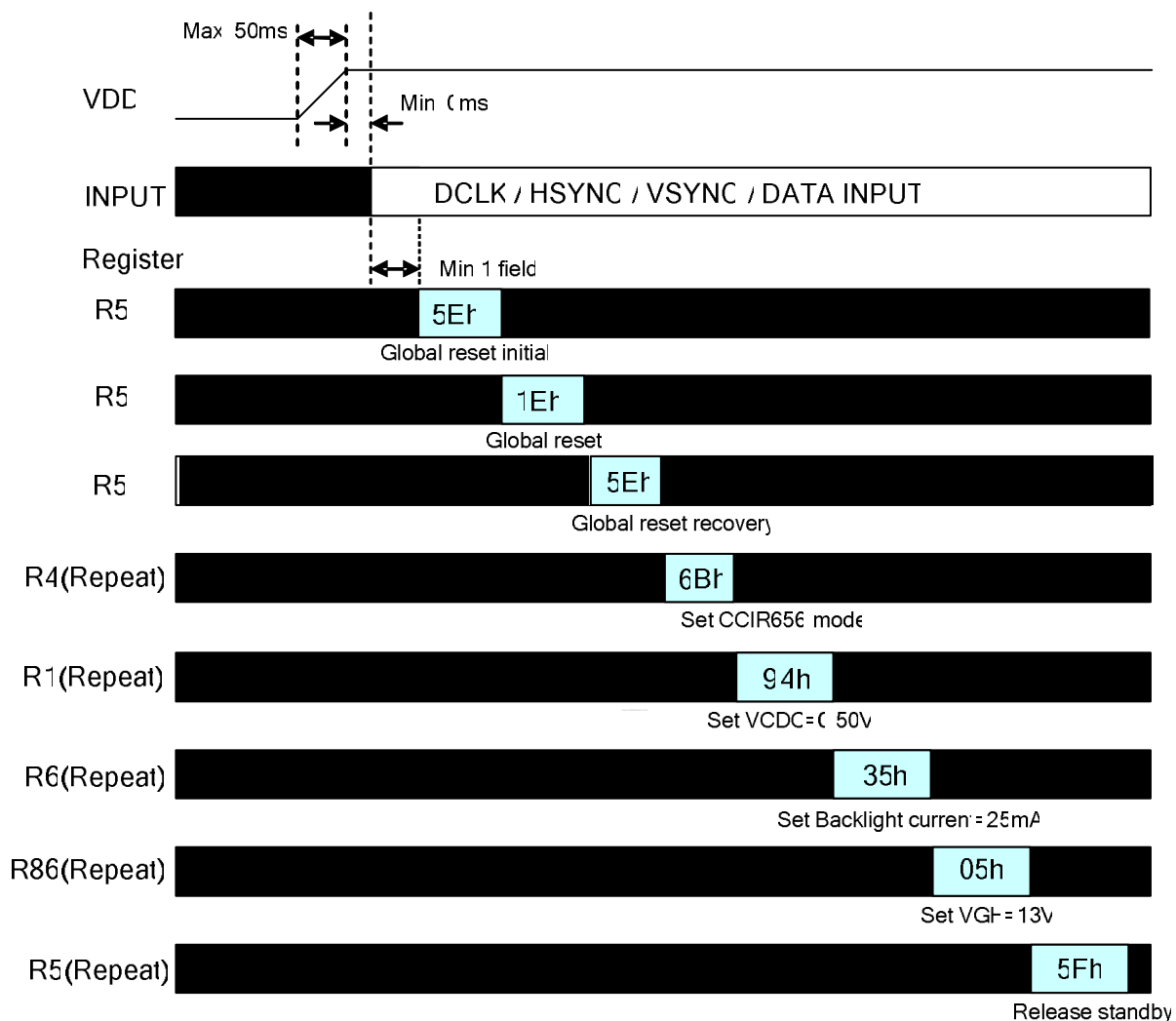


#### POWER OFF

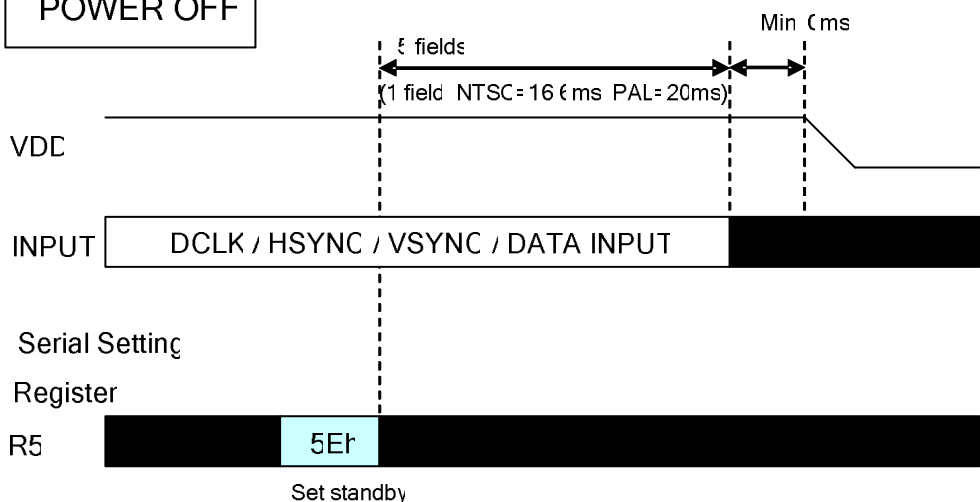


### 3.4 CCIR656

#### POWER ON



#### POWER OFF

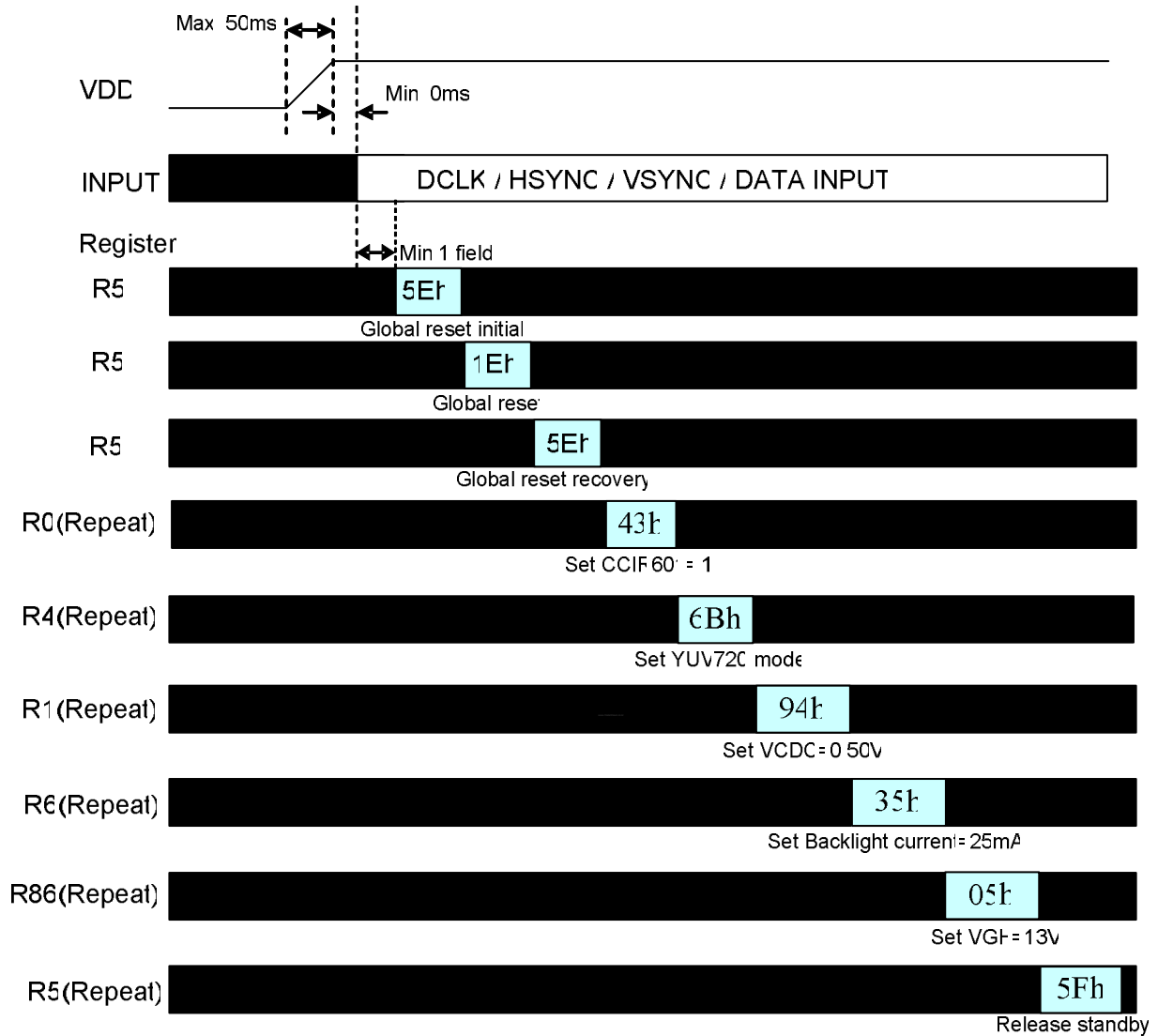




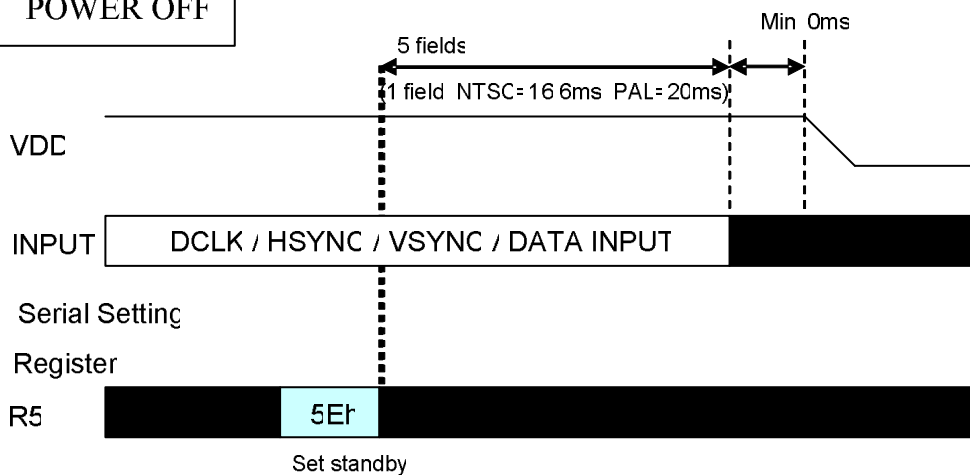
A027DN03 V3 Application Note	Version	0.2
	Page	61/63

### 3.5 YUV 720

#### POWER ON



#### POWER OFF

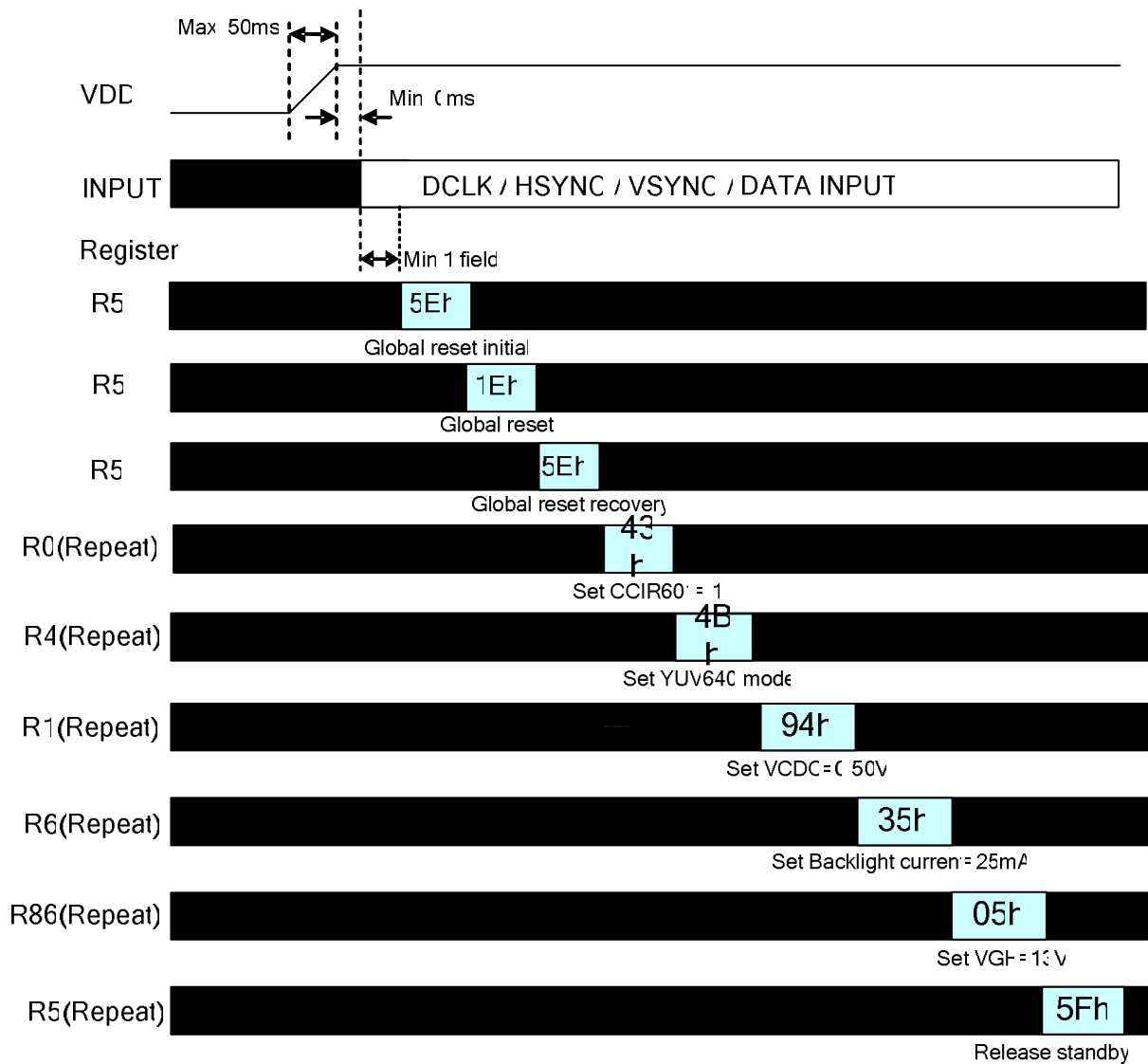




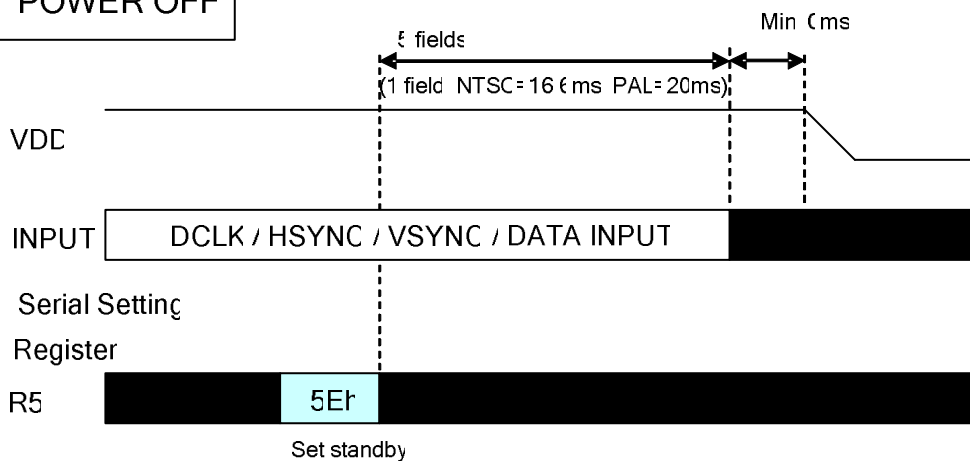
A027DN03 V3 Application Note	Version	0.2
	Page	62/63

### 3.6 YUV 640

#### POWER ON



#### POWER OFF



#### 4. Power generation circuit

The block diagram of built-in power generation circuit for TFT-LCD supply power is shown as below:

