RAA207700GBM/7701GBM/7702GBM

Synchronous Buck Regulator with Internal Power MOSFETs

R07DS0891EJ0001
Rev.0.01
Nov 29, 2012

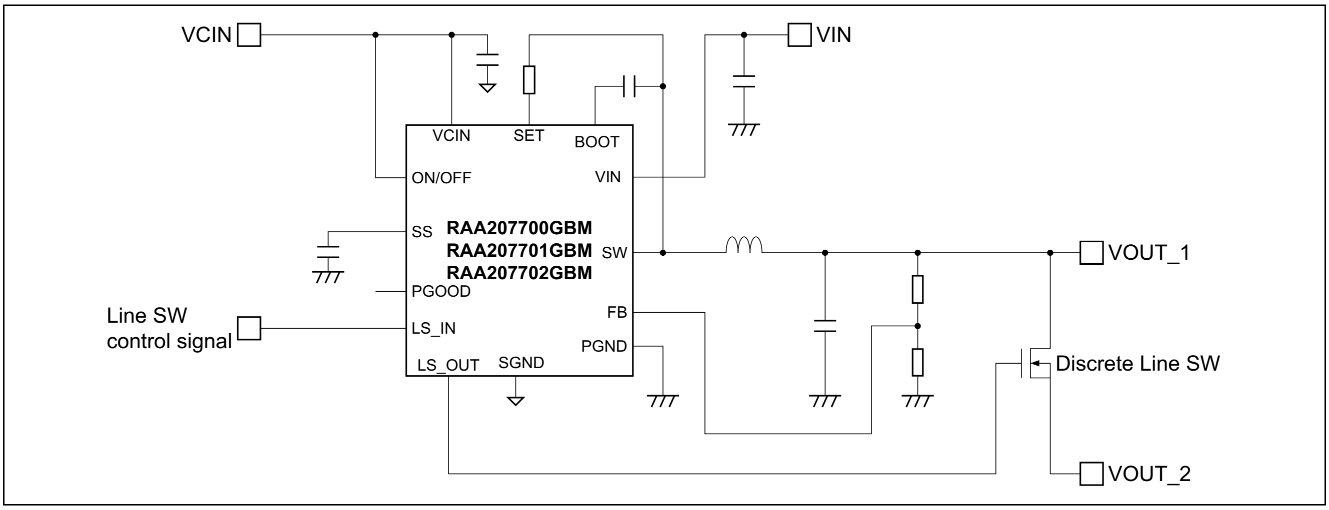
Description

The RAA207700GBM is monolithic synchronous buck regulator with power MOSFETs in extremely small package. The RAA207700GBM delivers high output current by small Rds(on) Power MOSFETs. Constant on time control architecture provides fast transient response, and minimize external components. The RAA207700GBM operates skip mode at light load, it provides high efficiency in all load condition. Three current ability products can be selected.

Features

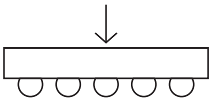
- Wide input voltage range: 3 V to 16 V
- Constant-On-Time control
- Built-in power MOSFETs suitable for PC, Server application
- Very low stand-by current: 0.1 μA (typ.)
- Very low quiescent current :320 μA (typ. at no load)
- Switching frequency: Adjustable up to 2 MHz
- High average output current, up to 15 A (7700GBM), 10 A (7701GBM), 5 A (7702GBM)
- Controllable driver: Remote on/off
- Power Good function
- Over current protection/Over voltage protection/Thermal shutdown function
- Built-in bootstrapping diode
- Soft Start period adjustable
- Enhanced light load mode function for higher efficiency
- High drivability built-in line switch driver for low-loss line switch driving
- Extremely small chip size package with solder bump
- Pb-Free/Halogen-Free

Application Circuit



Pin Arrangement

Top View



<RAA207700GBM>

	1	2	3	4	5
A	VCIN	SGND	FB	LS_IN	LS_OUT
B	BOOT	SET	PGOOD	SS	ON/OFF
C	SW	VIN	VIN	VIN	VIN
D	SW	SW	SW	SW	VIN
E	SW	PGND	PGND	PGND	PGND
F	SW	SW	SW	PGND	PGND
G	SW	PGND	PGND	PGND	PGND

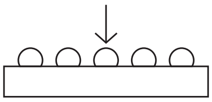
<RAA207701GBM>

	1	2	3	4	5
A	VCIN	SGND	FB	LS_IN	LS_OUT
B	BOOT	SET	PGOOD	SS	ON/OFF
C	SW	VIN	VIN	VIN	VIN
D	SW	SW	SW	SW	VIN
E	SW	PGND	PGND	PGND	PGND
F	SW	SW	SW	PGND	PGND

<RAA207702GBM>

	1	2	3	4	5
A	VCIN	SGND	FB	LS_IN	LS_OUT
B	BOOT	SET	PGOOD	SS	ON/OFF
C	SW	SW	VIN	VIN	VIN
D	SW	SW	PGND	PGND	PGND

Bottom View



<RAA207700GBM>

	5	4	3	2	1
A	LS_OUT	LS_IN	FB	SGND	VCIN
B	ON/OFF	SS	PGOOD	SET	BOOT
C	VIN	VIN	VIN	VIN	SW
D	VIN	SW	SW	SW	SW
E	PGND	PGND	PGND	PGND	SW
F	PGND	PGND	SW	SW	SW
G	PGND	PGND	PGND	PGND	SW

CSP 35-pin package
2.7 mm × 3.9 mm

<RAA207701GBM>

	5	4	3	2	1
A	LS_OUT	LS_IN	FB	SGND	VCIN
B	ON/OFF	SS	PGOOD	SET	BOOT
C	VIN	VIN	VIN	VIN	SW
D	VIN	SW	SW	SW	SW
E	PGND	PGND	PGND	PGND	SW
F	PGND	PGND	SW	SW	SW

CSP 30-pin package
2.7 mm × 3.4 mm

<RAA207702GBM>

	5	4	3	2	1
A	LS_OUT	LS_IN	FB	SGND	VCIN
B	ON/OFF	SS	PGOOD	SET	BOOT
C	VIN	VIN	VIN	SW	SW
D	PGND	PGND	PGND	SW	SW

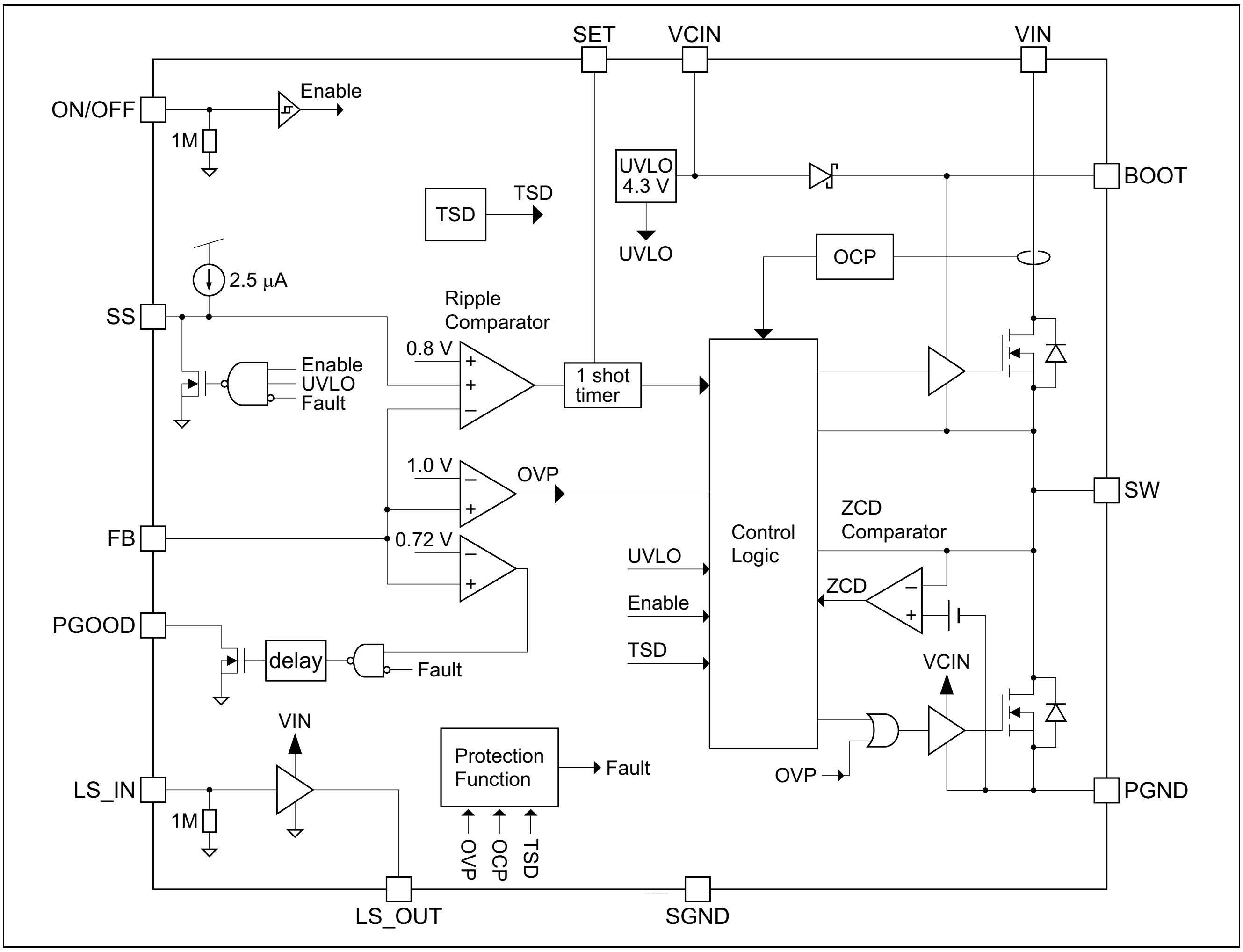
CSP 20-pin package
2.7 mm × 2.4 mm

Pin Description

Pin Name	Pin No.	Description	Remarks
VCIN	1A	Controller input voltage (+5 V input)	Controller supply input
SGND	2A	Controller analog GND	Should be connected to PGND on PCB pattern
FB	3A	Feedback voltage input pin	
LS_IN	4A	Line SW driver control pin	
LS_OUT	5A	Line SW driver output pin	
BOOT	1B	Bootstrap voltage pin	To be supplied +5 V through integrated SBD
SET	2B	Constant on time program pin	Tie resistor between SW and SET
PGOOD	3B	Power good indicator pin	Pull low when No Good (open drain output)
SS	4B	Soft start period program pin	Tie capacitor between SS and SGND
ON/OFF	5B	Operation enable pin	Operation stop when L signal asserted
VIN	—	Input voltage	
SW	—	Switching node	
PGND	—	Power ground	Should be connected to SGND on PCB pattern

Note: Pin assign of 1A-5A & 1B-5B is common through RAA207700GBM, RAA207701GBM and RAA207702GBM.

Block Diagram



1. Truth table for the ON/OFF pin

ON/OFF Input	Driver Chip Status
"L"	Shutdown (operation STOP)
"Open"	Shutdown (operation STOP)
"H"	Enable (Normal operation)

2. Truth table for Line Switch driver

LS_IN Input	LS_OUT Status
"L"	GND
"Open"	GND
"H"	VIN

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Input voltage	VIN	–0.3 to +20	V	1
Switch node voltage	SW	20(DC), 23(<10 ns)	V	1
BOOT voltage	VBOOT	25(DC), 28(<10 ns)	V	1, 2
Controller voltage	VCIN	–0.3 to +6	V	1
Input pin voltage (FB, LS_IN)	V_{INPUT}	–0.3 to VCIN +0.3	V	1, 3
ON/OFF voltage	$V_{ON/OFF}$	–0.3 to VIN	V	1
SET voltage	V_{SET}	–0.3 to VIN	V	1
PGOOD voltage	V_{PGOOD}	–0.3 to VIN	V	1
PGOOD sink current	I_{PGOOD}	+2	mA	4
Operating junction temperature	Tj-opr	–40 to +125	°C	
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Rated voltages are relative to voltages on the SGND and PGND pins.
2. BOOT – VCIN < 20 V
3. VCIN + 0.3 V < 6 V
4. For rated current, (+) indicates inflow to the chip.

Recommended Operating Condition

Item	Symbol	Ratings	Unit	Remarks
Input voltage	VIN	3 to 16	V	
Controller voltage	VCIN	4.5 to 5.5	V	
Continuous output current	IOUT	0 to 15 0 to 10 0 to 5	A	15 A: RAA207700GBM 10 A: RAA207701GBM 5 A: RAA207702GBM

Electrical Characteristics

(Ta = 25°C, VCIN = 5 V, VIN = 12 V, SW = 0 V, unless otherwise specified)

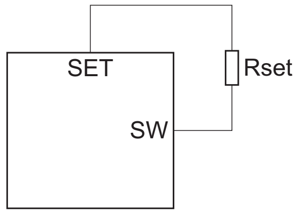
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	VCIN start threshold	VH	—	4.3	4.5	V	
	VCIN shutdown threshold in CCM	VL	3.6	3.8	—	V	
	VCIN shutdown threshold in ELL mode	V_{LCCM}	—	3.0	3.6	V	In ELL mode (DCM, f_{SW} < 100 kHz)
	VCIN operating current (RAA207700GBM)	I_{CIN}	—	40	—	mA	f_{SW} = 1 MHz, Ton = 200 ns
	VCIN operating current (RAA207701GBM)	I_{CIN}	—	35	—	mA	
	VCIN operating current (RAA207702GBM)	I_{CIN}	—	20	—	mA	
	VCIN quiescent current	Iq	—	320	400	μA	Output = no load, ELL mode
	VCIN disable current	$I_{CIN-DISBL}$	—	0.1	5	μA	ON/OFF = 0 V, LS_IN = 0 V
	VIN disable current	$I_{IN-DISBL}$	—	0.1	5	μA	ON/OFF = 0 V, LS_IN = 0 V
Remote on/off	Disable level	V_{DISBL}	—	—	0.6	V	3.3 / 5.0 V interface
	Enable level	V_{ENBL}	2.0	—	—	V	3.3 / 5.0 V interface
	Pull-down resistance	R_{DISBL}	0.7	1	1.3	MΩ	ON/OFF = 1 V
Line_SW input	Line SW off level	V_{LSIN_OFF}	—	—	0.6	V	3.3 / 5.0 V interface
	Line SW on level	V_{LSIN_ON}	2.0	—	—	V	3.3 / 5.0 V interface
	Pull-down resistance	R_{LS_IN}	0.7	1	1.3	MΩ	LS_IN = 1 V
Line_SW output	Line SW on output voltage	V_{LSW_ON}	VIN–0.5	VIN	—	V	LS_IN = 5 V
	Line SW off output voltage	V_{LSW_OFF}	—	—	0.1	V	LS_IN = 0 V
	Line SW on source current	I_{LSW_SOURCE}	—	25	—	mA	VIN = 12 V, LS_IN = 5 V
	Line SW off sink current	I_{LSW_SINK}	—	25	—	mA	VIN = 12 V, LS_IN = 0 V
	Line SW on propagation delay	T_{PLSWON}	—	300	—	ns	LSIN to LSOUT rising
	Line SW off propagation delay	$T_{PLSWOFF}$	—	300	—	ns	LSIN to LSOUT falling
	Line SW drive current of VIN	I_{IN-LS}	—	8	20	μA	LS_IN = 5 V
FB	Comparator threshold voltage	V_{FB_COMP}	792	800	808	mV	
	FB input current	I_{FB_IN}	–0.1	0	+0.1	μA	FB = 1 V
Power good indicator	Rising threshold on FB	V_{PG_rise}	0.67	0.72	0.77	V	
	Power good hysteresis	dV_{PG}	—	50	—	mV	
	Power good resistance	R_{PG}	0.25	0.5	1	kΩ	FB = 0 V
Soft start	Soft start bias current	I_{SS}	1.8	2.5	3.2	μA	
Over voltage protection	OVP trip voltage on FB	V_{OVP}	0.95	1.00	1.05	V	
Over current protection	OCP trip current (RAA207700GBM)	I_{OCP}	16.0	20.0	24.0	A	Fixed internally *1
	OCP trip current (RAA207701GBM)	I_{OCP}	12.0	15.0	18.0	A	Fixed internally *1
	OCP trip current (RAA207702GBM)	I_{OCP}	6.4	8.0	9.6	A	Fixed internally *1
Over temperature protection	TSD trip temperature	T_{TSD}	130	150	—	°C	*1
	Temperature hysteresis	T_{hys}	—	30	—	°C	*1

Note: *1 Not directly tested. Assured by related characteristics test.

Description of Operation

The RAA207700GBM operates as voltage-ripple based constant on time control architecture. Converter output is controlled by output voltage ripple which is determined by inductor ripple current and ESR & ESL of output capacitor. Each switching cycle starts High-side MOSFET turn on which time is decided by 1 shot timer. After High-side MOSFET turns off, Low side turns on, and it keeps until FB voltage becomes lower than reference voltage. In light load condition, Low-side MOSFET on time is decided by inductor zero current.

Switching Frequency, Constant on Time Setting



Switching Frequency in CCM mode is determined by following equation.

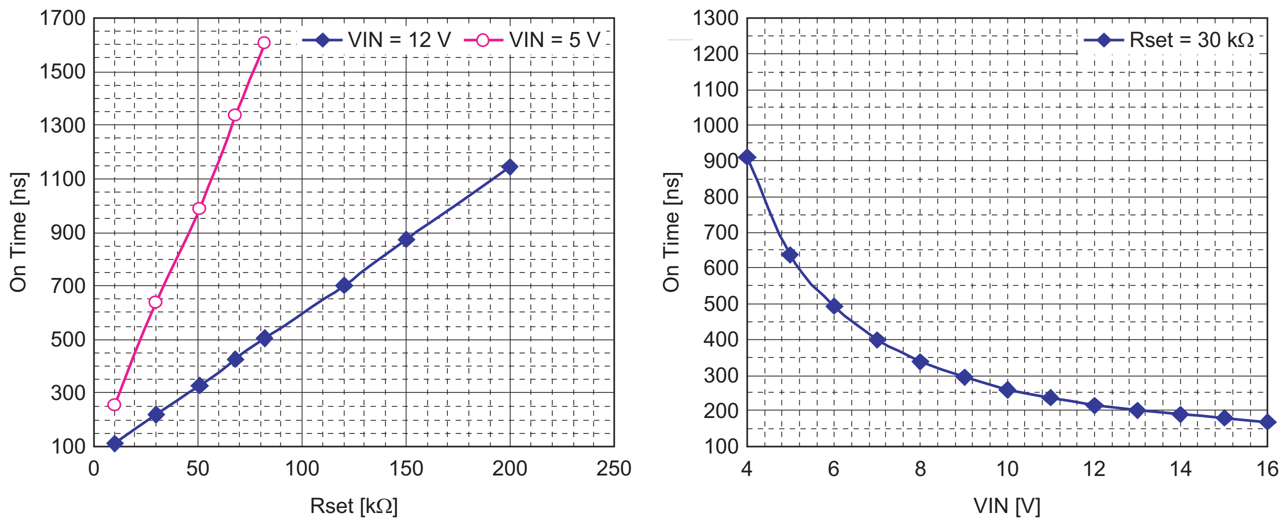
Switching Frequency: (Vout/Vin) • (1/ton) [Hz]

Here, ton is High-side MOS on time, and it is determined by following equation.

On time pulse: (50 pF • 1 V / Vin – 2.0 V) • Rset + 50 ns [s]

From above equation, constant on time is change depend on Vin, so switching frequency is almost constant when VIN change. This architecture is suitable for battery application. From the above equation, Rset is calculated by

Rset: (Vout / (Vin • Fsw) – 50 ns) • (Vin – 2.0 V) / (50 pF • 1 V) [Ω]

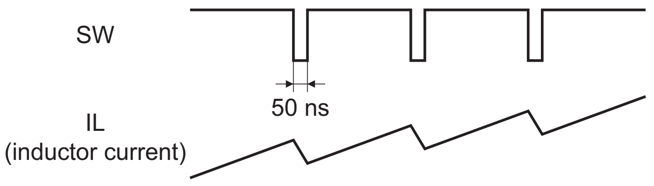


Maximum Duty Cycle Operation

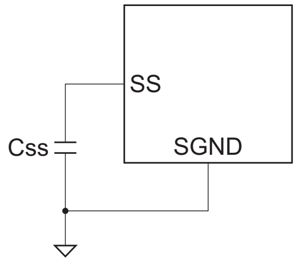
Maximum duty cycle is restricted by following equation.

Max. duty: 1 – (50 ns • Fsw)

Here, Fsw is switching frequency.
If FB voltage does not reach reference voltage after the High-side MOSFET turn on time is expired, Low-side MOSFET turns on 50 ns, and next switching cycle starts. Especially, this condition occurs when output load transient state.



Soft Start



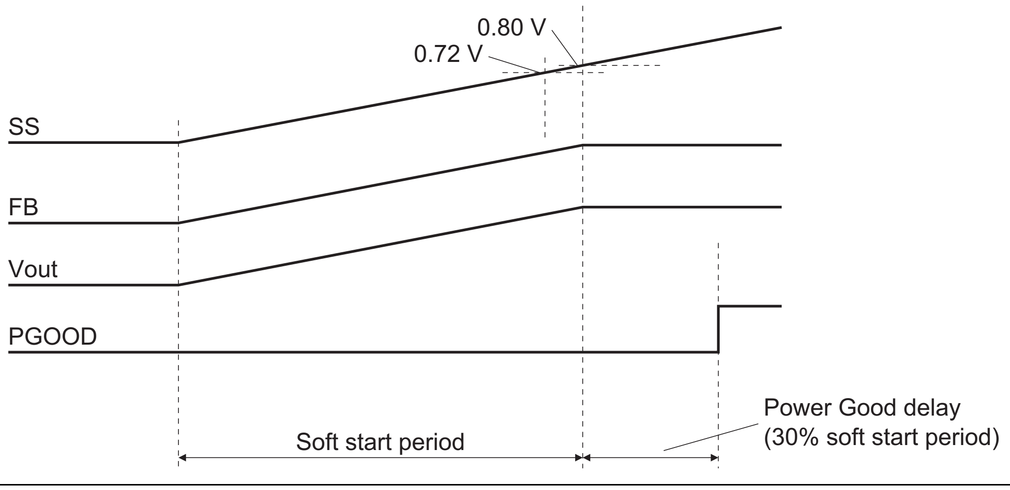
Soft start ramp period is adjustable by external capacitor (Css) selection. When converter start operating, 2 μA current from SS pin charges capacitor between SS and GND. Soft start period is determined by following equation.

Soft Start period: Css • 0.8 V / 2.5 μA [s]

Here, 0.8 V is internal reference voltage Vref. IC operates diode emulation mode at Soft start period, so it can prevent from reverse current when pre-bias condition. Soft start restarts when Enable signal re-entered, and after OCP, OVP, TSD, UVL release condition.

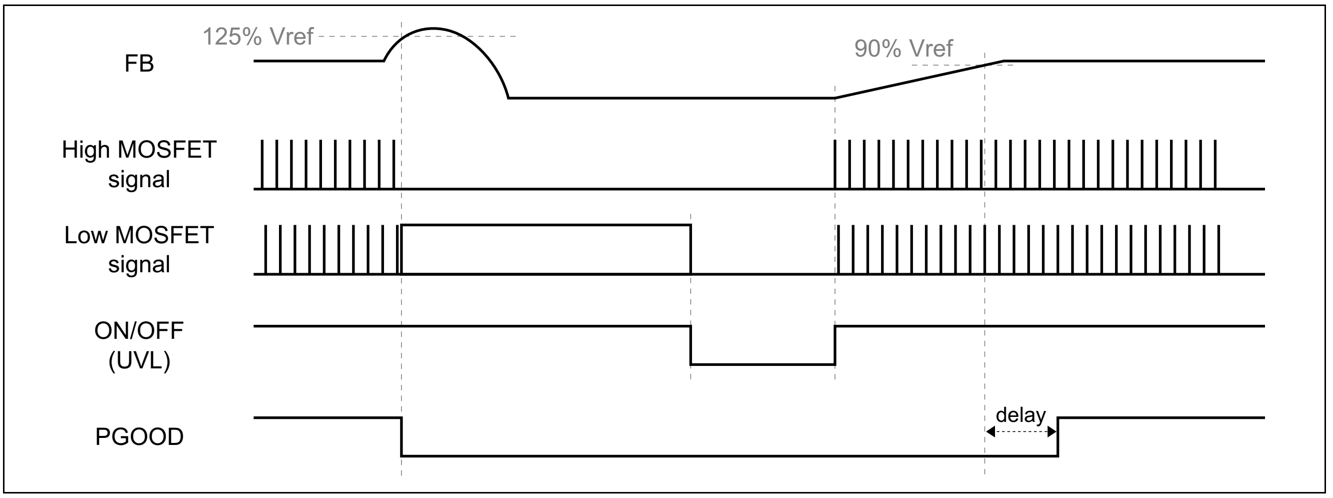
Power Good Indicator

Power good indicator is useful for controlling multi-converter systems for sequential start up and shut down. FB voltage ismonitored continuously by power good comparator. The power good comparator compares FB pin and 90% internal referencevoltage (0.72 V). When FB reaches reference voltage, PGOOD pin becomes high impedance after internal delay (30% of soft start period). Under the fault condition (UVLO, OVP, OCP, TSD), PGOOD pin is pulled low.



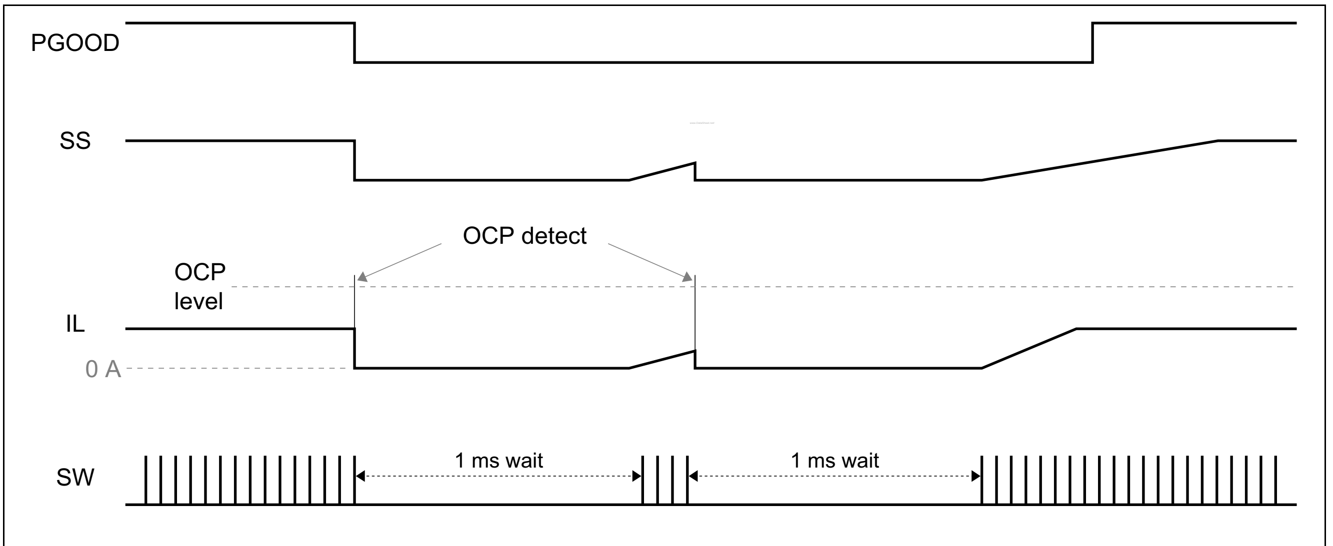
Over Voltage Protection (OVP)

When FB voltage exceeds 125% of reference voltage (1.00 V), switching stops immediately and latched Low-side MOSFET on state in order to pull the output voltage. To leave the OVP condition, VCIN needs to be pulled under the UVLO level, and re-enter the signal.



Over Current Protection (OCP)

OCP detection circuit monitors high-side MOSFET drain-source current. When the current exceeds fixed level eight time, IC starts hiccup operation. In the hiccup operation, switching stops and operate 1 ms timer. After 1 ms timer is expired, IC operates again from soft start state. If IC detect OCP in the soft start circuit, hiccup operation start again.



Note: PGOOD pin is connected VCIN through resistor.

Thermal Shutdown (TSD)

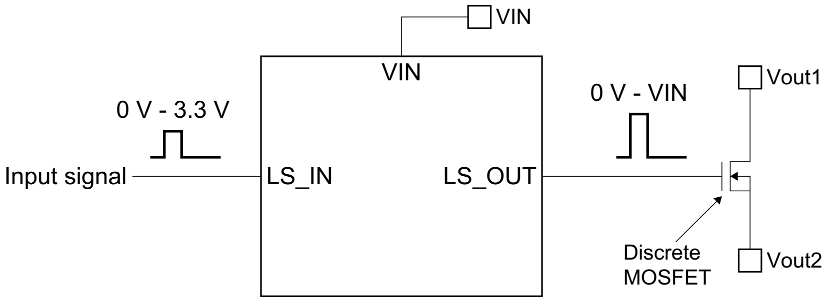
Thermal sensor monitors junction temperature of IC. When junction temperature exceeds 150°C, switching stops. After junction temperature become 125°C, IC restart switching from soft start (Non-latched function).

Enhanced Light Load Function (ELL)

IC operates diode emulation mode in light load condition. To enhance light load efficiency, IC detects light load condition automatically, and operate as Enhanced Light Load mode (ELL). In ELL mode, bias current of IC becomes small, so this function can improve the efficiency.

Line Switch Driver

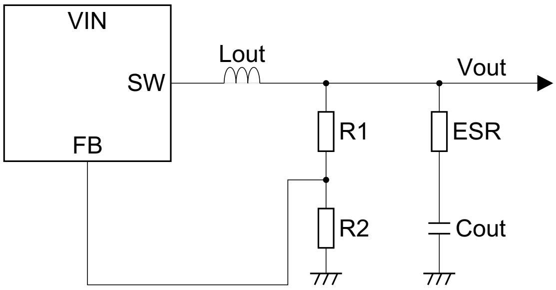
The RAA207700GBM/7701GBM/7702GBM incorporates high drivability built in line switch driver. The line switch driver can drives large gate capacitance MOSFET with low power consumption. (Typical 8 μA at Vin = 12 V)
Line switch driver operates independent of voltage regulator's state.



Note: This function is independent of state of voltage regulator.

Stability Criteria, Output Voltage Setting for High ESR Output Capacitor

Small output ripple voltage makes control loop unstable in constant on time architecture. Ripple voltage needs to be larger than 15 mV on FB pin. When using high ESR (>50 mΩ) capacitor such as Electrolytic capacitor, Polymer aluminum capacitor for output capacitor, ripple voltage on FB pin will be more than 15 mV.



Stability criteria

From loop stability analysis, constant on time control system must satisfy below equation.

Stability criteria: ESR • Cout > ton / 2

Here, ton is constant on time. If the system cannot satisfy above equation, subharmonic oscillation will occur.

Vout setting

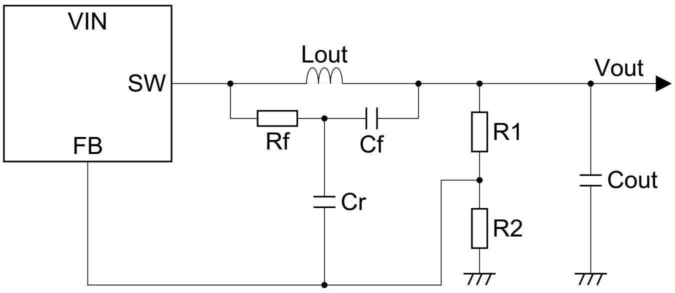
FB comparator compares FB voltage and internal accurate reference voltage (0.8 V). Feedback loop controls FB voltage to match the reference voltage. Therefore, output voltage is set by following equation.

Vout: 0.8 V • (R1+R2) / R2

Here, R1 and R2 is output voltage divider resister (refer to above figure). However, ripple voltage on FB pin affects FB voltage, so Vout slightly shifts from setting value. If the system needs high accuracy, adjust Vout by changing R1, R2 value.

Operating with Small ESR Output Capacitor

When using low-ESR output capacitor like MLCC, voltage ripple on output voltage node is very small. So voltage ripple needs to be enhanced by additional components. Recommended ripple enhance method is like below figure.



Ripple injection on FB pin

Rf and Cf make ripple voltage using inductor DCR ripple. Cr is used for AC ripple injection to FB pin. Ripple voltage between Rf and Cf is described by following equation.

Vripple: (VIN – VOUT) • ton / (Rf • Cf)

Make sure above ripple voltage is larger than 15 mV.

Stability criteria

From loop stability analysis of above circuit configuration, the system must satisfy below equation.

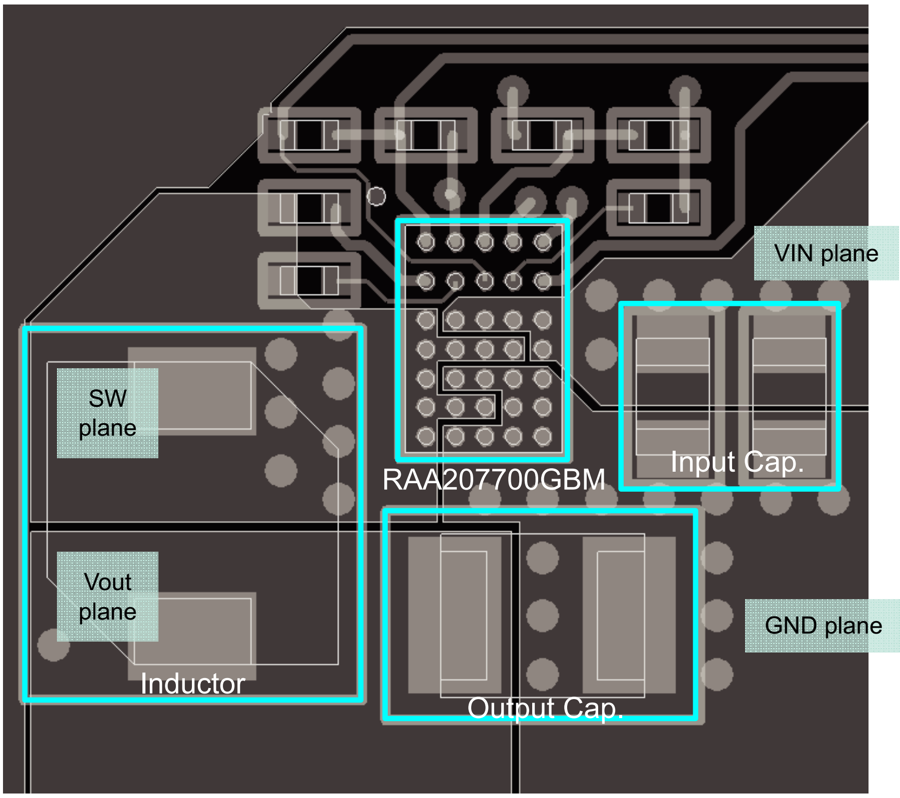
Stability criteria: Lout • Cout / (Rf • Cf) > ton / 2

If the system cannot satisfy above equation, subharmonic oscillation will occur.

Vout setting

Output voltage setting is basically same concept as high ESR capacitor use case. Ripple voltage from injection circuit affects FB voltage, so it need to be adjust R1, R2 for high accuracy system.

Board Layout Example (RAA207700GBM)



Top Layer (Top view)

Representative Inductors

Maker	Inductance [µH]	ΔL/L0 = 20% Change [A]	Dimensions [mm]
NEC Tokin MPC series	0.42	20.0	6.7 × 8.0 × 4.0
	0.60	19.0	6.7 × 8.0 × 5.0
	0.88	24.0	10.0× 11.5 × 4.0
	1.0	25.0	10.0 × 11.7 × 5.5
ALPS Green Device GLMC series	0.47	13.9 *1	6.5 × 7.4 × 3.0
	1.0	10 *1	6.5 × 7.4 × 3.0
	1.5	8.8 *1	6.5 × 7.4 × 3.0
TOKO FDVE0630 series	0.33	15.9	6.7 × 7.4 × 3.0
	0.47	15.6	6.7 × 7.4 × 3.0
	0.75	10.9	6.7 × 7.4 × 3.0
	1.0	9.5	6.7 × 7.4 × 3.0
TDK SPM5030 series	0.35	14.9	5.0 × 5.2 × 3.0
	0.47	11.0	5.0 × 5.2 × 3.0
	0.75	9.7	5.0 × 5.2 × 3.0

Note: *1 30% change

- Small size inductor for RAA207702GBM

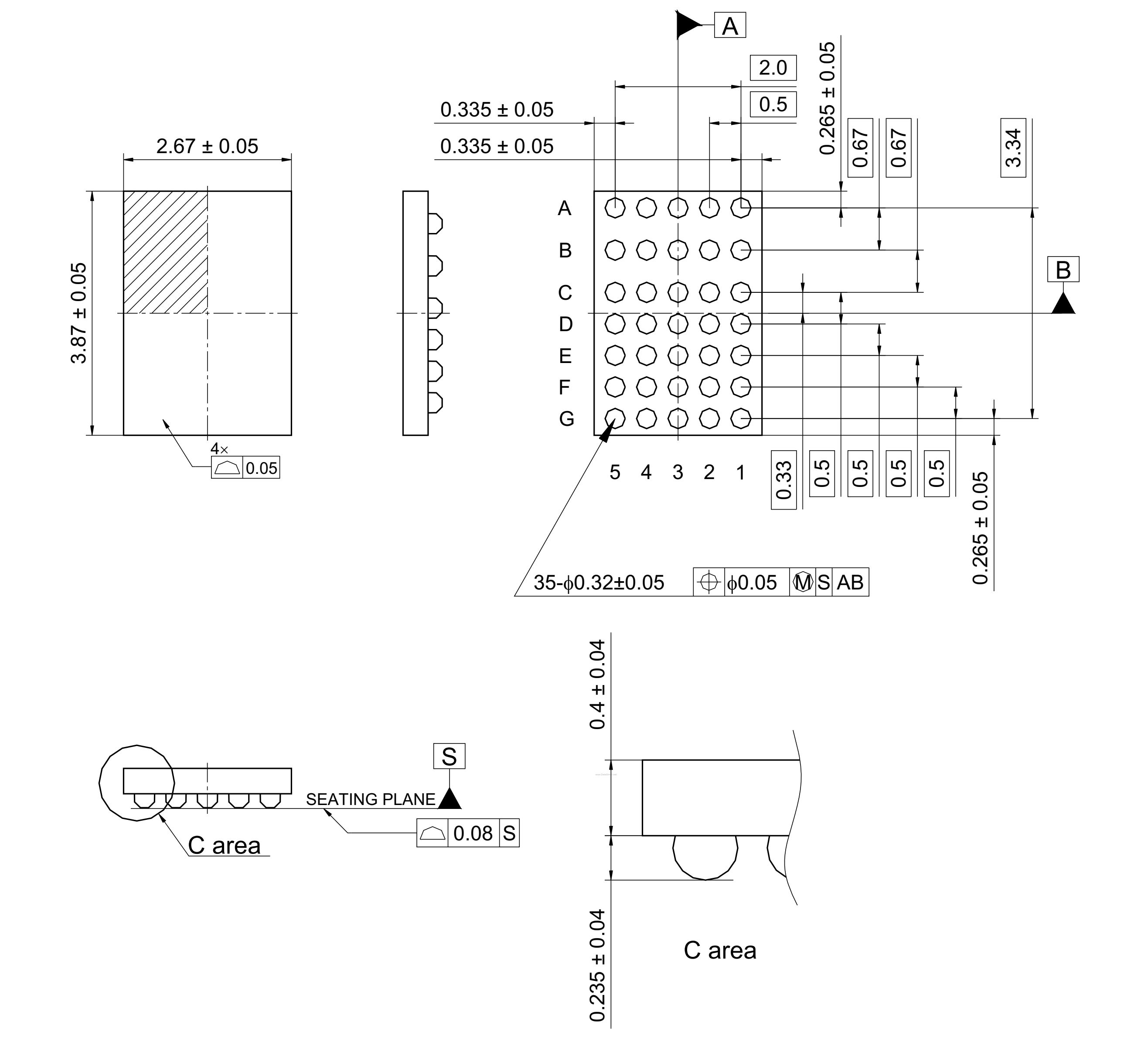
Maker	Inductance [µH]	ΔL/L0 = 30% Change [A]	Dimensions [mm]
TOKO FDSD0420 series	0.68	8.3	4.2 × 4.2 × 2.0
	1.0	6.8	4.2 × 4.2 × 2.0
	1.5	5.7	4.2 × 4.2 × 2.0
TDK SPM4012 series	0.47	8.3	4.4 × 4.1 × 1.2
	1.0	4.8	4.4 × 4.1 × 1.2

Representative Output Capacitors

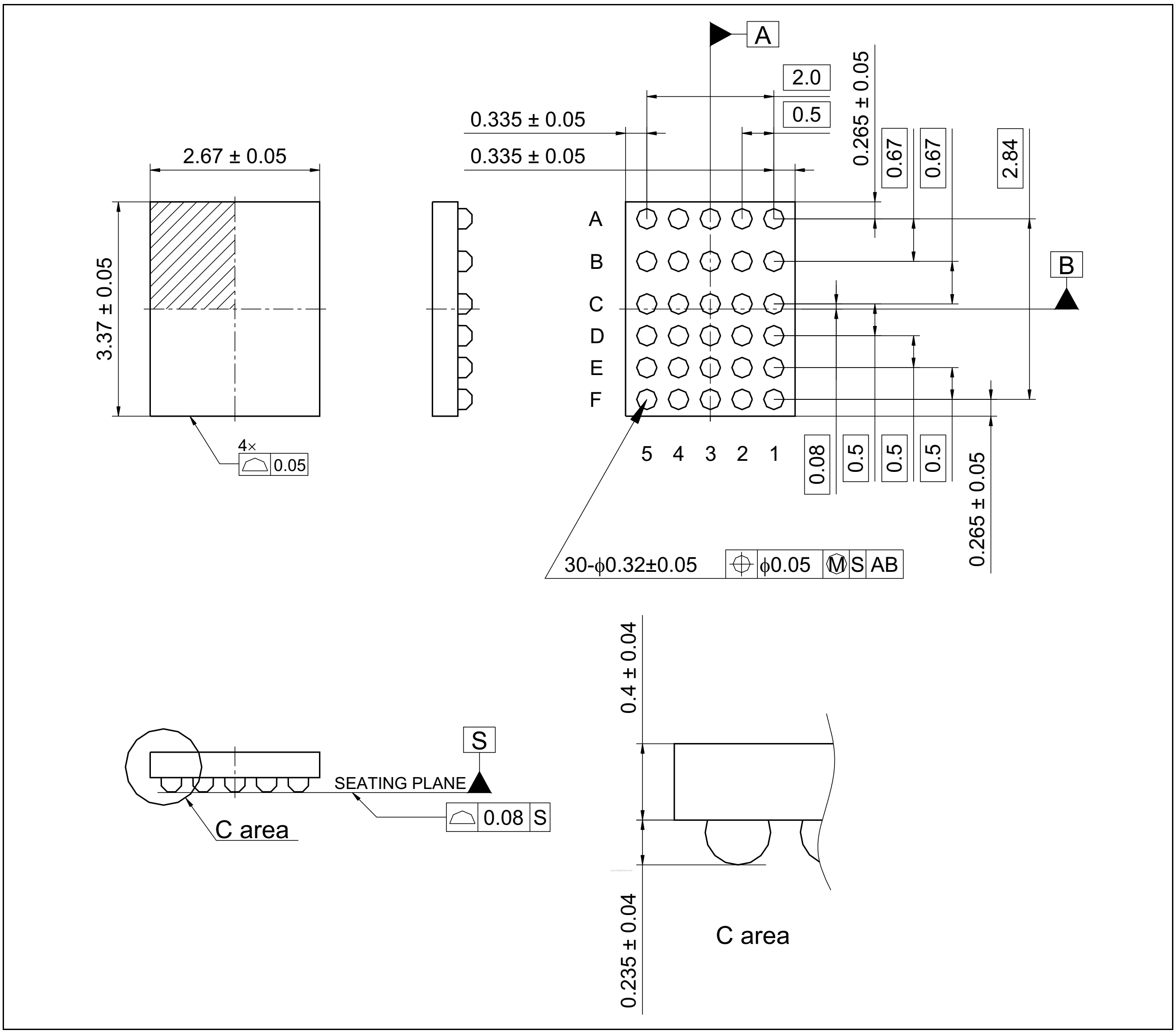
Maker	Maximum Voltage [V]	Capacitance [µF]
Sanyo POSCAP series	2.0 to 10	47 to 330
Sanyo OS-CON series	2.0 to 10	47 to 330
Murata MLCC series	6.3 to 10	22 to 47
TDK MLCC series	6.3 to 10	22 to 47
TAIYO YUDEN MLCC series	6.3 to 10	22 to 47

Package Dimensions

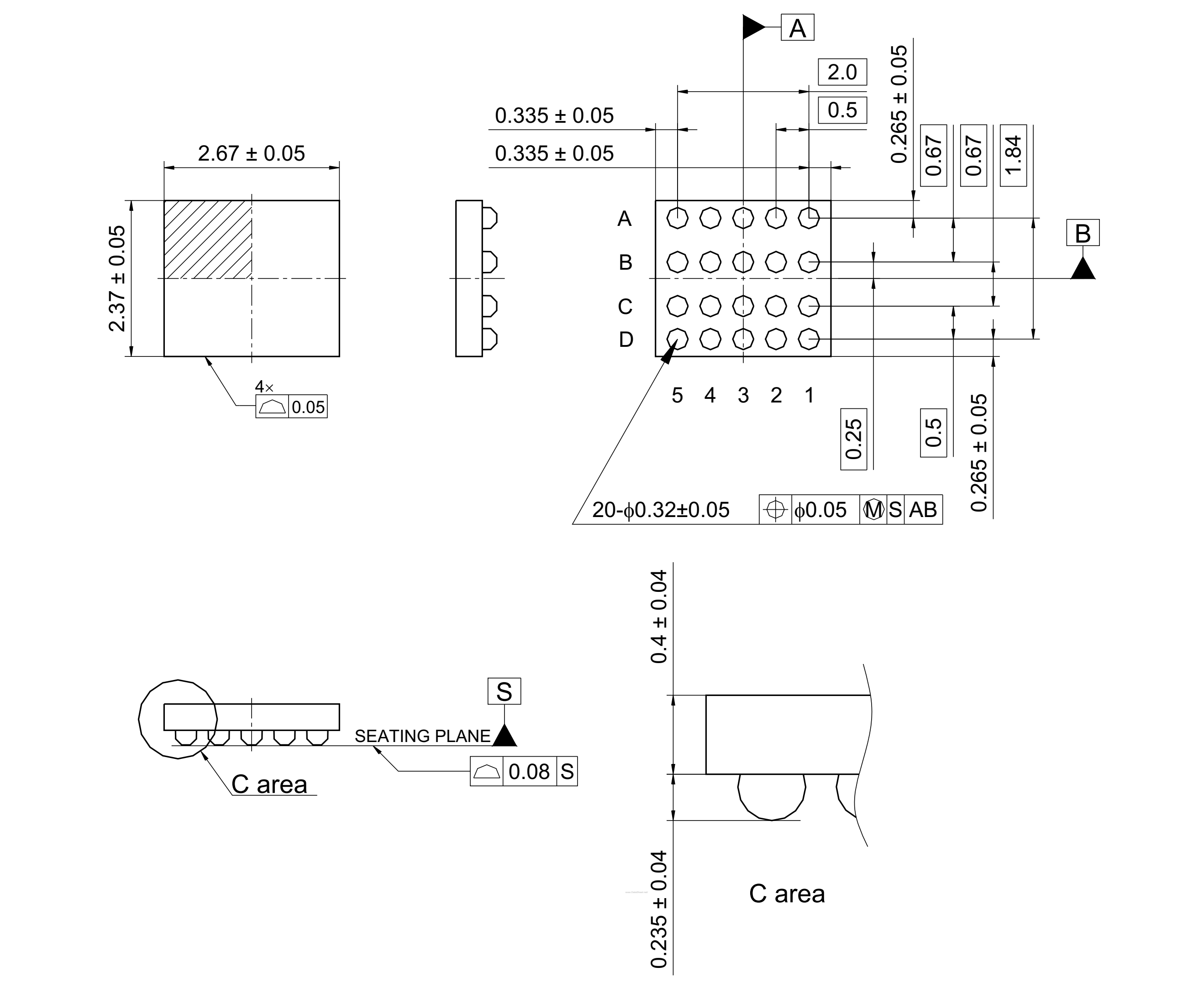
- RAA207700GBM



- RAA207701GBM



- RAA207702GBM



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