

**AOD4142**
**N-Channel SDMOS™ POWER Transistor**
**General Description**

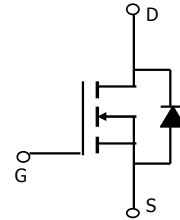
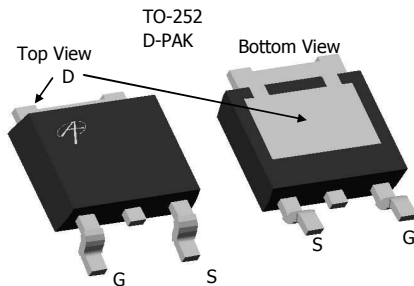
The AOD4142 is fabricated with SDMOS™ trench technology that combines excellent  $R_{DS(ON)}$  with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free\*

**Features**

$V_{DS}$  (V) = 25V  
 $I_D$  = 50A ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 5.3m $\Omega$  ( $V_{GS}$  = 10V)  
 $R_{DS(ON)}$  < 9.8m $\Omega$  ( $V_{GS}$  = 4.5V)

**100% UIS Tested!**  
**100%  $R_g$  Tested!**


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	50	A
$T_C=25^\circ\text{C}$		43	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	120	
Continuous Drain Current <sup>A</sup>	$I_{DSM}$	17	
$T_A=25^\circ\text{C}$		13	
Avalanche Current <sup>C</sup>	$I_{AR}$	50	
Repetitive avalanche energy $L=50\mu\text{H}$ <sup>C</sup>	$E_{AR}$	63	mJ
Power Dissipation <sup>B</sup>	$P_D$	50	W
$T_C=25^\circ\text{C}$		25	
Power Dissipation <sup>A</sup>	$P_{DSM}$	2.5	W
$T_A=25^\circ\text{C}$		1.6	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	15	20	$^\circ\text{C/W}$
$t \leq 10\text{s}$		41	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JC}$	2.1	3	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	25			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			10 50	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	2	2.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	120			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =30A		4.4	5.3	mΩ
		T <sub>J</sub> =125°C		6.6	7.9	
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		7.8	9.8	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =30A		65		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				50	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =12.5V, f=1MHz	1440	1800	2160	pF
C <sub>oss</sub>	Output Capacitance		310	445	580	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		170	285	400	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.8	1.6	2.4	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =12.5V, I <sub>D</sub> =30A	25	31	37	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge		12	15	18	nC
Q <sub>gs</sub>	Gate Source Charge		4	4.8	6	nC
Q <sub>gd</sub>	Gate Drain Charge		5.3	8.9	13	nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =12.5V, R <sub>L</sub> =0.42Ω, R <sub>GEN</sub> =3Ω		8		ns
t <sub>r</sub>	Turn-On Rise Time			10.4		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			29		ns
t <sub>f</sub>	Turn-Off Fall Time			9		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =30A, dI/dt=500A/μs	9.6	12	14	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =30A, dI/dt=500A/μs	17	21	25	nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

Rev1 : Oct 2008

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

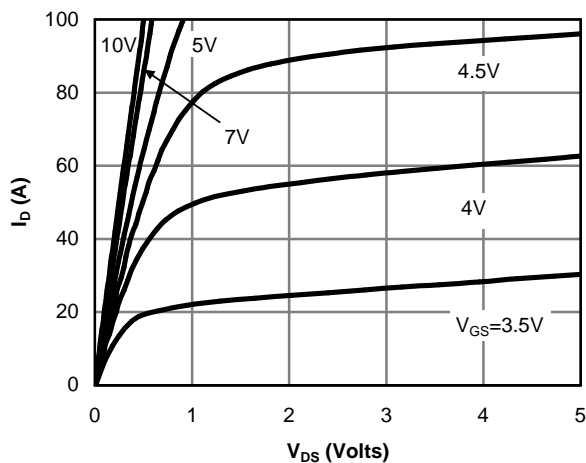


Fig 1: On-Region Characteristics

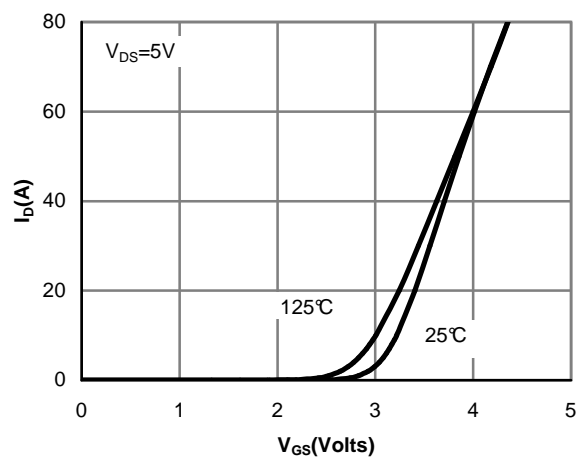


Figure 2: Transfer Characteristics

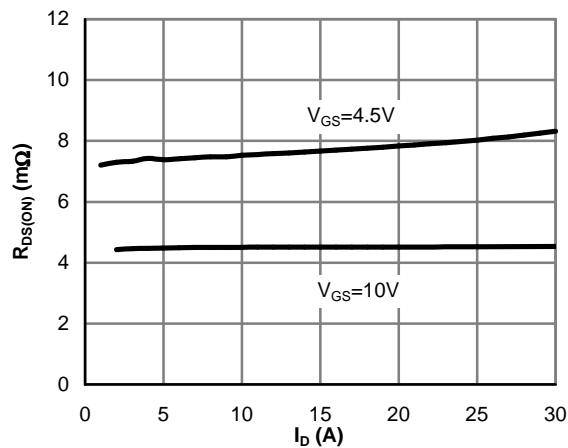


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

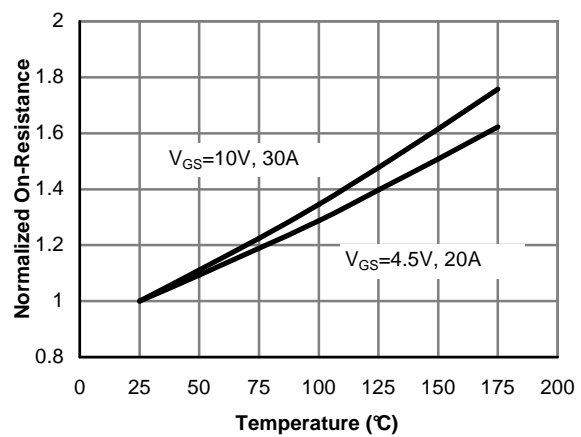


Figure 4: On-Resistance vs. Junction Temperature

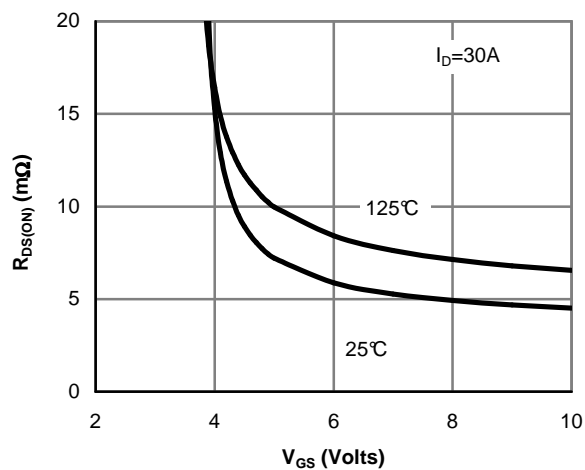


Figure 5: On-Resistance vs. Gate-Source Voltage

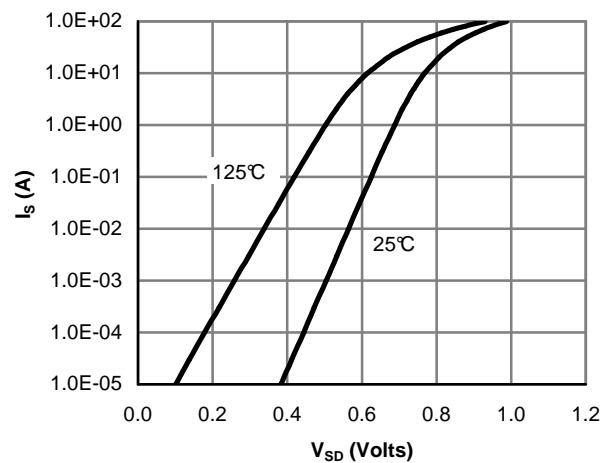


Figure 6: Body-Diode Characteristics

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

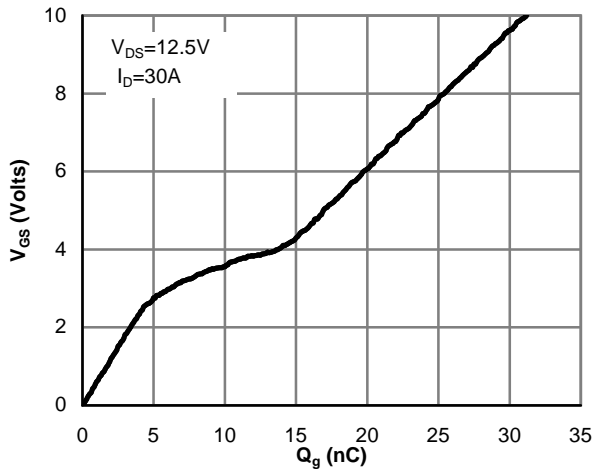


Figure 7: Gate-Charge Characteristics

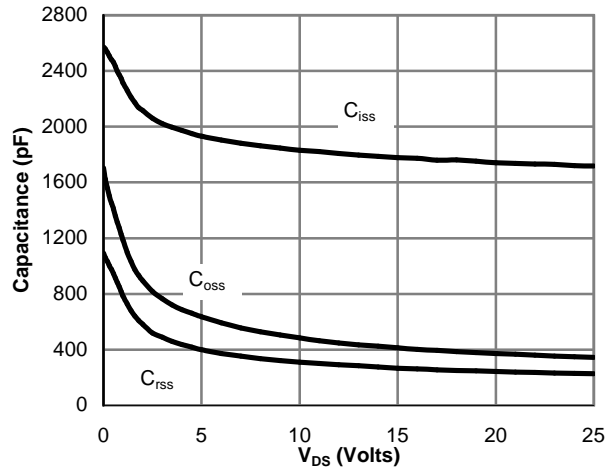


Figure 8: Capacitance Characteristics

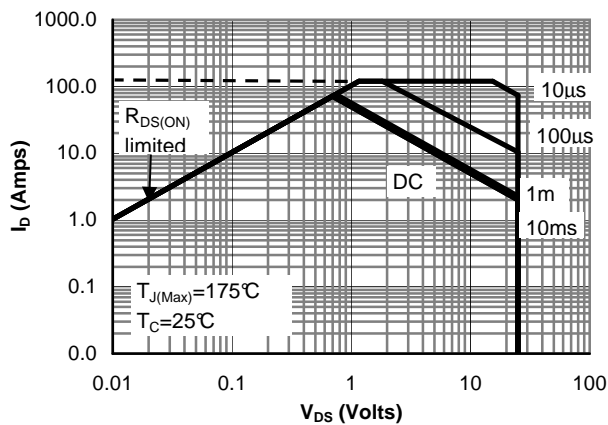


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

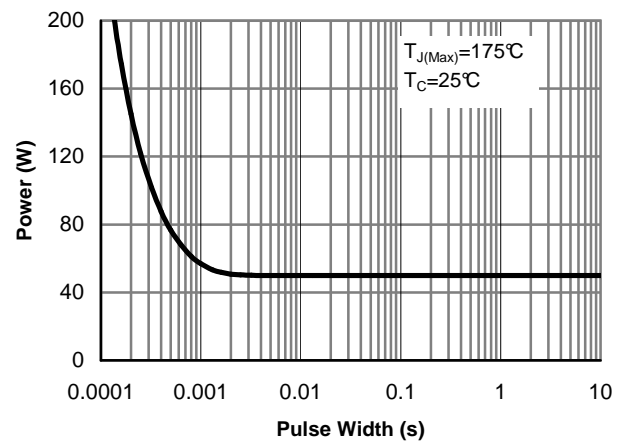


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

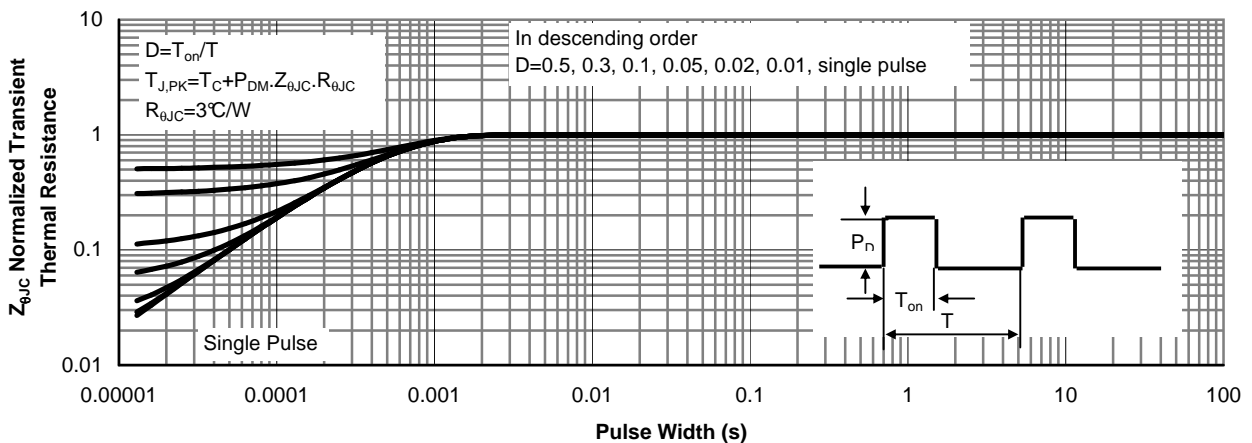


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

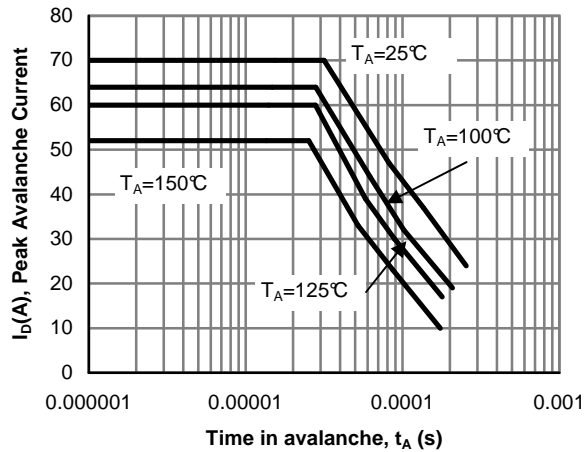


Figure 12: Single Pulse Avalanche capability

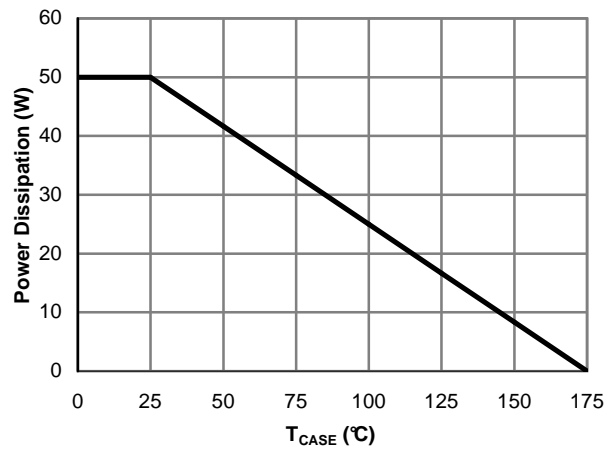


Figure 13: Power De-rating (Note F)

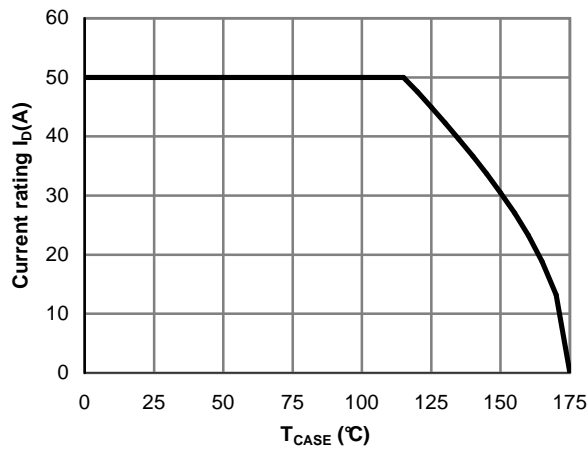


Figure 14: Current De-rating (Note F)

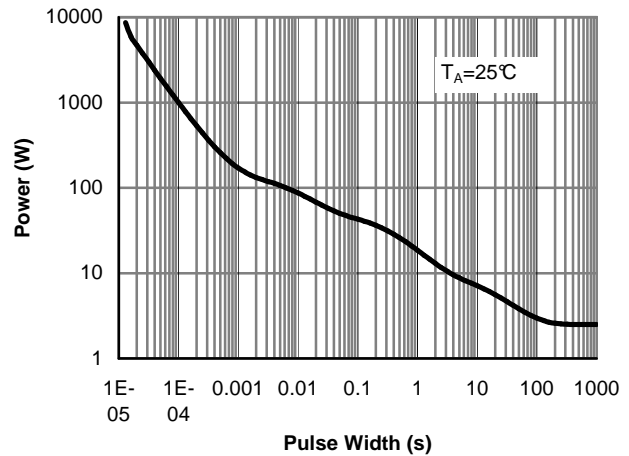


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

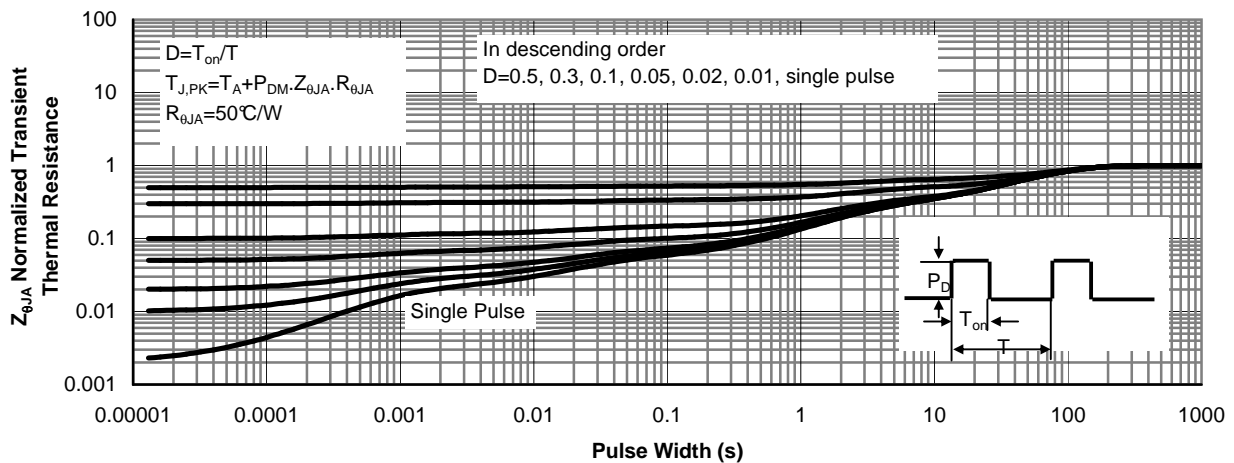


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

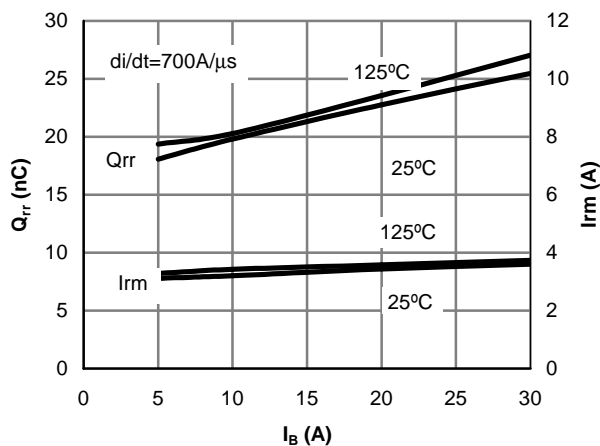


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

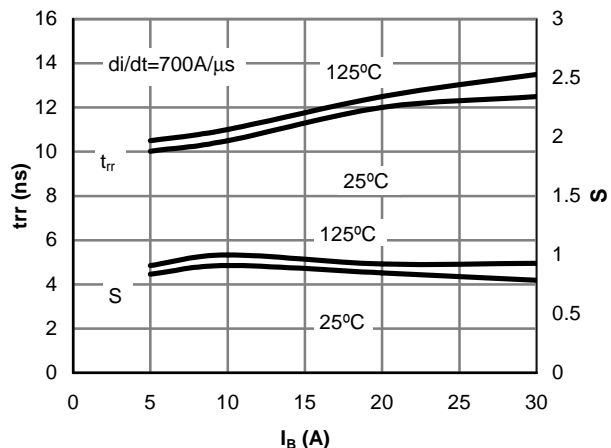


Figure 18: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

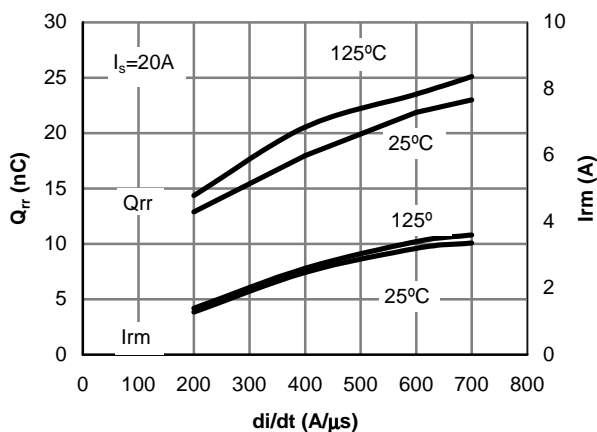


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

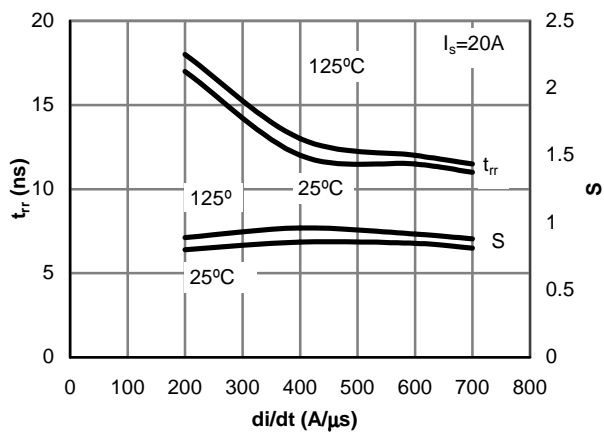
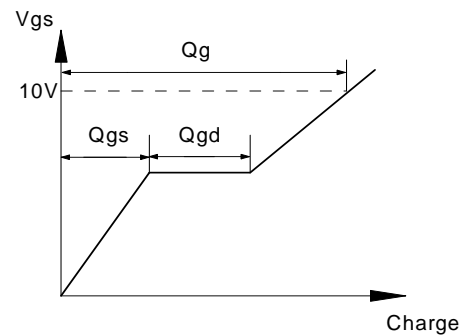
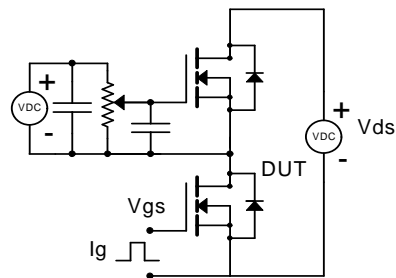
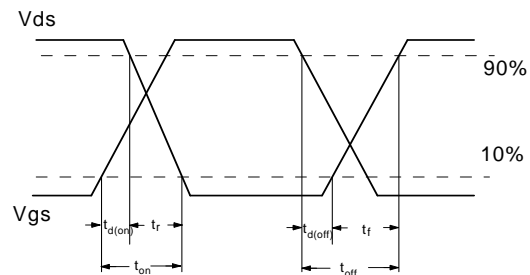
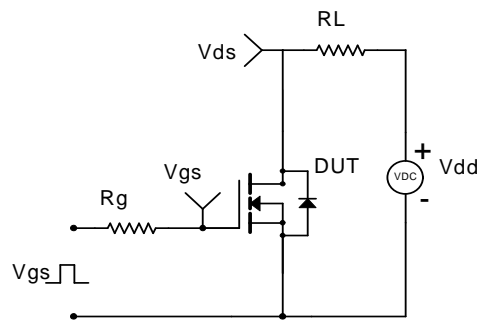


Figure 20: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt

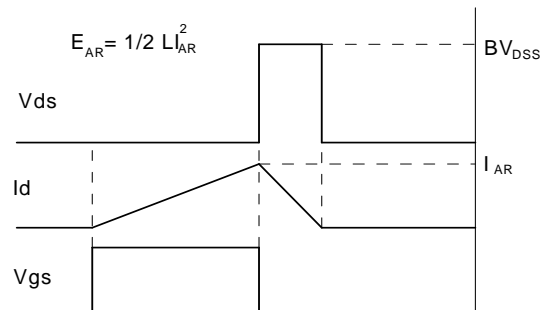
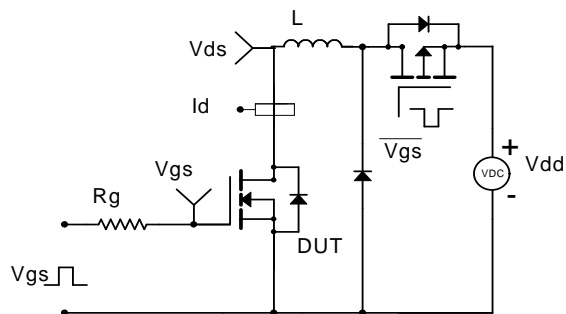
### Gate Charge Test Circuit & Waveform



## Resistive Switching Test Circuit & Waveforms



## Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



## Diode Recovery Test Circuit & Waveforms

