

## MSC23B236A-xxBS8/DS8

2,097,152-Word × 36-Bit DRAM MODULE : FAST PAGE MODE TYPE

### DESCRIPTION

The Oki MSC23B236A-xxBS8/DS8 is a fully decoded 2,097,152-word × 36-bit CMOS dynamic random access memory composed of four 16-Mb (1M × 16) DRAMs in SOJ and four 2-Mb (1M × 2) DRAMs in SOJ. The mounting of eight DRAMs together with decoupling capacitors on a 72-pin glass epoxy SIMM Package supports any application where high density and large capacity of storage memory are required.

### FEATURES

- 2,097,152-word × 36-bit (Parity) organization
- 72-pin SIMM
  - MSC23B236A-xxBS8 : Gold tab
  - MSC23B236A-xxDS8 : Solder tab
- Single 5 V supply ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, 3-state, nonlatch
- Refresh : 1024 cycles/16 ms
- $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
- Fast Page Mode capability

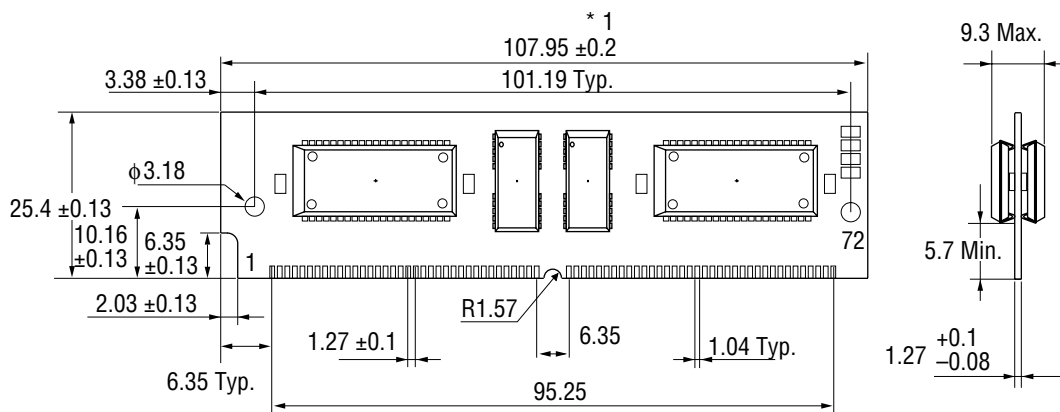
### PRODUCT FAMILY

Family	Access Time (Max.)			Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>		Operating (Max.)	Standby (Max.)
MSC23B236A-60BS8/DS8	60 ns	30 ns	15 ns	110 ns	3410 mW	44 mW
MSC23B236A-70BS8/DS8	70 ns	35 ns	20 ns	130 ns	3080 mW	

## PIN CONFIGURATION

## MSC23B236A-xxBS8/DS8

(Unit : mm)

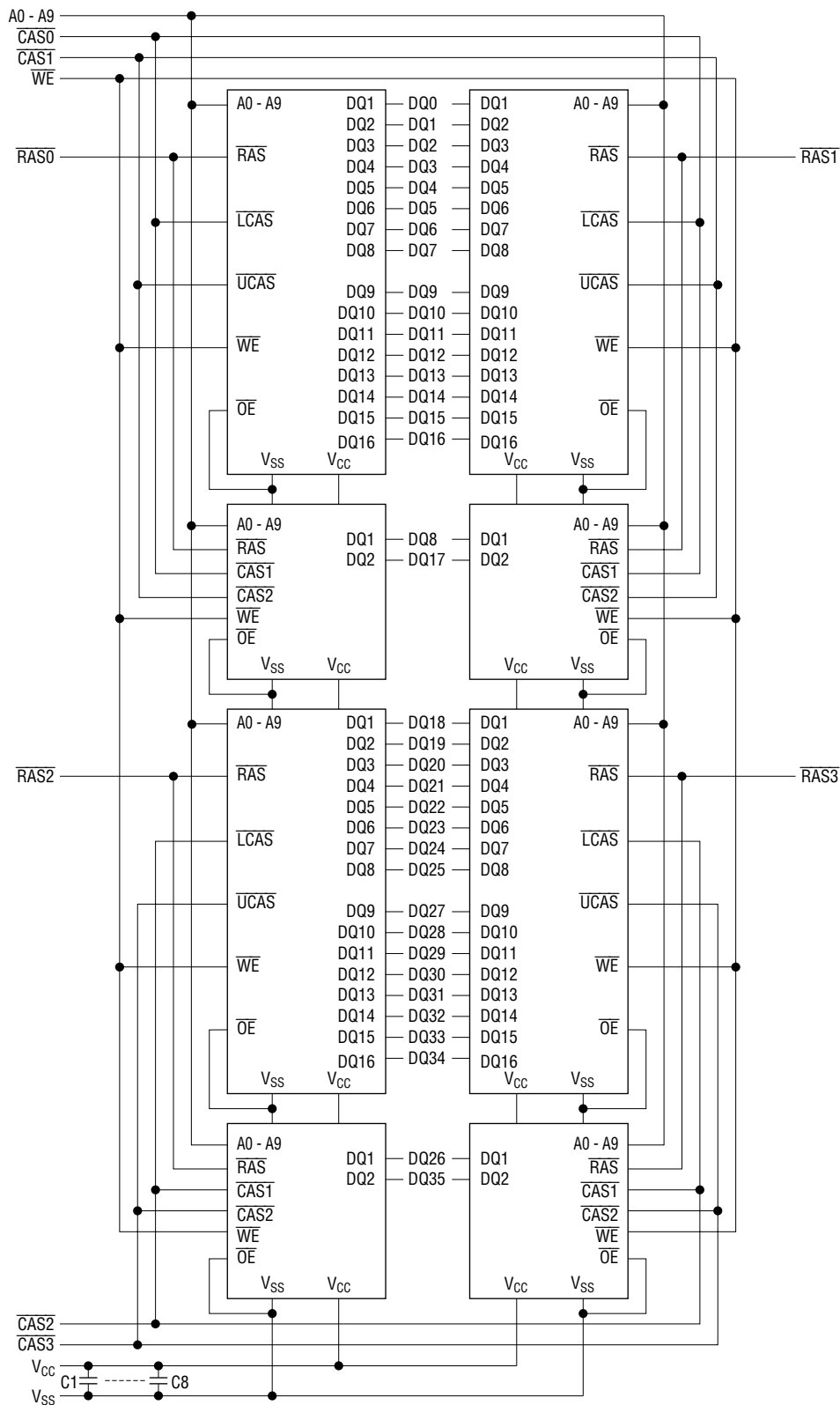


Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>SS</sub>	16	A4	31	A8	46	NC	61	DQ14
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ33
3	DQ18	18	A6	33	$\overline{RAS3}$	48	NC	63	DQ15
4	DQ1	19	NC	34	$\overline{RAS2}$	49	DQ9	64	DQ34
5	DQ19	20	DQ4	35	DQ26	50	DQ27	65	DQ16
6	DQ2	21	DQ22	36	DQ8	51	DQ10	66	NC
7	DQ20	22	DQ5	37	DQ17	52	DQ28	67	PD1
8	DQ3	23	DQ23	38	DQ35	53	DQ11	68	PD2
9	DQ21	24	DQ6	39	V <sub>SS</sub>	54	DQ29	69	PD3
10	V <sub>CC</sub>	25	DQ24	40	$\overline{CAS0}$	55	DQ12	70	PD4
11	NC	26	DQ7	41	$\overline{CAS2}$	56	DQ30	71	NC
12	A0	27	DQ25	42	$\overline{CAS3}$	57	DQ13	72	V <sub>SS</sub>
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	NC	44	$\overline{RAS0}$	59	V <sub>CC</sub>		
15	A3	30	V <sub>CC</sub>	45	$\overline{RAS1}$	60	DQ32		

## Presence Detect Pins

Pin No.	Pin Name	MSC23B236A -60BS8/DS8	MSC23B236A -70BS8/DS8
67	PD1	NC	NC
68	PD2	NC	NC
69	PD3	NC	V <sub>SS</sub>
70	PD4	NC	NC

## BLOCK DIAGRAM



## ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1.0 to 7.0	V
Voltage $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-1.0 to 7.0	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D$	9.2	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-40 to 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Recommended Operating Conditions

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.4	—	6.5	V
Input Low Voltage	$V_{IL}$	-1.0	—	0.8	V

### Capacitance

( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	$C_{IN1}$	—	53	pF
Input Capacitance ( $\overline{WE}$ )	$C_{IN2}$	—	65	pF
Input Capacitance ( $\overline{RAS0} - \overline{RAS3}$ )	$C_{IN3}$	—	20	pF
Input Capacitance ( $\overline{CAS0} - \overline{CAS3}$ )	$C_{IN4}$	—	35	pF
I/O Capacitance (DQ0 - DQ35)	$C_{DQ}$	—	20	pF

Note : Capacitance measured with Boonton Meter.

# DC Characteristics

( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Condition	MSC23B236A -60BS8/DS8		MSC23B236A -70BS8/DS8		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	$I_{LI}$	$0\text{ V} \leq V_I \leq 6.5\text{ V}$ ; All other pins not under test = $0\text{ V}$	-80	80	-80	80	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	$\overline{D_{OUT}}$ disable $0\text{ V} \leq V_O \leq 5.5\text{ V}$	-20	20	-20	20	$\mu\text{A}$	
Output High Voltage	$V_{OH}$	$I_{OH} = -5.0\text{ mA}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 4.2\text{ mA}$	0	0.4	0	0.4	V	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{RAS}$ , $\overline{CAS}$ cycling, $t_{RC} = \text{Min.}$	—	620	—	560	mA	1, 2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{RAS}$ , $\overline{CAS} = V_{IH}$	—	16	—	16	mA	1
		$\overline{RAS}$ , $\overline{CAS}$ $\geq V_{CC} - 0.2\text{ V}$	—	8	—	8	mA	1
Average Power Supply Current (RAS-only Refresh)	$I_{CC3}$	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ , $t_{RC} = \text{Min.}$	—	620	—	560	mA	1, 2
Average Power Supply Current (CAS before RAS Refresh)	$I_{CC6}$	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$ , $t_{RC} = \text{Min.}$	—	620	—	560	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	$\overline{RAS} = V_{IL}$ , $\overline{CAS}$ cycling, $t_{PC} = \text{Min.}$	—	480	—	450	mA	1, 3

Notes: 1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.  
2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .  
3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1,2,3

Parameter	Symbol	MSC23B236A -60BS8/DS8		MSC23B236A -70BS8/DS8		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t <sub>RC</sub>	110	—	130	—	ns	
Fast Page Mode Cycle Time	t <sub>PC</sub>	40	—	45	—	ns	
Access Time from $\overline{\text{RAS}}$	t <sub>RAC</sub>	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t <sub>CAC</sub>	—	15	—	20	ns	4, 5
Access Time from Column Address	t <sub>AA</sub>	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t <sub>CPA</sub>	—	35	—	40	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t <sub>CLZ</sub>	0	—	0	—	ns	4
Output Buffer Turn-off Delay Time	t <sub>OFF</sub>	0	15	0	20	ns	7
Transition Time	t <sub>T</sub>	3	50	3	50	ns	3
Refresh Period	t <sub>REF</sub>	—	16	—	16	ms	
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	60	10k	70	10k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t <sub>RASP</sub>	60	100k	70	100k	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t <sub>CP</sub>	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	15	10k	20	10k	ns	
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5	—	5	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t <sub>RHCP</sub>	35	—	40	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	15	30	15	35	ns	6
Row Address Set-up Time	t <sub>ASR</sub>	0	—	0	—	ns	
Row Address Hold Time	t <sub>RAH</sub>	10	—	10	—	ns	
Column Address Set-up Time	t <sub>ASC</sub>	0	—	0	—	ns	
Column Address Hold Time	t <sub>CAH</sub>	15	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t <sub>AR</sub>	50	—	55	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	30	—	35	—	ns	

## AC Characteristics (2/2)

(V<sub>CC</sub> = 5 V ±10%, Ta = 0°C to 70°C) Note 1,2,3

Parameter	Symbol	MSC23B236A -60BS8/DS8		MSC23B236A -70BS8/DS8		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	ns	
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	ns	8
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	ns	
Write Command Hold Time	t <sub>WCH</sub>	10	—	15	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t <sub>WCR</sub>	45	—	55	—	ns	
Write Command Pulse Width	t <sub>WP</sub>	10	—	15	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	15	—	20	—	ns	
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	ns	
Data-in Hold Time	t <sub>DH</sub>	15	—	15	—	ns	
Data-in Hold Time from $\overline{\text{RAS}}$	t <sub>DHR</sub>	50	—	55	—	ns	
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	10	—	15	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>WRP</sub>	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>WRH</sub>	10	—	10	—	ns	

- Notes:
1. A start-up delay of 200  $\mu$ s is required after power-up followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.  
When using the internal refresh counter, a minimum of eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  initialization cycles is required.
  2. AC measurement assume  $t_T = 5$  ns.
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}$  (Max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.

**See ADDENDUM B for AC Timing Waveforms**