




## Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications

( V ) Final Specifications

Module	11.6"(11.57") HD 16:9 Color TFT-LCD with LED Backlight design
Model Name	B116XTN04.0 (H/W:0A)
Note (  )	<i>LED Backlight with driving circuit design</i>

Customer	Date
Checked & Approved by	Date
Note: This Specification is subject to change without notice.	

Approved by	Date
<u>Kevin Shen</u>	<u>8/15/2012</u>
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## Contents

<b>1. Handling Precautions</b>	<b>4</b>
<b>2. General Description</b>	<b>5</b>
2.1 General Specification	5
2.2 Optical Characteristics	6
<b>3. Functional Block Diagram</b>	<b>11</b>
<b>4. Absolute Maximum Ratings</b>	<b>12</b>
4.1 Absolute Ratings of TFT LCD Module	12
4.2 Absolute Ratings of Environment	12
<b>5. Electrical Characteristics</b>	<b>13</b>
5.1 TFT LCD Module	13
5.2 Backlight Unit	15
<b>6. Signal Interface Characteristic</b>	<b>16</b>
6.1 Pixel Format Image	16
6.2 The Input Data Format	17
6.3 Integration Interface Requirement	18
6.4 Interface Timing	20
<b>7. Panel Reliability Test</b>	<b>22</b>
7.1 Vibration Test	22
7.2 Shock Test	22
7.3 Reliability Test	22
<b>8. Mechanical Characteristics</b>	<b>23</b>
8.1 LCM Outline Dimension	23
<b>9. Shipping and Package</b>	<b>25</b>
9.1 Shipping Label Format	25
9.2 Carton Package	26
9.3 Shipping Package of Palletizing Sequence	27
<b>10. Appendix: EDID Description</b>	<b>29</b>



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AU OPTRONICS CORPORATION

### Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2012/02/29	All	First Edition for Customer	-	-
0.1 2012/03/15	28	TBD	Update EDID	
0.1 2012/03/27	6	TBD	Update Color / Chromaticity Coordinates	

## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentarily. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrosatic breakdown.

## 2. General Description

B116XTN04.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 HD, 1366(H) x 768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are LVDS interface compatible.

B116XTN04.0 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	293.8			
Active Area	[mm]	256.125 X 144.0			
Pixels H x V		1366x3(RGB) x 768			
Pixel Pitch	[mm]	0.1875 x 0.1875			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally White			
White Luminance (I <sub>LED</sub> =20mA) (Note: I <sub>LED</sub> is LED current)	[cd/m <sup>2</sup> ]	200 typ. (5 points average) 170 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		400 typ			
Response Time	[ms]	8 typ / 16 Max			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	2.9 max. (Include Logic and BLU power)			
Weight	[Grams]	235 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	267.5	268.0	268.5
		Width	174.0	174.5	175.0
		Thickness	-	-	3.6
Electrical Interface		1 channel LVDS			
Glass Thickness	[mm]	0.5			
Surface Treatment		Anti-Glare, Hardness 3H Reflection 4.3%			
Support Color		262K colors ( RGB 6-bit )			

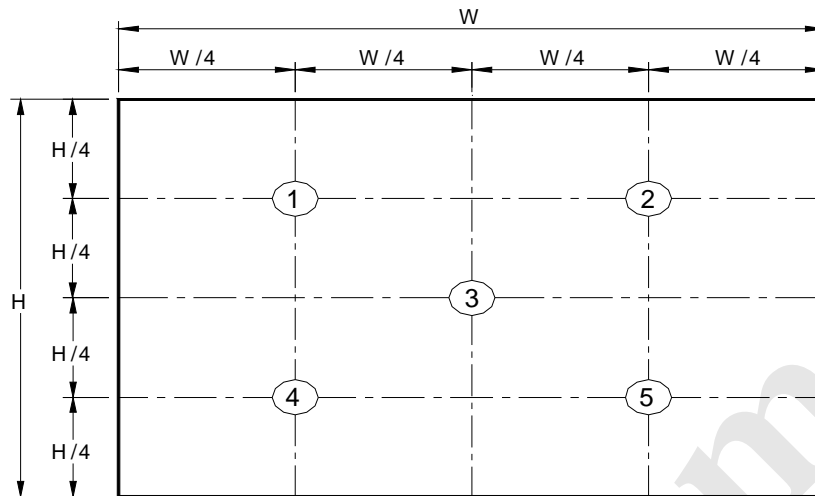
Temperature Range Operating Storage (Non-Operating)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

## 2.2 Optical Characteristics

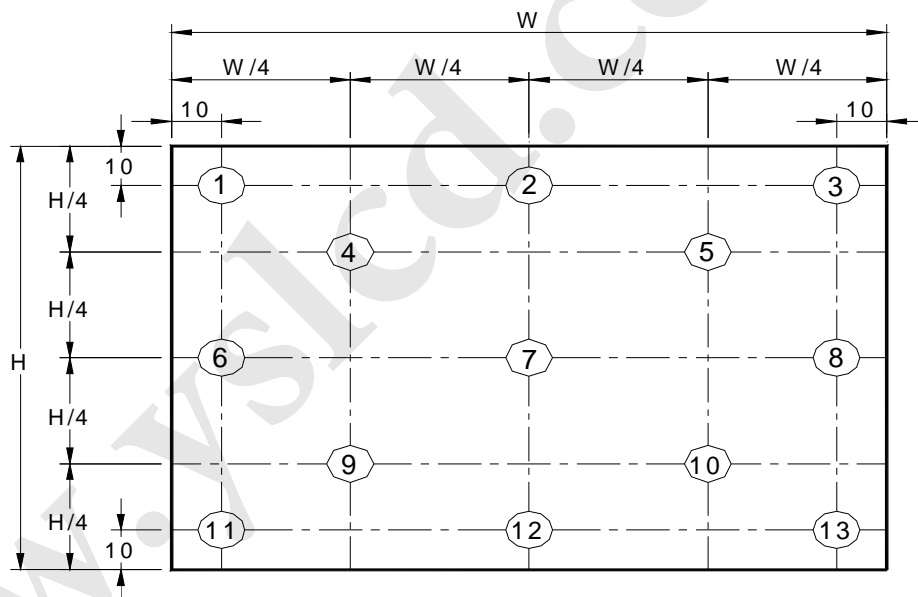
The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance I <sub>LED</sub> =20mA		5 points average	170	200	-	cd/m <sup>2</sup>	1, 4, 5.
Viewing Angle	$\theta_R$	Horizontal (Right)	40	45	-	degree	4, 9
	$\theta_L$	CR = 10 (Left)	40	45	-		
	$\phi_H$	Vertical (Upper)	10	15	-		
	$\phi_L$	CR = 10 (Lower)	30	35	-		
Luminance Uniformity	$\delta_{5P}$	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	$\delta_{13P}$	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		300	400	-		4, 6
Cross talk	%				4		4, 7
Response Time	T <sub>RT</sub>	Rising + Falling	-	8	16	msec	4, 8
Color / Chromaticity Coordinates	Red	R <sub>x</sub>	0.555	0.585	0.615	CIE 1931	4
		R <sub>y</sub>	0.313	0.343	0.373		
	Green	G <sub>x</sub>	0.292	0.322	0.352		
		G <sub>y</sub>	0.51	0.54	0.57		
	Blue	B <sub>x</sub>	0.125	0.155	0.185		
		B <sub>y</sub>	0.118	0.148	0.178		
	White	W <sub>x</sub>	0.283	0.313	0.343		
		W <sub>y</sub>	0.299	0.329	0.359		
NTSC	%		-	45	-		

**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

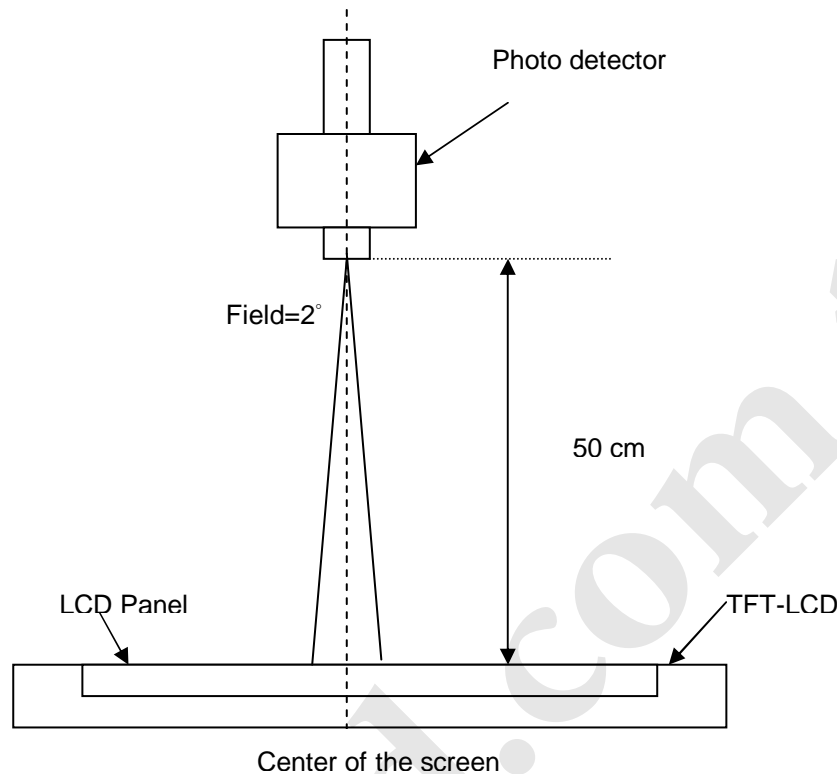
$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, measurement should be executed in the

center of screen unless otherwise noted.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ,  $Y_L = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$

$L(x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

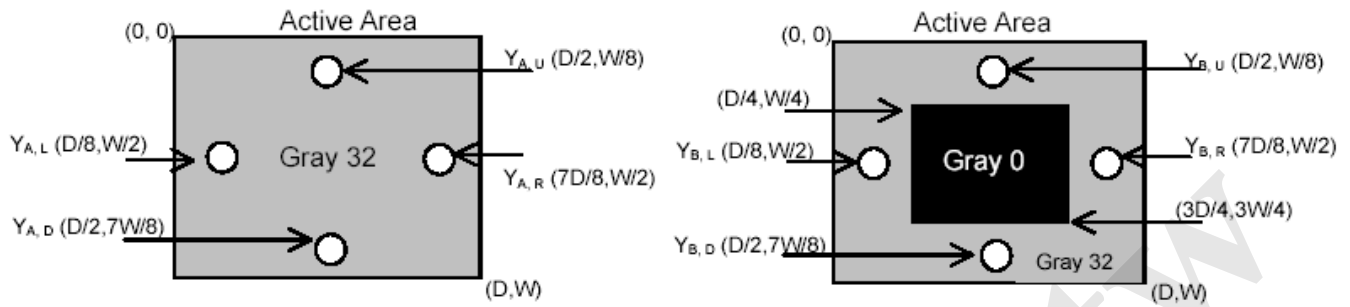
**Note 7 :** Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

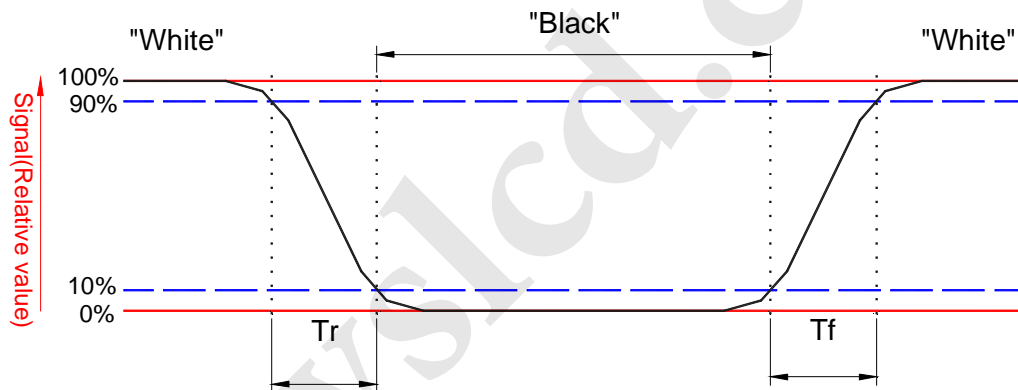
$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



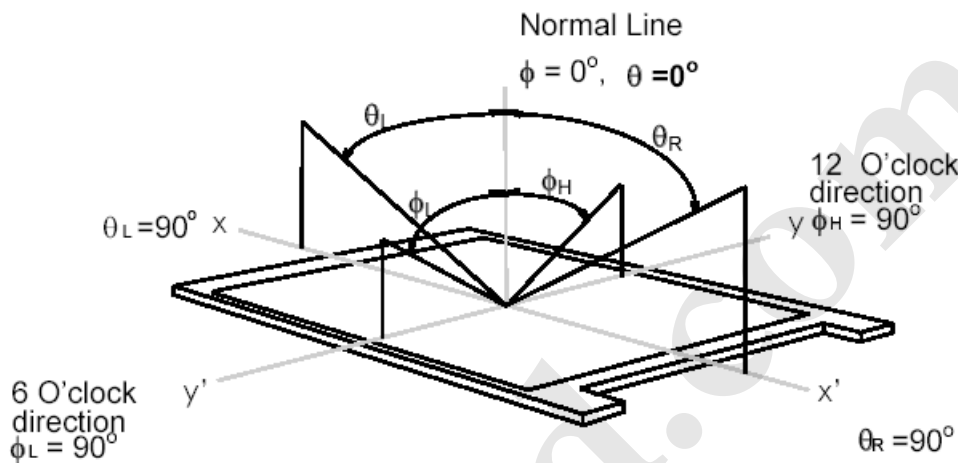
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time is interval between the 10% and 90% of amplitudes. Refer to figure as below.



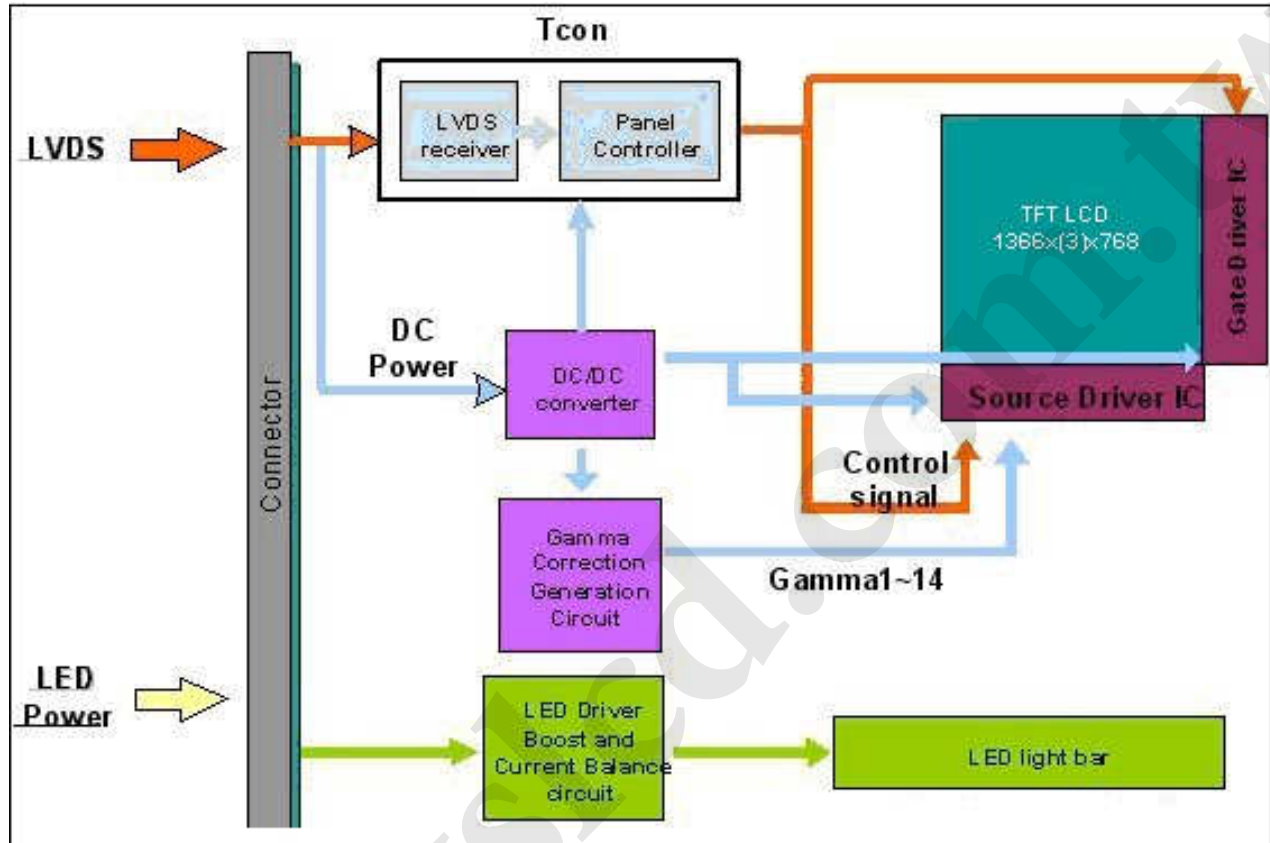
## Note 9. Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 11.6 inches wide Color TFT/LCD 40 Pin one channel Module



## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Environment

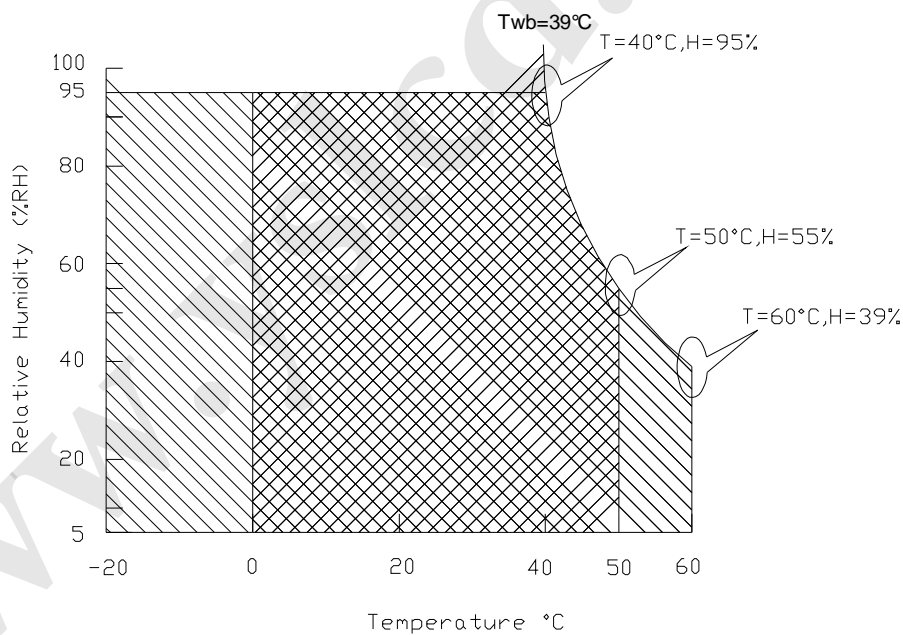
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )


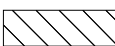
Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range 

Storage Range  + 

## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

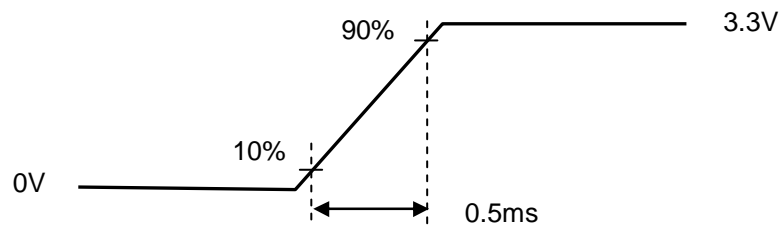
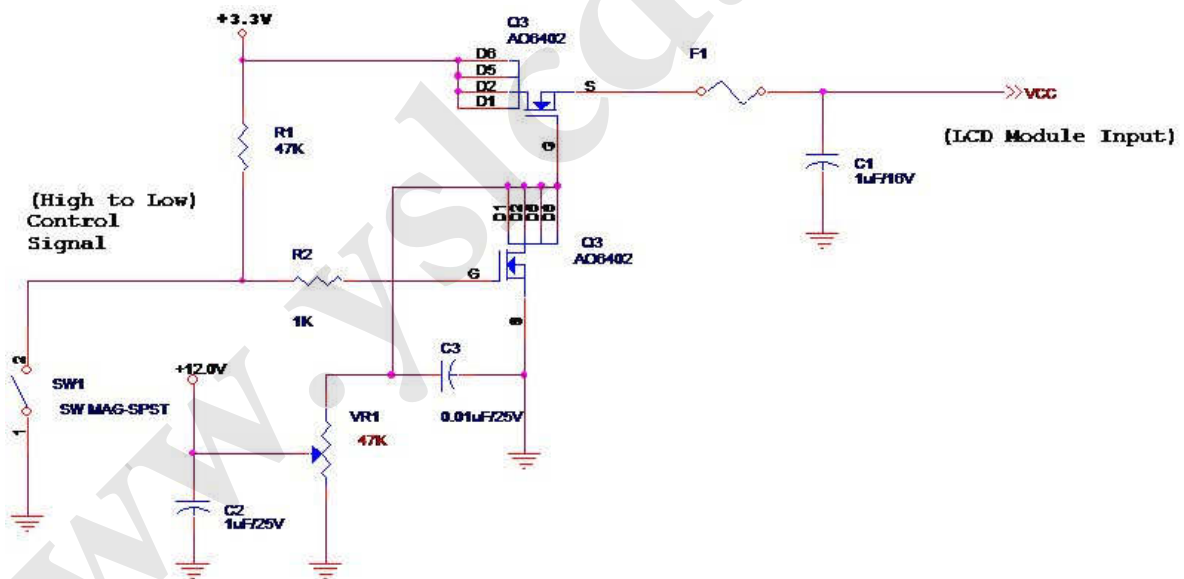
Input power specifications are as follows;

The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.8	[Watt]	Note 1
IDD	IDD Current	-	-	242	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ( $P_{max}=V_{3.3} \times I_{black}$ )

Note 2 : Measure Condition



Vin rising time

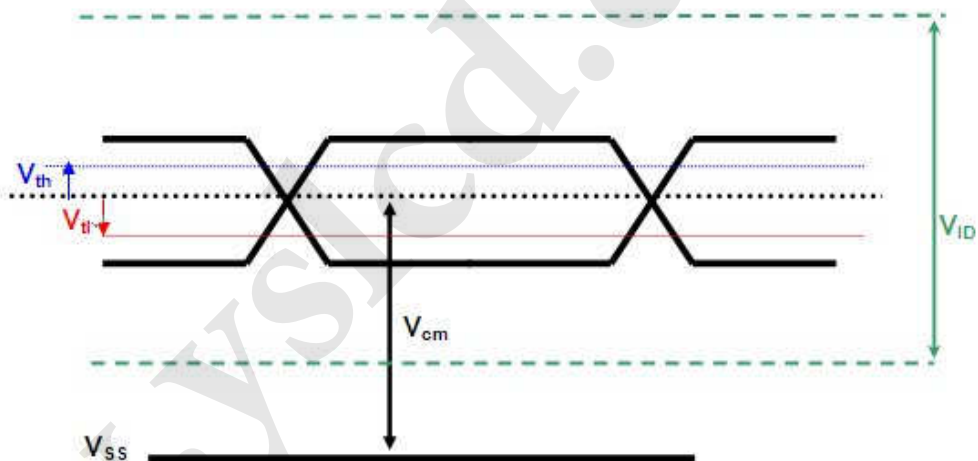
## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
$V_{th}$	Differential Input High Threshold ( $V_{cm}=+1.2V$ )		100	[mV]
$V_{tl}$	Differential Input Low Threshold ( $V_{cm}=+1.2V$ )	-100	-	[mV]
$V_{ID}$	Differential Input Voltage	100	600	[mV]
$V_{cm}$	Differential Input Common Mode Voltage	1.125	1.375	[V]

Note: LVDS Signal Waveform





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AU OPTRONICS CORPORATION

### 5.2 Backlight Unit

#### 5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	2.08	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	10,000	-	-	Hour	(Ta=25°C), Note 2 If=20 mA

**Note 1:** Calculator value for reference  $P_{LED} = V_F$  (Normal Distribution) \*  $I_F$  (Normal Distribution) / Efficiency, and PLED include driving circuit loss.

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

#### 5.2.2 Backlight input signal characteristics

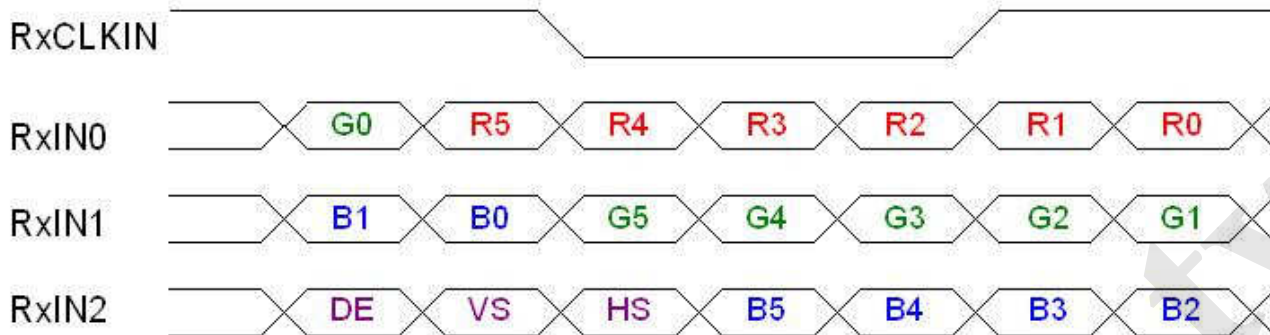
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	6.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	1K	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

**Note 1:** Recommend system pull up/down resistor no bigger than 10kohm

**Note 2:** If the PWM duty ratio(min) is set between 5% to 1% , the PWM input frequency should be set below 1KHz . The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 5% range.



## 6.2 The Input Data Format



Signal Name	Description	
R5 R4 R3 R2 R1 R0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
G5 G4 G3 G2 G1 G0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
B5 B4 B3 B2 B1 B0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
RxCLKIN	Data Clock	The signal is used to strobe the pixel data and DE signals. All pixel data shall be valid at the falling edge when the DE signal is high.
DE	Display Timing	This signal is strobed at the falling edge of RxCLKIN. When the signal is high, the pixel data shall be valid to be displayed.
VS	Vertical Sync	The signal is synchronized to RxCLKIN .
HS	Horizontal Sync	The signal is synchronized to RxCLKIN .

Note: Output signals from any system shall be low or High-impedance state when VDD is off.

## 6.3 Integration Interface Requirement

### 6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

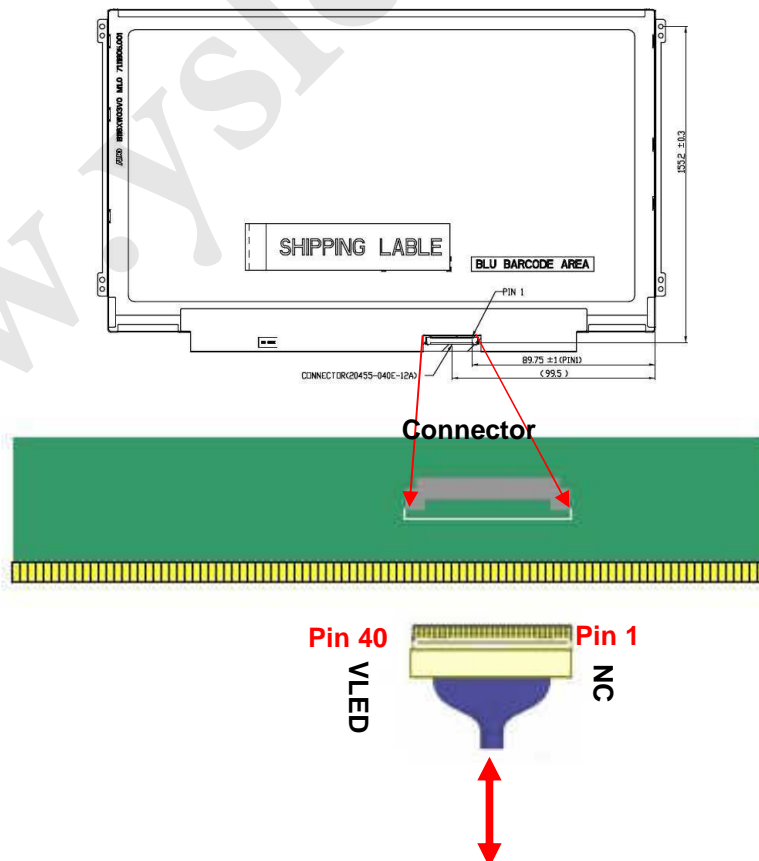
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	STM MSAK24025P40 or compatible
Mating Housing/Part Number	IPEX 20453-040T-11 or compatible

### 6.3.2 Pin Assignment

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	NC	No Connection (Reserve)
2	VDD	Power Supply +3.3V
3	VDD	Power Supply +3.3V
4	VEDID	EDID +3.3V Power
5	NC	No Connect (Reserve)
6	CLK_EDID	EDID Clock Input
7	DAT_EDID	EDID Data Input
8	RxOIN0-	-LVDS Differential Data INPUT(Odd R0-R5,G0)
9	RxOIN0+	+LVDS Differential Data INPUT(Odd R0-R5,G0)
10	VSS	Ground
11	RxOIN1-	-LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
12	RxOIN1+	+LVDS Differential Data INPUT(Odd G1-G5,B0-B1)
13	VSS	Ground
14	RxOIN2-	-LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
15	RxOIN2+	+LVDS Differential Data INPUT(Odd B2-B5,HS,VS,DE)
16	VSS	Ground
17	RxOCKIN-	-LVDS Odd Differential Clock INPUT
18	RxOCKIN+	-LVDS Odd Differential Clock INPUT
19	NC	Color Matrix Enable (3.0V~3.6V, 3.3V type)
20	NC	No connection
21	NC	No connection
22	NC	No connection

23	NC	No connection
24	NC	No connection
25	NC	No connection
26	NC	No connection
27	NC	No connection
28	NC	No connection
29	NC	No connection
30	NC	No connection
31	VLED_GND	LED Ground
32	VLED_GND	LED Ground
33	VLED_GND	LED Ground
34	NC	No Connection (Reserve)
35	VPWM_EN	PWM logic input level
36	VLED_EN	LED enable input level
37	NC	No connection (Disable)
38	VLED	LED Power Supply
39	VLED	LED Power Supply
40	VLED	LED Power Supply



Note1: Input signals shall be low or High-impedance state when VDD is off.

## 6.4 Interface Timing

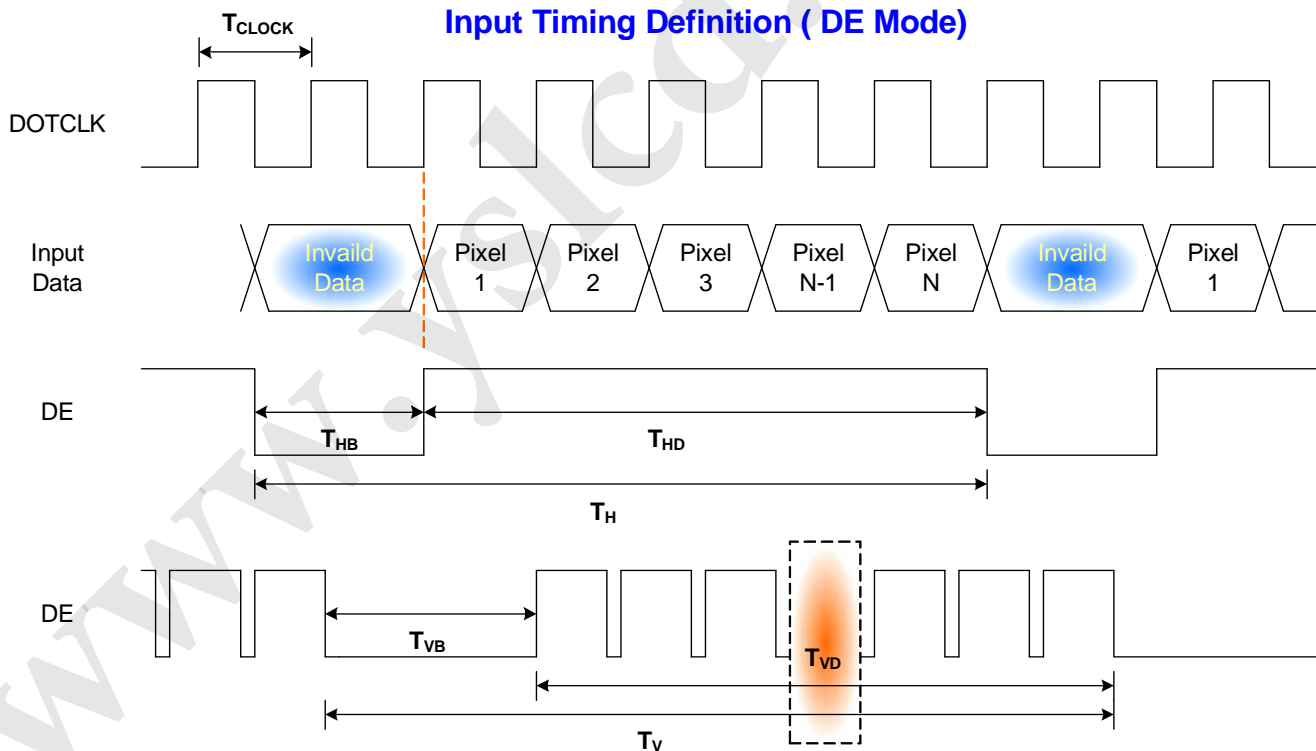
### 6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T <sub>Clock</sub>	66.4	69.3	80	MHz
Vertical Section	Period	T <sub>V</sub>	776	793	1000	T <sub>Line</sub>
	Active	T <sub>VD</sub>	768			
	Blanking	T <sub>VB</sub>	8	25	180	
Horizontal Section	Period	T <sub>H</sub>	1426	1456	2000	T <sub>Clock</sub>
	Active	T <sub>HD</sub>	1366			
	Blanking	T <sub>HB</sub>	60	90	634	

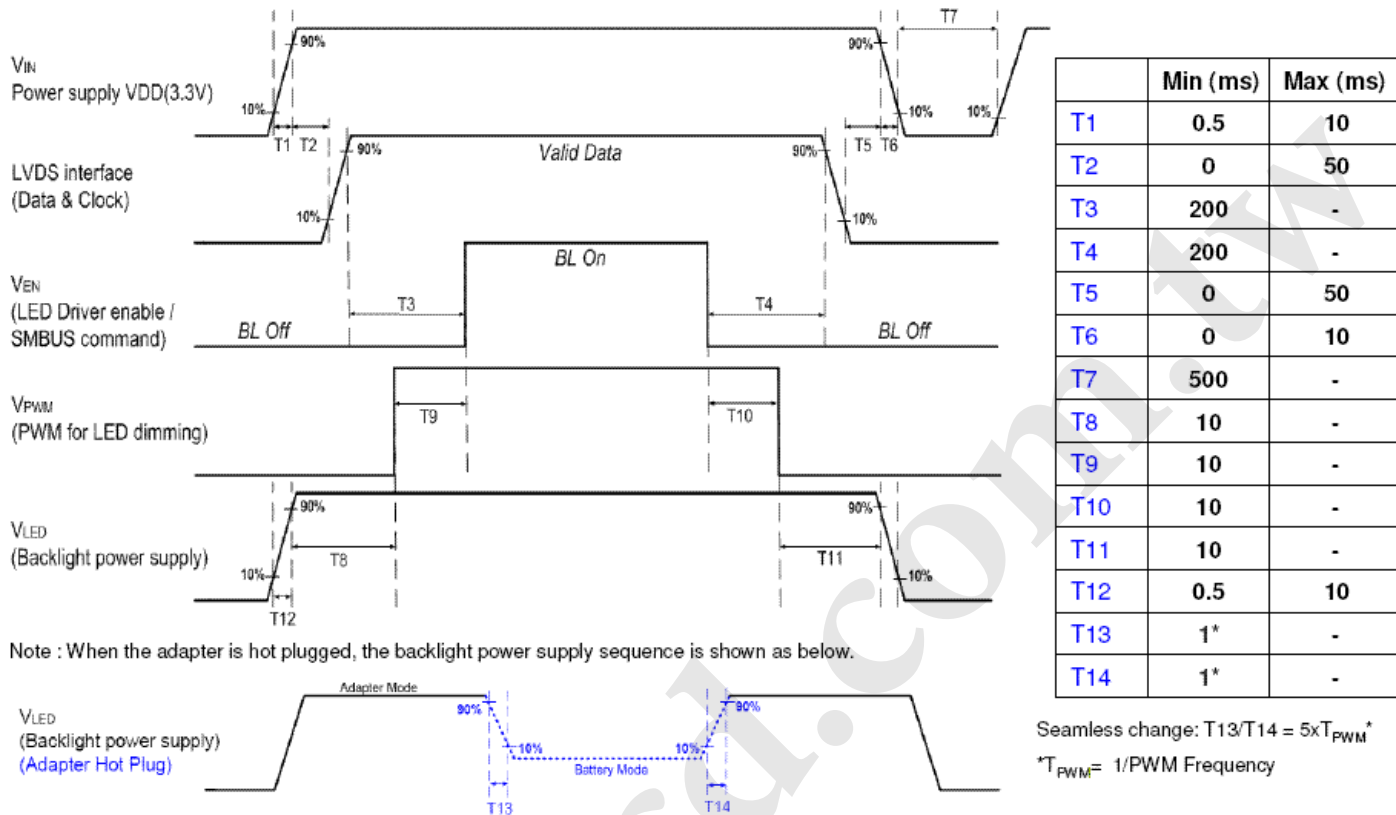
### 6.4.2 Timing diagram

#### Input Timing Definition (DE Mode)



## 6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off



Note 1 : If  $T3 < 200\text{ms}$ , the display garbage may occur. ( $T3 > 200\text{ms}$  is recommended)

Note 2 : If  $T1$  or  $T12 < 0.5\text{ms}$ , the inrush current may cause the damage of fuse. If  $T1$  or  $T12 < 0.5\text{ms}$ , the inrush current  $I^2t$  is under typical melt of fuse Spec, there is no mentioned problem.

## 7. Panel Reliability Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C , 90%RH, 300h	
High Temperature Operation	Ta= 50°C , Dry, 300h	
Low Temperature Operation	Ta= 0°C , 300h	
High Temperature Storage	Ta= 60°C , 35%RH, 300h	
Low Temperature Storage	Ta= -20°C , 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C , Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost  
 . Self-recoverable. No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

## 8.1 LCM Outline Dimension



Note: Prevention IC data

## 9. Shipping and Package

### 9.1 Shipping Label Format

[Z40]

 *XXXXXXXXXXXXX.XXXXXX	Manufactured MM/WW Model No: <b>B116XTN04.0</b> AU Optronics Made in China (Z40) H/W: <b>0A</b> F/W: 1	   
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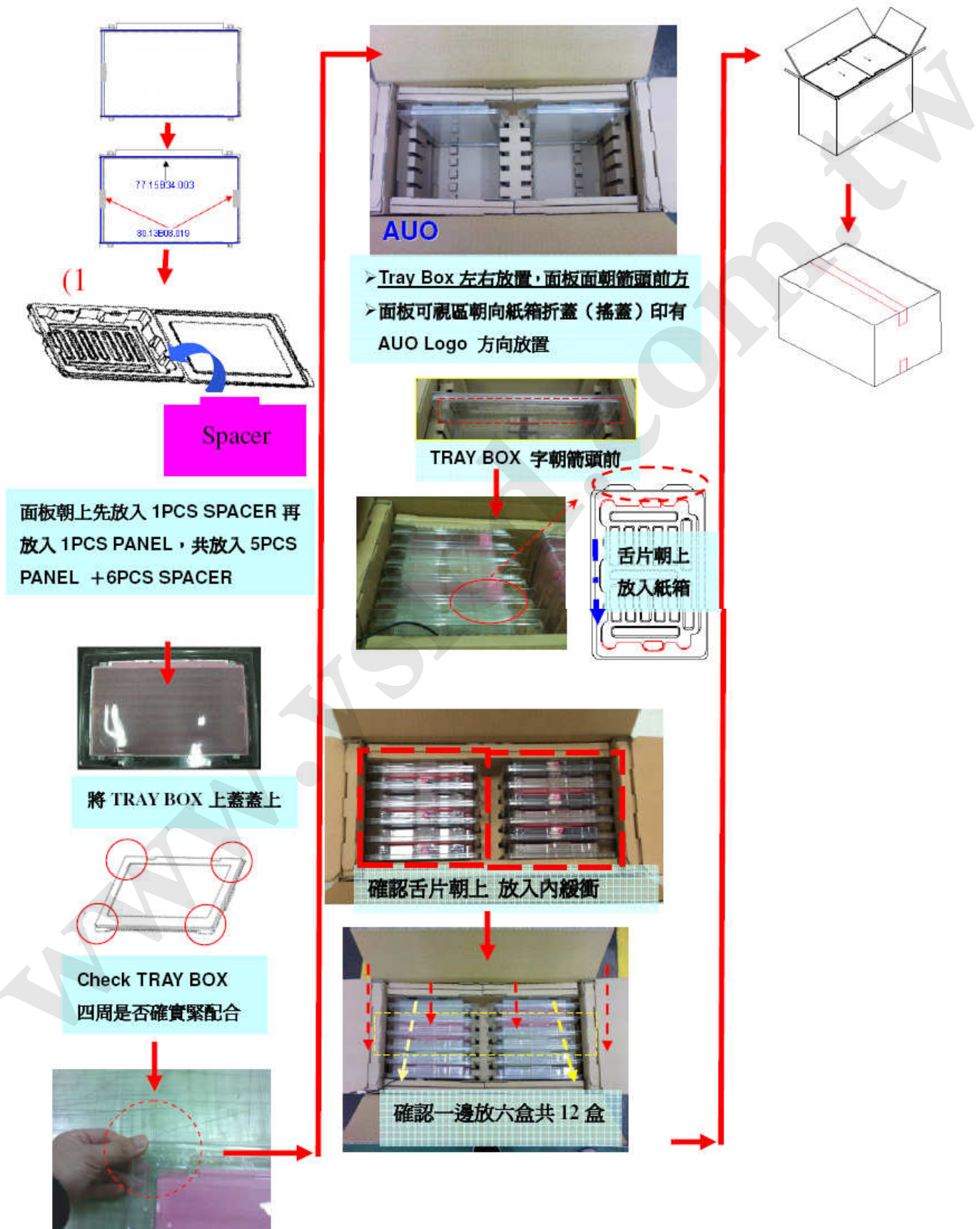
[Z30]

 *XXXXXXXXXXXXX.XXXXXX	Manufactured MM/WW Model No: <b>B116XTN04.0</b> AU Optronics Made in China (Z30) H/W: <b>0A</b> F/W: 1	   
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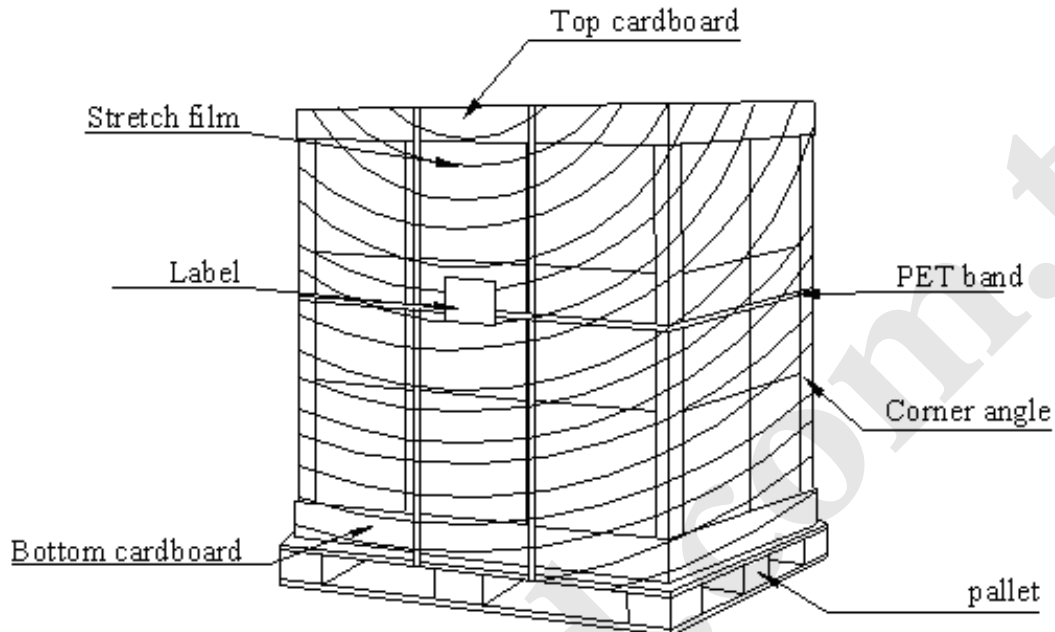
Note: Z40/Z30 is different from Module MFG

## 9.2 Carton Package

The outside dimension of carton is 553(L)mm\* 275(W)mm\* 379(H)mm



## 9.3 Shipping Package of Palletizing Sequence



## 9.4 Handling guide

This is a thin and slime LCD model, and please be cautious when pulling it out of package or assembling it onto platform. Careless handlings, e.g. twist, bending, pressing, or collision, will result malfunction of LCD models.

### (1) Handling method notice



Do not lift and hold the panel with single hand at right or left side from tray.



Lift and hold the panel up with both hands from tray.

## (2) On the table notice



Do not press edge of panel to avoid glass broken.

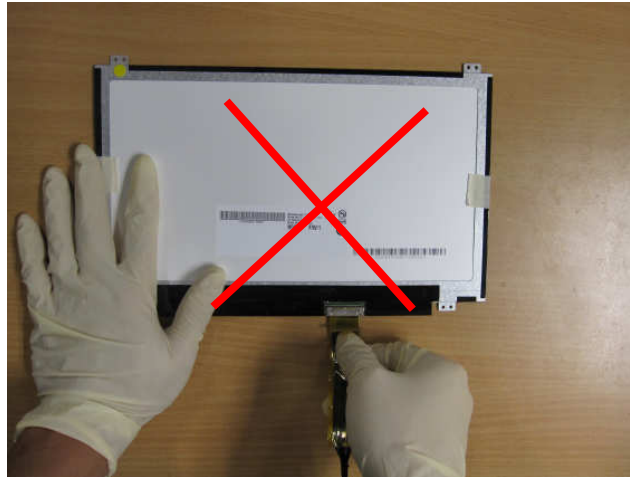


Do not press the surface of the panel to avoid the glass broken or polarizer scratch.

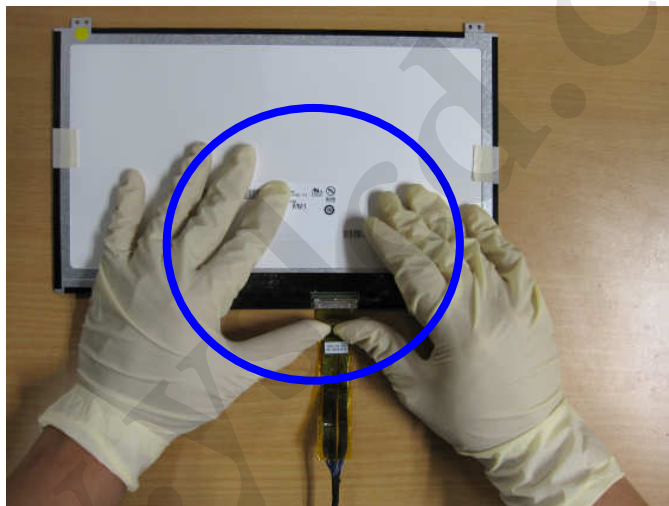


Do not put anything or tool on the panel to avoid the glass broken or polarizer scratch.

## (3) Cable assembly notice



Do not insert the connector with single hand and touching the PCBA.



Insert the connector by pushing right and left edge.

## 10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value	
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	



# Product Specification

AU OPTRONICS CORPORATION

08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	5C	01011100	92	
0B	hex, LSB first	40	01000000	64	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	16	00010110	22	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	<b>Video input def.</b> (digital I/P, non-TMDS, CRGB)	90	10010000	144	
15	<b>Max H image size</b> (rounded to cm)	1A	00011010	26	
16	<b>Max V image size</b> (rounded to cm)	0E	00001110	14	
17	<b>Display Gamma</b> (=gamma*100)-100)	78	01111000	120	
18	<b>Feature support</b> (no DPMS, Active OFF, RGB, tmg Blk#1)	02	00000010	2	
19	Red/green low bits ( <b>Lower 2:2:2:2 bits</b> )	99	10011001	153	
1A	Blue/white low bits ( <b>Lower 2:2:2:2 bits</b> )	85	10000101	133	
1B	Red x ( <b>Upper 8 bits</b> )	95	10010101	149	
1C	Red y/ highER 8 bits	55	01010101	85	
1D	Green x	56	01010110	86	
1E	Green y	92	10010010	146	
1F	Blue x	28	00101000	40	
20	Blue y	22	00100010	34	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	



# Product Specification

AU OPTRONICS CORPORATION

32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	12	00010010	18	
37	Pixel Clock/10000 USB	1B	00011011	27	
38	Horz active <b>Lower 8bits</b>	56	01010110	86	
39	Horz blanking <b>Lower 8bits</b>	5A	01011010	90	
3A	HorzAct:HorzBlnk <b>Upper 4:4 bits</b>	50	01010000	80	
3B	Vertical Active <b>Lower 8bits</b>	00	00000000	0	
3C	Vertical Blanking <b>Lower 8bits</b>	19	00011001	25	
3D	Vert Act : Vertical Blanking <b>(upper 4:4 bit)</b>	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	36	00110110	54	
41	Horz&Vert Sync Offset/Width <b>Upper 2bits</b>	00	00000000	0	
42	Horizontal Image Size <b>Lower 8bits</b>	00	00000000	0	
43	Vertical Image Size <b>Lower 8bits</b>	90	10010000	144	
44	Horizontal & Vertical Image Size <b>(upper 4:4 bits)</b>	10	00010000	16	
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0	
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0	
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	



# Product Specification

AU OPTRONICS CORPORATION

5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	
60	Manufacture	55	01010101	85	
61	Manufacture	4F	01001111	79	
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	
72	Manufacture P/N	31	00110001	49	
73	Manufacture P/N	31	00110001	49	
74	Manufacture P/N	36	00110110	54	
75	Manufacture P/N	58	01011000	88	
76	Manufacture P/N	54	01010100	84	
77	Manufacture P/N	4E	01001110	78	
78	Manufacture P/N	30	00110000	48	
79	Manufacture P/N	34	00110100	52	
7A	Manufacture P/N	2E	00101110	46	
7B	Manufacture P/N	30	00110000	48	
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	CC	11001100	204	