1K-BIT SERIAL EEPROM WITH MICROWIRE INTEFACE

(compatible to CAT93C46 Catalyst)

DESCRIPTION

The IN93LC46 is a Electric erasable programmable ROM (EEPROM) memory data capacity 1K (128x8 or 64x16) with 3-wire interface.
There are 3 modification of ICs
A: ICs IN93AA(LC)46AD/AN are 8 bits registers (128x8) - ORG pin is not used
B: ICs IN93AA(LC)46BD/BN are 16 bits registers (64x16) - ORG pin is not used
C: ICs IN93AA(LC)46CN/CD are configured as either registers of 8 bits (ORG pin at GND) or 16 bits (ORG pin at V_{CC}, or not connected). Each register can be written (or read) serially by using the DI (or DO) pin.
The ICs is purposed for reading, writing & nonvolatile data storage in electronic units with 3-wire interface. ICs can be used in TV-sets, telecom equipment & consumer electronic devices.

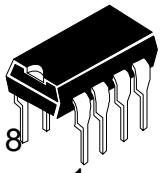
FEATURES

- 100 year 1K data retention for Ta=25°C;
- Build-in voltage multiplier;
- Serial I/O bus;
- Autoincrement of word address;
- Self-timed write cycle with auto-clear;
- 1,000,000 program/erase cycles;
- Power-up internal logic setup;
- Read cycles quantity are not limited;

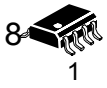
- Supply voltage range , U_{CC}

for IN93LC46N/D 2,5 …5,5 V;
for IN93AA46N/D 1,8 …5,5 V;

- Low power consumption;
- Operating temperature range -40 … +85 °C.



N SUFFIX
DIP



D SUFFIX
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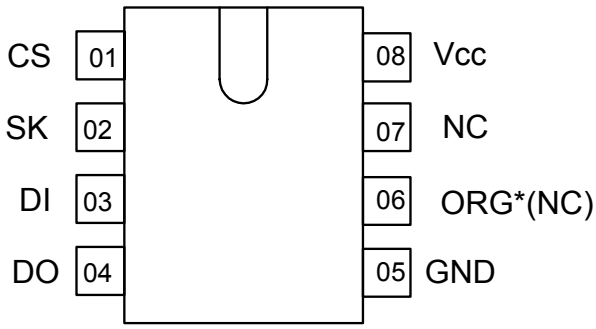
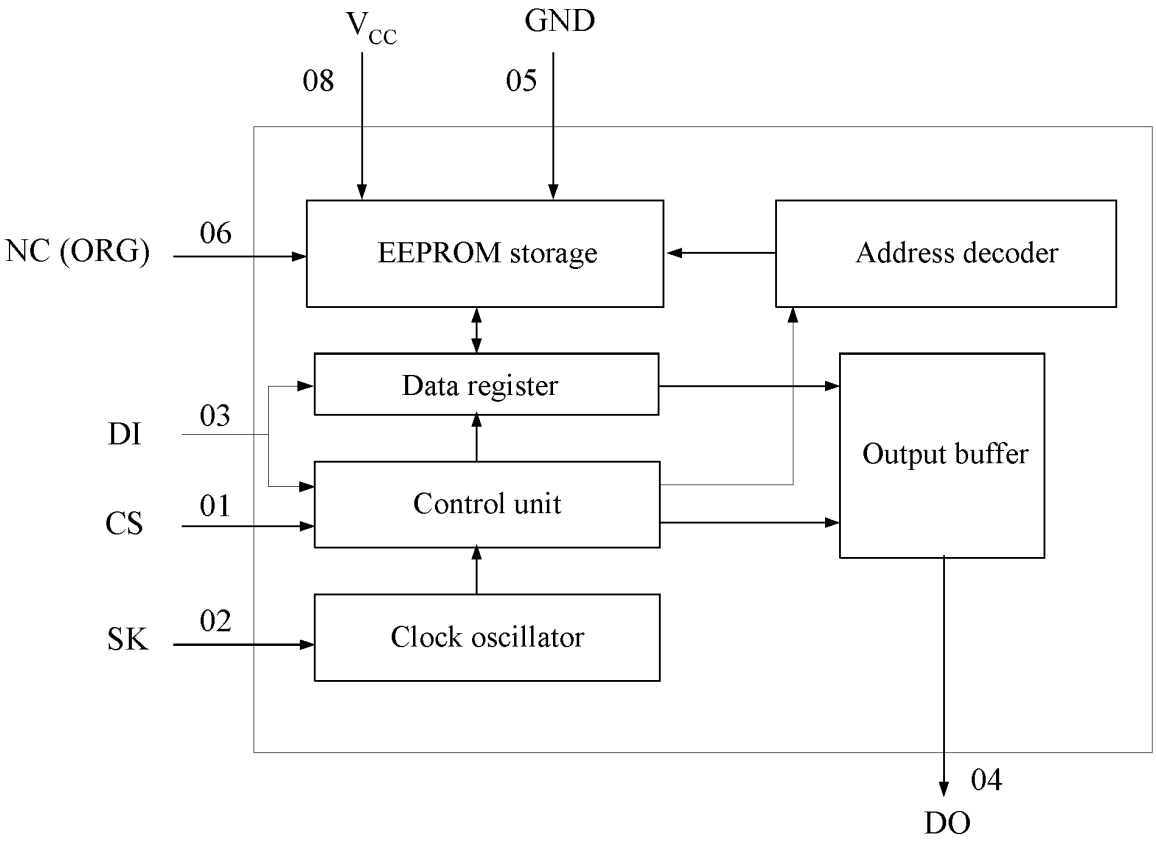
PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+1.8 to 6.0V Power Supply
GND	Ground
ORG*	Memory Organization pin *
NC	No Connection



Note
* this pin is present only in IN93AA46CN, IN93AA46CD:
When the ORG pin is connected to V_{CC}, the x16 organization is selected.
When it is connected to ground, the x8 pin is selected.
If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

Block Diagram



Recommended Operation Conditions & Maximum Ratings*

Parameter, unit		Symbol	Recommended Operation Conditions		Maximum Ratings	
			Min	Max	Min	Max
Supply voltage,V	IN93LC46AN, IN93LC46AD, IN93LC46BN, IN93LC46BD, IN93LC46CN, IN93LC46CD	Ucc	2,5	6,0	- 2,0	7,0
	IN93AA46AN, IN93AA46AD, IN93AA46BN, IN93AA46BD, IN93AA46CN, IN93AA46CD		1,8	6,0		
High level input voltage, V	4,5 V ≤ Ucc ≤ 5,5 V	U_{IH} [1)]	2,0	Ucc + 0,5	–	Ucc + 2,0
	1,8 V ≤ Ucc < 4,5 V		0,7Ucc	Ucc + 0,5		
Low level input voltage, V	4,5 V ≤ Ucc ≤ 5,5 V	U_{IL} [2)]	-0,1	0,8	- 2,0	–
	1,8 V ≤ Ucc < 4,5 V		0	0,2Ucc		
Low level output current мА		I_{OL}	–	2,1	–	–
Output short-circuit current, mA		I_{OS} [3)]	–	–	–	100

[1)] The maximum constant voltage is Ucc+0,5B. While operation pulses up to U_{CC}+2V can be applied to inputs, pulse duration have to be less than 20 nanoseconds. The maximal constant input voltage is Ucc+0,5B. While operation positive pulses up to Ucc +2V can be applied to inputs, pulse duration have to be less than 20 nanoseconds.

[2)] The minimal constant voltage is -0,5B. While operation negative pulses up to-2V can be applied to inputs, pulse duration have to be less than 20 nanoseconds. The maximal constant input voltage is Ucc+0,5B. While operation positive pulses up to Ucc +2V can be applied to inputs, pulse duration have to be less than 20 nanoseconds.

[3)] Time no more than 1 sec

Electric Parameters

(IN93AA46N/D U_{CC} = 1,8 V – 6,0 V;
IN93LC46N/D U_{CC} = 2,5 V – 6,0 V)

Parameter, unit	Symbol	Mode	Min	Max	T_A, °C
Low level output voltage, V	U_{OL1}	4,5 V ≤ U_{CC} ≤ 5,5 V I_{OL} = 2,1 mA	–	0,4	25 ± 10; -45; 85
High level output voltage, V	U_{OH1}	4,5 V ≤ U_{CC} ≤ 5,5 V I_{OH} = -400 uA	2,4	–	
Low level output voltage, V	U_{OL2}	1,8 V ≤ U_{CC} < 4,5 V I_{OL} = 1 mA	–	0,2	
High level output voltage, V	U_{OH2}	1,8 V ≤ U_{CC} < 4,5 V I_{OH} = -100 uA	U_{CC}-0,2	–	
Low level input leakage current, uA	I_{ILL}	U_I = 0 V 1,8 V ≤ U_{CC} ≤ 6,0 V	–	-1,0	
High level input leakage current, uA	I_{ILH}	U_I = Ucc 1,8 V ≤ U_{CC} ≤ 6,0 V	–	1,0	
Low level output leakage current, uA	I_{OLL}	U_O = 0 V U_{IL} = 0 V 1,8 V ≤ U_{CC} ≤ 6,0 V	–	-1,0	
High level output leakage current, uA	I_{OLH}	U_O = Ucc U_{IL} = 0 V 1,8 V ≤ U_{CC} ≤ 6,0 V	–	1,0	
Consumption current (8-bit mode), uA	I_{CC1}	Ucc = 5,5 V U_{IL} = 0 V U_{ORG} = 0 V or ORG not connected	–	10	
Consumption current (16-bit mode), nA	I_{CC2}	Ucc = 5,5 V U_{IL} = 0 V U_{IH} = Ucc U_{ORG} = Ucc	–	900	
Consumption current (Operating Read), uA	$I_{OCC\ R}$	Ucc = 5,0 V f_C = 1 MHz	–	500	
Consumption current (Operating Write/Erase), uA	$I_{OCC\ E/W}$	Ucc = 5,0 V f_C = 1 MHz	–	3,0	
Output Delay to Low, ns	t_{PD0}	U_{CC} = 4,5 V f_C = 1 MHz	–	250	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	500	
		U_{CC} = 1,8 V f_C = 0,25 MHz	–	1000	
Output Delay to High, ns	t_{PD1}	U_{CC} = 4,5 V f_C = 1 MHz	–	250	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	500	
		U_{CC} = 1,8 V f_C = 0,25 MHz	–	1000	

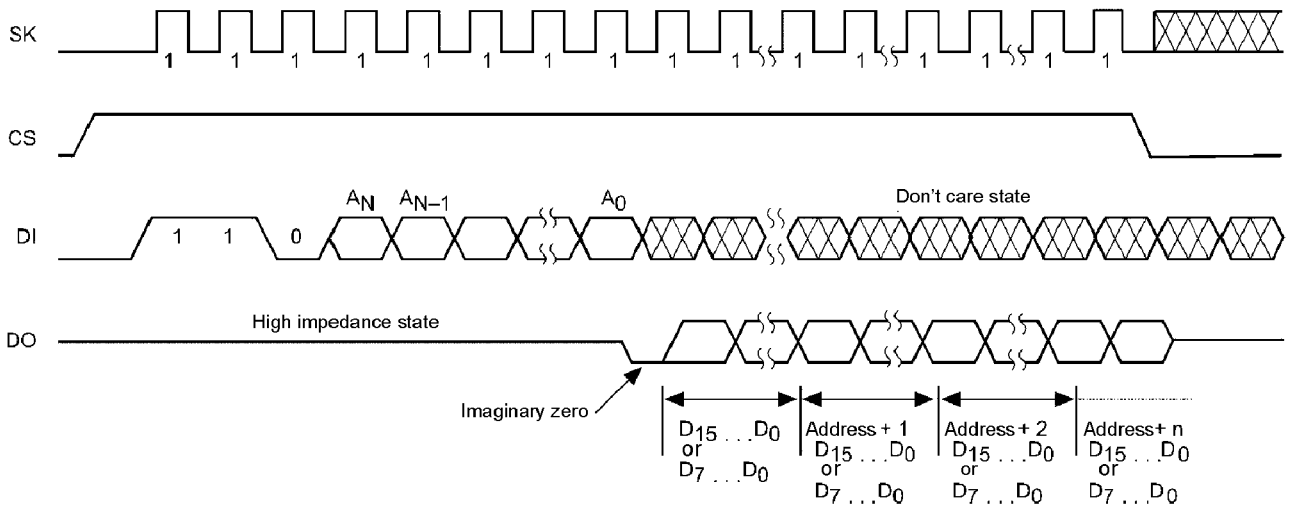
Parameter, unit	Symbol	Mode	Min	Max	T_A, °C
Output Delay to High-Z, ns	t_{HZ}	U_{CC} = 4,5 V f_C = 1 MHz	–	100	25 ± 10; -40; 85
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	200	
		U_{CC} = 1,8 V f_C = 0,25 MHz	–	400	
Write/Erase cycle, ms	t_{CY}	U_{CC} = 4,5 V f_C = 1 MHz	–	10	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	10	
		U_{CC} = 1,8 V f_C = 0,25 MHz	–	10	
Output Delay to Status Check, ns	t_{SV}	U_{CC} = 4,5 V f_C = 1 MHz	–	250	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	500	
		U_{CC} = 1,8 V f_C = 0,25 MHz	–	1000	
Power-up to Read Operation Time, ms	t_{PUR}	U_{CC} = 4,5 V f_C = 1 MHz	–	1,0	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	1,0	
		U_{CC} = 1,8 V f_C = 0,25 MHz	–	1,0	
Power-up to Wtite Operation Time, ms	t_{PUW}	U_{CC} = 4,5 V f_C = 1 MHz	–	1,0	
		U_{CC} = 2,5 V f_C = 0,5 MHz	–	1,0	
		U_{CC} = 1,8 V f_C = 0,25 MHz	–	1,0	
Program/erase cycles	$N_{E/W}$	Ucc = 5,0 V	1000000	–	25 ± 10
Note t_{PUR} & t_{PUW} times are delays from of power up to operation started					

3-wire Interface Parameters (-40 °C ≤ T_A ≤ 85 °C)

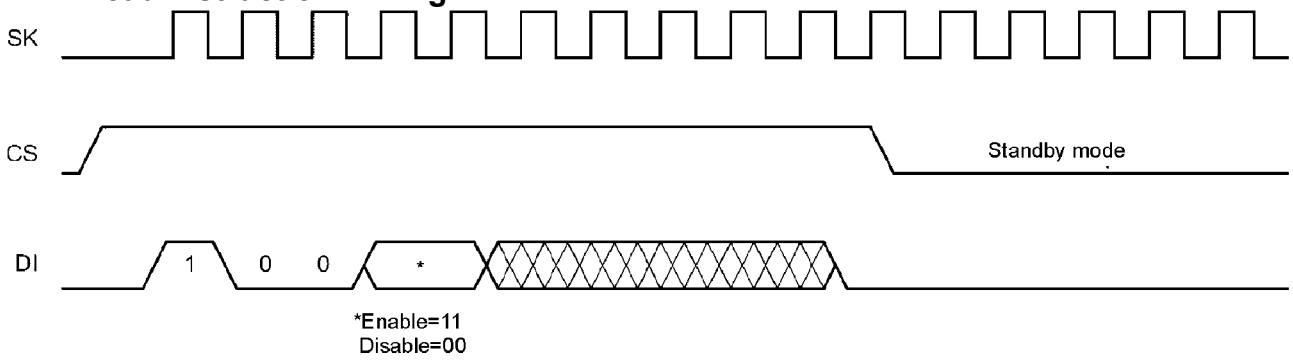
Parameter, unit	Symbol	Mode						
			1,8V≤U_{CC}≤6,0V		2,5V≤U_{CC}≤6,0V		4,5V≤U_{CC}≤6,0V	
			Min	Max	Min	Max	Min	Max
Clock frequency, MHz	f_C	C_L=100 pF	-	0,25	-	0,5	-	2
CS Setup Time, ns	t_{CSS}		200	-	100	-	50	-
CS Hold Time, ns	t_{CSH}		0	-	0	-	0	-
DI Setup Time, ns	t_{DIS}		400	-	200	-	100	-
DI Hold Time, ns	t_{DIH}		400	-	200	-	100	-
Minimum CS Low Time, ns	$t_{CS\ MIN}$		1000	-	500	-	250	-
Minimum SK High Time, ns	t_{SKHI}		1000	-	500	-	250	-
Minimum SK Low Time, ns	t_{SKLOW}		1000	-	500	-	250	-

Instruction Set

Instruction	Start Bit	Op-code	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6-A0	A5-A0			Read Address AN- AO
ERASE	1	11	A6-A0	A5-A0			Clear Address AN- AO
WRITE	1	01	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN- AO
EWEN	1	00	11XXXXX	11XXXX			Write Enable
EWDS	1	00	00XXXXX	00XXXX			Write Disable
ERAL	1	00	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	00	01XXXXX	01XXXX	D7-DO	D15-D0	Write All Addresses

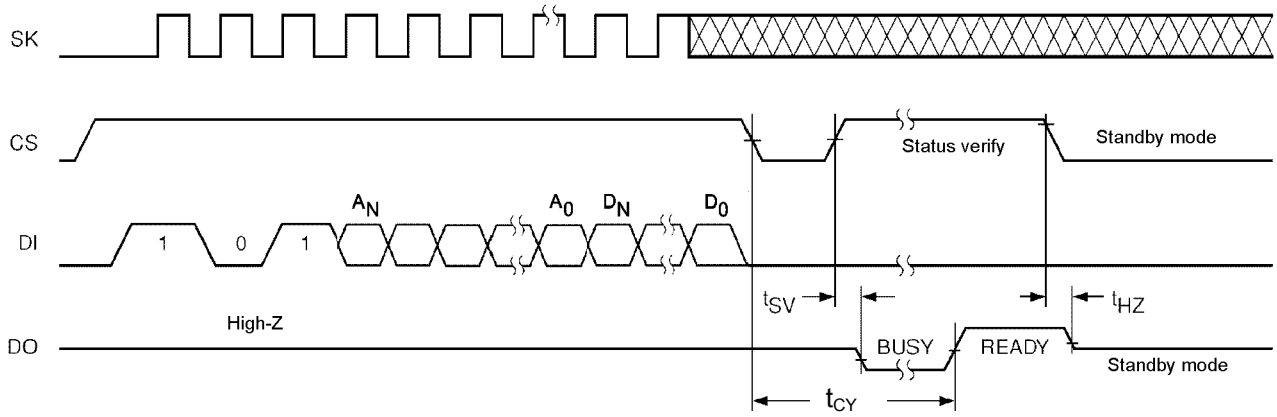


Read Instruction Timing



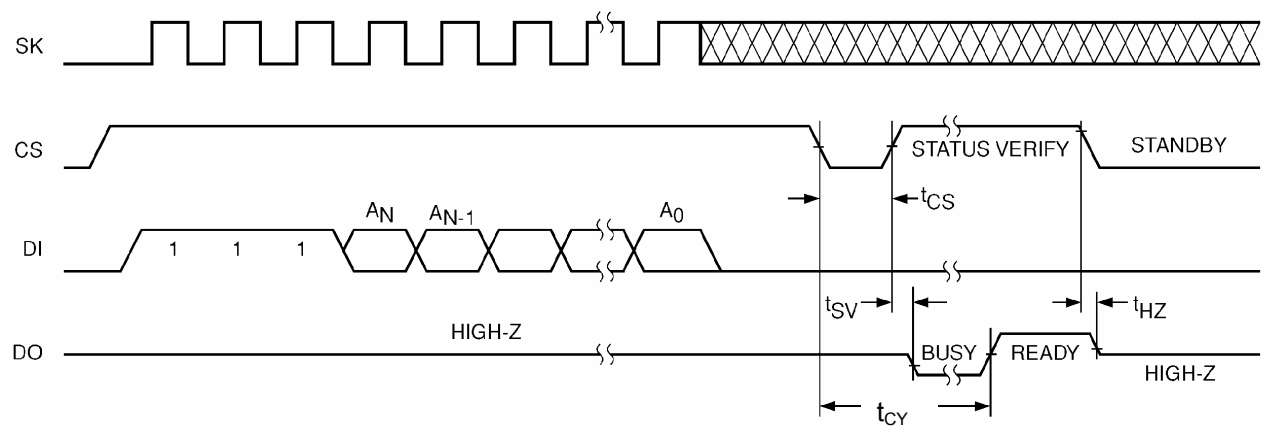
EWEN/EWDS Instruction Timing

The IN93AA46/IN93LC46 powers up switch IC to the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction.



ERAL Instruction Timing

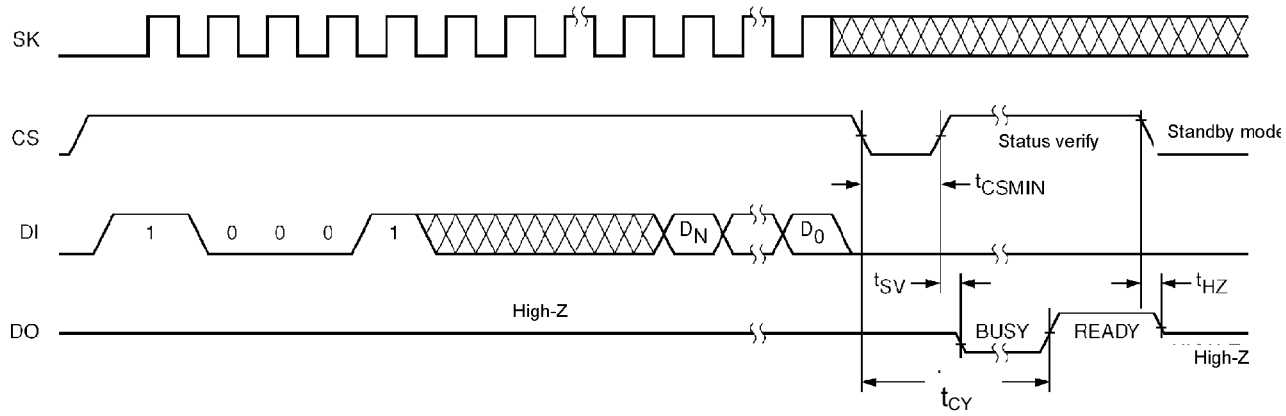
The IN93AA46/IN93LC46 ignore all external signals applied to SK and DI pins during cycle of active programming. Erase/write cycle duration (t_{CY}) can be measured (controlled) by scanning of IC output. Low level (logical “0”) means that programming still in progress, high level (logical “1”) means that programming is already completed. Transition of output to High-Z state after programming cycle was completed is executed by applying low level (logic “0”) to CS pin or applying high level (logical “1”) to DI pin (for case CS = 1).



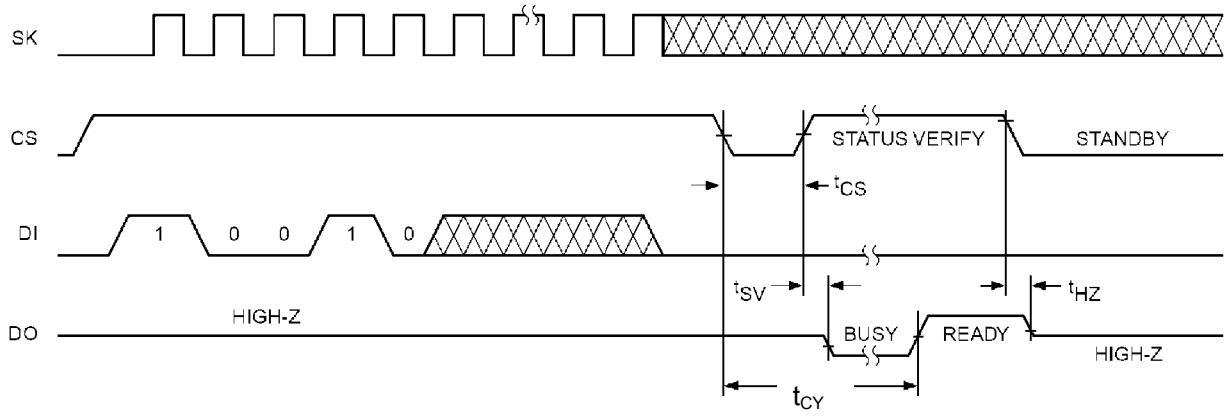
ERASE Instruction Timing

Once cleared, the content of a cleared location returns to a logical “1” state.

t_{CY}

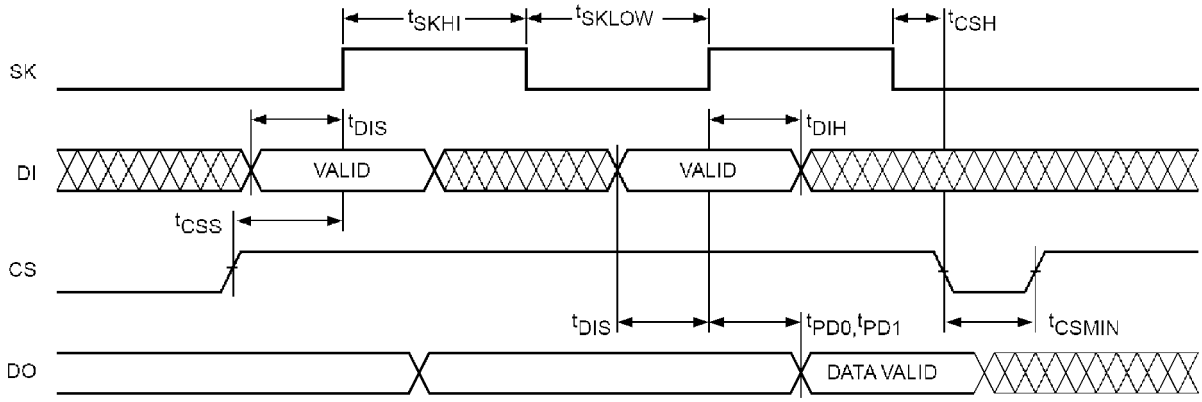


WRAL Instruction Timing



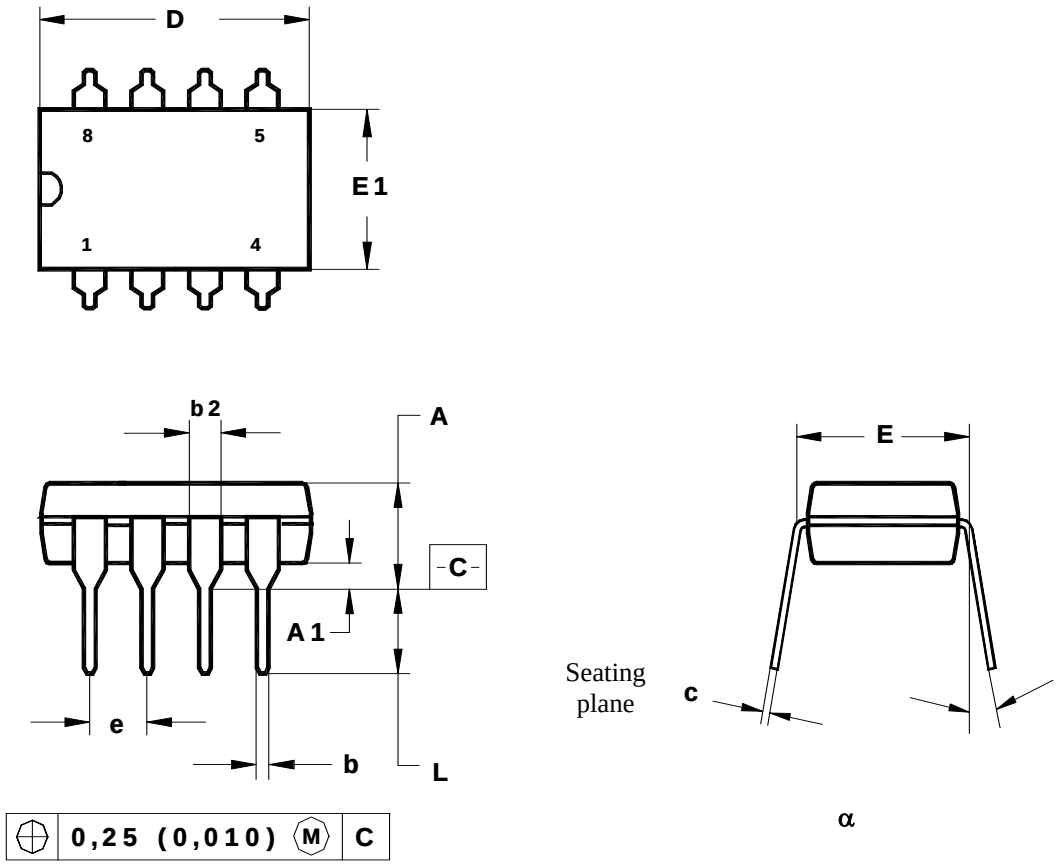
Once cleared, the contents of all memory bits return to a logical “1” state.

ERAL Instruction Timing



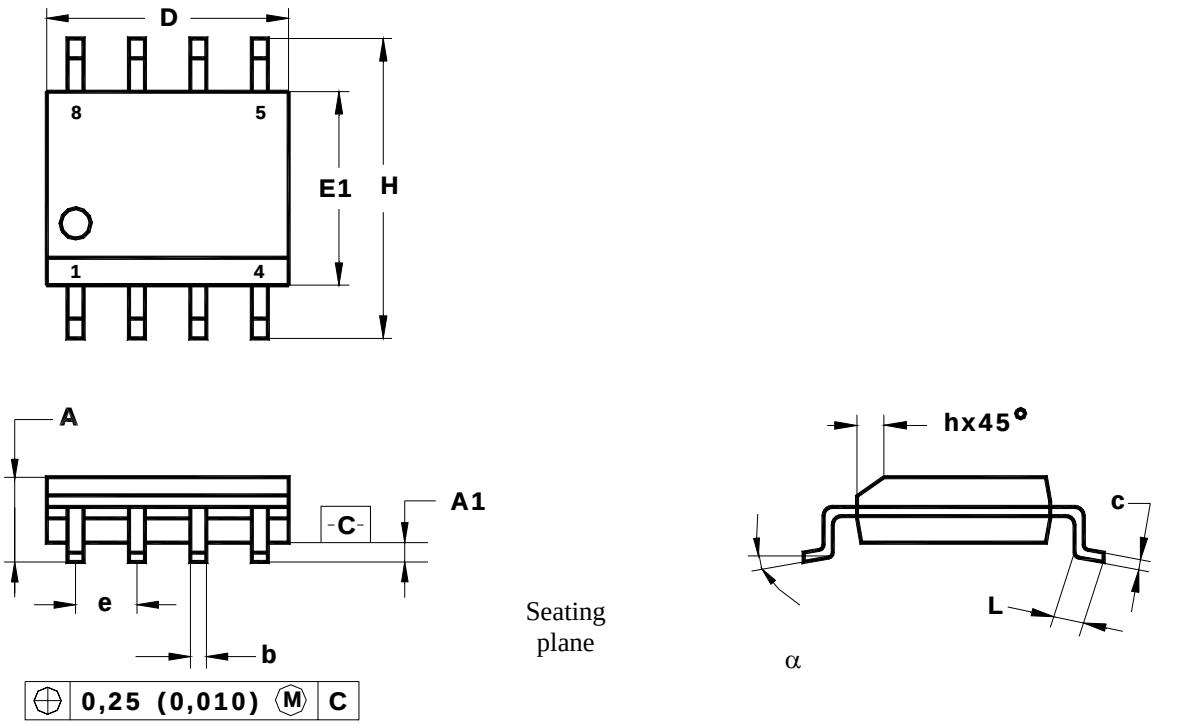
Sychronous Data Timing

N SUFFIX PLASTIC DIP
(MS-001BA)



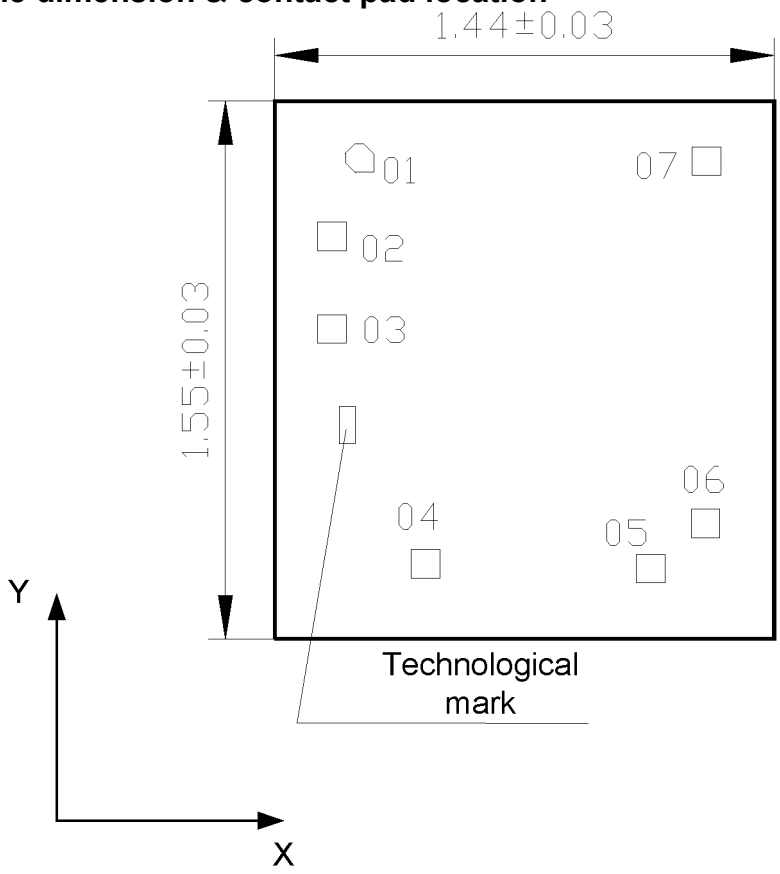
	D	E1	A	b	b2	e	α	L	E	c	A1
mm											
min	9.02	6.07	—	0.36	1.14		0°	2.93	7.62	0.20	0.38
max	10.16	7.11	5.33	0.56	1.78	2.54	15°	3.81	8.26	0.36	—
inches											
min	0.355	0.240	—	0.014	0.045		0°	0.115	0.300	0.008	0.015
max	0.400	0.280	0.210	0.022	0.070	0.1	15°	0.150	0.325	0.014	—

D SUFFIX PLASTIC SOP
(MS-012AA)



	D	E1	H	b	e	α	A	A1	c	L	h
mm											
min	4.80	3.80	5.80	0.33		0°	1.35	0.10	0.19	0.41	0.25
max	5.00	4.00	6.20	0.51	1.27	8°	1.75	0.25	0.25	1.27	0.50
inches											
min	0.1890	0.1497	0.2284	0.013		0°	0.0532	0.0040	0.0075	0.016	0.0099
max	0.1968	0.1574	0.2440	0.020	0.100	8°	0.0688	0.0090	0.0098	0.050	0.0196

Die dimension & contact pad location



Technology mark coordinates, mm: left bottom corner x = 0,15, y =0,655.

Die thickness 0,46±0,02 mm.

Pad location table

Pad number	Coordinates (left bottom corner), mm		Contact pad description
	X	Y	
01	0,2026	1,3386	CS
02	0,1241	1,1189	SK
03	0,1241	0,8524	DI
04	0,3938	0,1753	DO
05	1,0430	0,1620	GND
06	1,2006	0,2911	NC (ORG*)
07	1,2040	1,3360	V_{CC}

Note contact pad coordinates are indicated according passivation layer

* For ICs IN93LC46CN/CD, IN93AA46CN/CD