SPECIFICATION
FOR
APPROVAL

( ) Preliminary Specification
(●) Final Specification

Title	TFT-LCD Timing Controller

BUYER	
MODEL	FORT_REV(HS503022)

SUPPLIER	LG.Philips LCD Co., Ltd.
MODEL	FORT_REV(HS503022)
LG Part Number	0IHYL-0047A

SIGNATURE	DATE
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Please return 1 copy for your confirmation with your signature and comments.

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TFT-LCD Timing Controller

P/N : 0IHYL-0047A

Contents

Record of Revisions

Rev. No.	Rev. Date	Page	Description
1.0	Aug. 20. 2003	-	First Draft (Preliminary)
1.1	Sep. 24. 2003	-	
1.1		22 ~ 24	18. Application Circuit [Correction]
		25 ~ 30	19. Application Notes [Correction]

1. General description

FORT_REV IC, which is developed by LG.Philips LCD, is timing controller controlling 6.5" wide TFT-LCD module. It is improved LG first ASIC version FORT(0IHYL-0043A).

2. Function

It uses 23.9MHz input clock, and creates the divide signal for comparing PLL phase.

1) Outside of Controller IC, it is composed PLL circuit with additional VCO, LPF, pulls the sync signal of PAL, NTSC into CSY pin and it is used for creating MCLK by PDP signal with DIV signal which is created inside of IC.
2) It creates signal for driving Source drive IC, Gate drive IC by using Horizontal Sync 'HSY', Vertical Sync 'VSY', input signal.
   (1) The signal for Source Drive IC : SSPL, SSPR, LRO, SOE, SSC, SAM
   (2) The signal for Gate Drive IC : UDO, GSP, GSC
   (3) The signal for driving VCOM : FRP or VCAC
      *.When you design the amplification circuit of VCOM, you should be care.
         In case of Non-Inverting amplification,use FRP.
         In case of Inverting amplification,use VCAC.
   (4) The signal for controlling polarity change of display : FRP
3) MODE1, MODE2, MODE3 is for selecting of display mode.
4) It is for controlling the reverse of signal, left/right, up/down by using LRS, UDS.
5) Simultaneously, Successive Data Sampling is possible by controlling PSAM.
6) It is shown the start of Horizontal Line over ODD, EVEN input signal by STRN controlling.
7) It can be changed a position of horizontal Start Pulse by SSP_S1, SSP_S2.
8) It can be changed the vertical Start Pulse as 1H by GSP_S.
9) At NTSC Vertical wide mode 2nd GSC controlled by GSS_S.
10) Use input signal N_P it can be controlled NTSC PAL Mode.
    If you set NTSC/PAL auto detection selection ATMN "H" it operates internal detection signal. If ATMN "L" NTSC/PAL selected by N_P input Signal.

3. Feature

(1) Process : CMOS(0.35㎛)

(2) Package : TQFP: 48pin, Height: 1.0㎜, Pitch: 0.5㎜

4. Pin Diagram

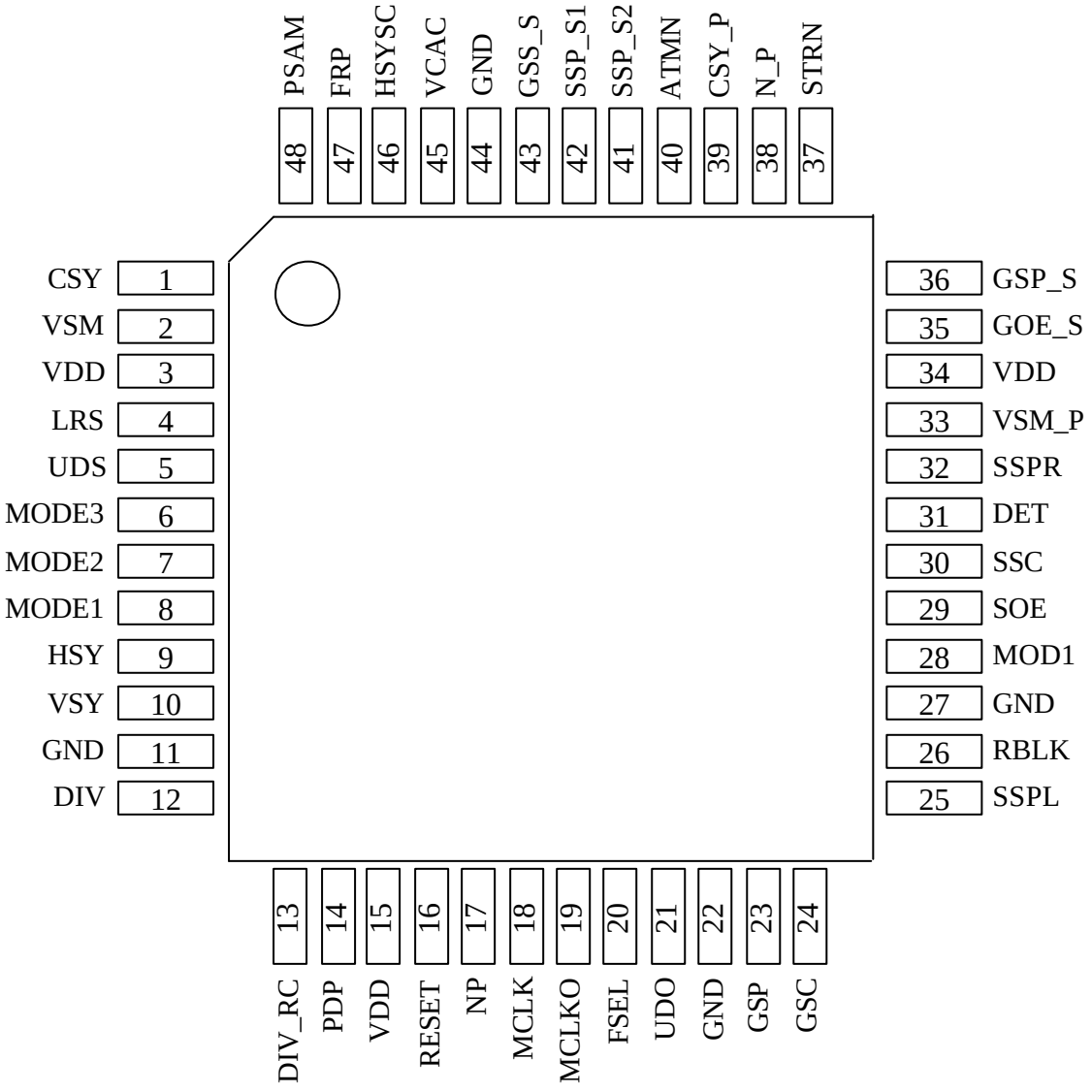


Fig. 1 Pin Diagram

5. Block Diagram

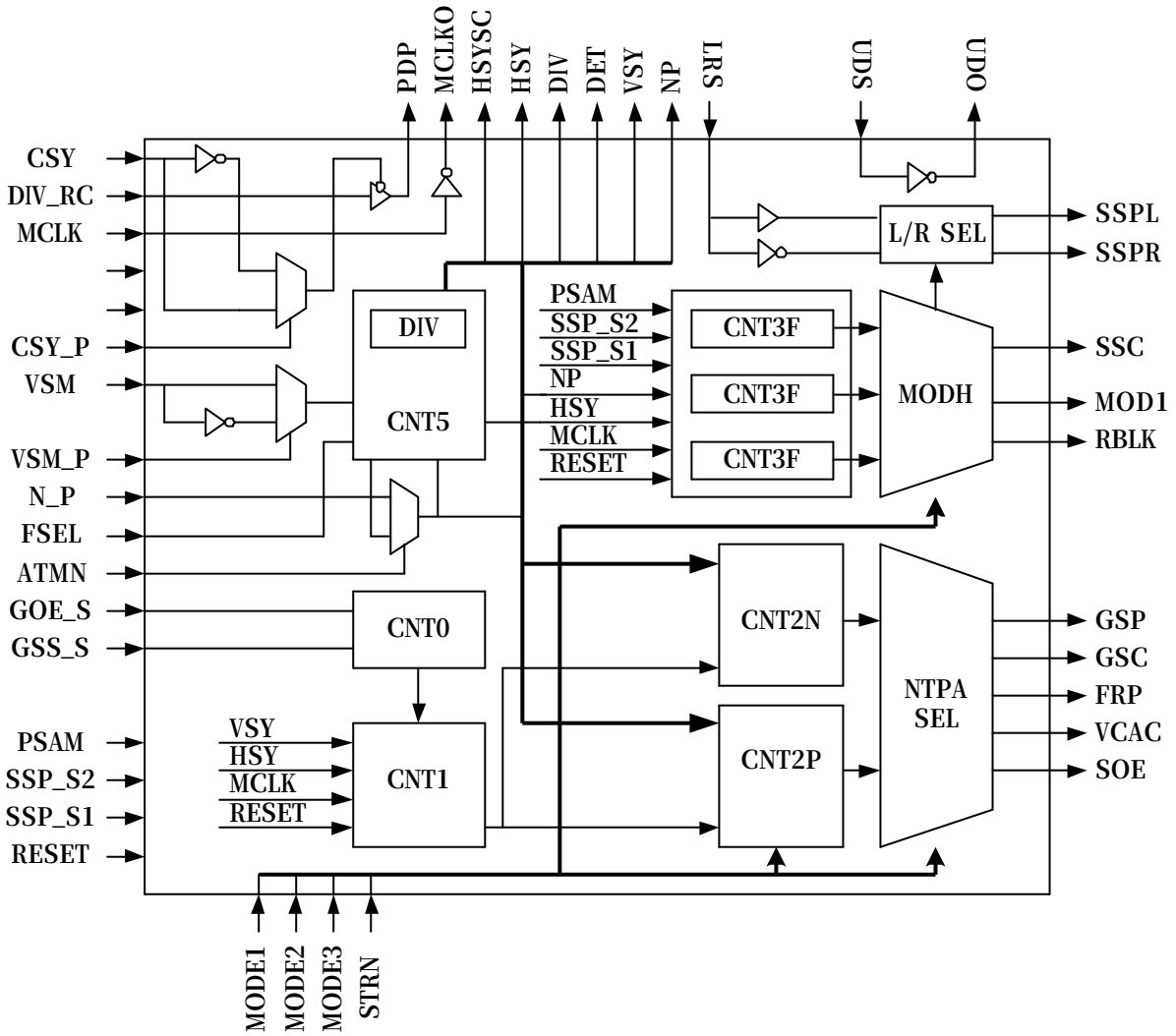


Fig. 2 Block Diagram

6. Main function description

It makes control signals which are needed at external input signal MCLK that is from external PLL Block.

CNT0 : set up the timing of output internal signal(FSC,BSC) which is based on Hsync.
which is controlled of GOE_S, GSS_S. it is based on 'H', 'L' setting.

CNT1 : Set up the timing "FSC, BSC" as taking the signal value which is set up at CNT0(FSC_R, BSC_R, FSC_F, BSC_F) and set up Vertical Reset signal "VSR, VSR2".

CNT2N : Block of setting the vertical control signal when input NTSC signal.
Set up the Vertical control signal by taking MODE1,2,3, STRN, GSP_S signal from outside ,FSC_IN,BSC_IN from CNT1 .

CNT2P : Block of setting the vertical control signal when input PAL signal.
Set up the Vertical control signal by taking MODE1,2,3, STRN, GSP_S signal from outside and FSC_IN from CNT1.

CNT3N : Set up Source Start Pulse(SSP) and Source Sampling Clock(SSC) of Normal mode by taking HSY from CNT 5 Block.

CNT3F : Set up Source Start Pulse(SSP) and Source Sampling Clock(SSC) of Full mode by taking HSY from CNT 5 Block.

CNT3C : Set up Source Start Pulse(SSP) and Source Sampling Clock(SSC) of wide mode by taking HSY from CNT 5 Block.

NTPASEL : Choose Vertical Control Signal of NTSC/PAL Mode

MODH : Choose Horizontal Control Signal of each MODE

CNT5 : Set up the output signal to meet the synchronous of PLL.
The block of sensing NTSC/PAL signal and sensing of no-signal.

L/R SEL : Decide the SSPL and SSPR by the external input L/R signal.

7. Pin Configuration

Table 1. Pin Configuration

Pin No.	Name	Type	I/O Pad	Pin No.	Name	Type	I/O Pad
1	CSY	IN	Normal	25	SSPL	OUT	Tri-State(4㎃)
2	VSM	IN	Normal	26	RBLK	OUT	4㎃
3	VDD	Power	-	27	GND	Ground	-
4	LRS	IN	Pull-Up	28	MOD1	OUT	4㎃
5	UDS	IN	Pull-Up	29	SOE	OUT	4㎃
6	MODE3	IN	Pull-Up	30	SSC	OUT	8㎃
7	MODE2	IN	Pull-Up	31	DET	OUT	4㎃
8	MODE1	IN	Pull-Up	32	SSPR	OUT	4㎃
9	HSY	OUT	4㎃	33	VSM_P	IN	Pull-Up
10	VSY	OUT	4㎃	34	VDD	Power	-
11	GND	Ground	-	35	GOE_S	IN	Pull-Down
12	DIV	OUT	4㎃	36	GSP_S	IN	Pull-Down
13	DIV_RC	IN	Normal	37	STRN	IN	Pull-Down
14	PDP	OUT	Tri-State(4㎃)	38	N_P	IN	Pull-Up
15	VDD	Power	-	39	CSY_P	IN	Pull-Down
16	RESET	IN	Normal	40	ATMN	IN	Pull-Down
17	NP	OUT	4㎃	41	SSP_S2	IN	Pull-Down
18	MCLK	IN	Normal	42	SSP_S1	IN	Pull-Down
19	MCLKO	OUT	4㎃	43	GSS_S	IN	Pull-Down
20	FSEL	IN	Pull-Up	44	GND	Ground	-
21	UDO	OUT	4㎃	45	VCAC	OUT	4㎃
22	GND	Ground	-	46	HSYSC	OUT	4㎃
23	GSP	OUT	4㎃	47	FRP	OUT	4㎃
24	GSC	OUT	4㎃	48	PSAM	IN	Pull-Up

Notice : All Pull-Down pad should be connected with VDD or GND.

8. Signal Description

Table 2. Signal Description

No.	Name	PIN	Function	Description
1	CSY	I	Sync Signal Input	Composite Sync Signal or Horizontal Sync Signal Input (Synchronization Period : Hi time)
2	VSM	I	Sync Signal Input	Vertical Modulated Signal from Composite Signal or Vertical Sync Signal Input
3	VDD	-	Power	5.0V DC Voltage (±10%)
4	LRS	I	Horizontal Scanning Direction Select	When LRS "H" : SSPL"Enable", SSPR "Hi-Z", LRO"L" (Right → Left Direction Scan) When LRS "L" : SSPL"Hi-Z", SSPR "Enable", LRO"H" (Left → Right Direction Scan)
5	UDS	I	Vertical Scanning Direction Select	When UDS "H" : UDO="L" (Up → Down Direction Scan) When UDS "L" : UDO="H" (Down → Up Direction Scan)
6	MODE3	I	Screen Display Mode Selection 3	* Refer to Table 3, Fig. 3-1,3-2,3-3,3-4,3-5
7	MODE2	I	Screen Display Mode Selection 2	* Refer to Table 3, Fig. 3-1,3-2,3-3,3-4,3-5
8	MODE1	I	Screen Display Mode Selection 1	* Refer to Table 3, Fig. 3-1,3-2,3-3,3-4,3-5
9	HSY	O	Horizontal sync Output(Negative)	Horizontal sync Output (Negative)
10	VSY	O	Vertical sync Output(Negative)	Vertical sync Output (Negative)
11	GND	-	Ground	Ground
12	DIV	O	Horizontal Display Position Control	Horizontal Display Position is controlled by DIV. PDP signal synchronized DIV. PLL Circuit block makes MCLK. (Refer to Fig.12)
13	DIV_RC	I	Horizontal Display Position Control Input	For external horizontal display position control. DIV output adopted external circuit and DIV_RC synchronized PDP Signal. (Refer to Fig.12)
14	PDP	O	Phase detect Pulse	It is made by CSY and DIV. External PLL circuit was synchronized by PDP Signal. (Refer to Fig.4, 12)
15	VDD	-	Power	5.0V DC Voltage (±10%)
16	RESET	I	Reset	Logic Initial Reset
17	NP	O	NTSC/PAL Selection output	When ATMN "H" : NP= "H" at NTSC, NP= "L" at PAL input [Auto detect mode] When ATMN "L" : NP output depends on input NTSC/PAL select signal N_P. [N_P="H" (NTSC), N_P="L" (PAL)]
18	MCLK	I	Main Clock	It's a synchronized Clock which is made by PLL circuit. It is used timing controller main clock .(Refer to Fig.12)

No.	Name	PIN	Function	Description
19	MCLKO	O	Clock output	For synchronizing PLL MCLKO inverted output MCLK (typ : 23.9㎒) (Refer to Fig.12)
20	FSEL	I	No Signal Detect Selection Pin	FSEL"H" : Black Screen Display when No Signal. FSEL"L" : none use
21	UDO	O	Gate Drive IC Up/Down Selection Output	When UDS "H" : UDO = "L" (Down → Up Direction Scan) When UDS "L" : UDO = "H" (Up → Down Direction Scan)
22	GND	-	Ground	Ground
23	GSP	O	Gate Drive IC Start Pulse	It is synchronized GSC falling edge which is 1 Horizontal High t ime Period width and 1 Vertical Frequency. (Refer to Fig.6, 7)
24	GSC	O	Gate Drive IC Shift Clock	It's used Gate Drive IC Shift Clock. (Refer to Fig.6, 7, 8)
25	SSPL	O	Horizontal Start Pulse(Left)	When LRS "H" : SSPL"output", SSPR "Hi-Z" (Left → Right Direction Scan) When LRS "L" : SSPL"Hi-Z", SSPR "output" (Right → Left Direction Scan)
26	RBLK	O	4:3 Mode Side Black Control	It's used for 4:3 Mode Display Side Black Control Display Enable. It's used for CHROMA IC H-Blanking input.
27	GND	-	Ground	Ground
28	MOD1	O	Gate Drive IC Output Method Control	When LRS "H", N_P"H", MODE3,2,1 "HLL,LLH", MOD1 "L" output Else MOD1"H" output
29	SOE	O	Source Drive IC Output Enable	Image Data enter into Liquid Crystal Panel data line from Source Drive IC. Which is inverted FRP Signal
30	SSC	O	Source D-IC Shift Clock	It is used for Source Drive IC Shift Clock which is differ from Image Display Mode.
31	DET	O	For No-Signal Test	Video signal detection output Video Signal : "H", No-Signal : "L"
32	SSPR	O	Horizontal Start Pulse(Right)	When LRS "H" : SSPL"output", SSPR "Hi-Z (Left → Right Direction Scan) When LRS "L" : SSPL"Hi-Z", SSPR "output" (Right → Left Direction Scan)
33	VSM_P	I	VSM polarity Control	VSM_P can replace the negative VSM with the positive VSM. Default : "L"
34	VDD	-	Power	5.0V DC Voltage (±10%)
35	GOE_S	I	Internal FSC Control	This option control Internal FSC Width which is control Gate Drive IC Output. (Refer to Table 4)
36	GSP_S	I	GSP Position Control	GSP Signal outputs referred to page 15,16 timing Diagram when GSP_S is "L" If GSP_S is "H" above GSP shifted 1 Horizontal Period.

No.	Name	PIN	Function	Description
37	STRN	I	ODD/EVEN GSP Position Control	Refer to Fig.6, 7
38	N_P	I	Manual NTSC/PAL Selection	When ATMN "L" : NP output depends on input NTSC/PAL select signal N_P. [N_P="H" (NTSC), N_P="L" (PAL)]
39	CSY_P	I	CSY polarity Control	CSY_P can replace the negative CSY with the positive CSY. Default : "L"
40	ATMN	I	NTSC/PAL Auto Selection	When ATMN "H" : NTSC/PAL input Automatically detect. (NTSC/PAL selection output pin "NP" automatically detected chip inside) When ATMN "H": NP = "H" output at NTSC input NP = "L" output at PAL input When ATMN "L": NTSC/PAL manually selected by N_P input.
41	SSP_S2	I	SSP Start Position Control	Horizontal Screen Display Position controlled by SSP_S2, SSP_S1 which is change SSPL,SSPR position.(Refer to Fig.5)
42	SSP_S1	I	SSP Start Position Control	Horizontal Screen Display Position controlled by SSP_S2, SSP_S1 which is change SSPL,SSPR position.(Refer to Fig.5)
43	GSS_S	I	GSC Control at NTSC Mode	It is Control GSC output when NTSC Vertical expand mode(Cinema,Wide2), which is refer to page 19.
44	GND	-	Ground	Ground
45	VCAC	O	Common Voltage Control Signal	It's used for Liquid Crystal Panel Common Voltage Control Signal.
46	HSYSC	O	Hsync Output (Negative)	It's used for CHROMA IC Hsync Input.
47	FRP	O	Video Signal Polarity Control	It's used for Video image Signal Polarity Control input.
48	PSAM	I	Sampling Mode selection	Source drive IC data sampling mode select Successive Sampling Mode : "H', Simultaneously Sampling Mode : "L

9. Electrical SPECIFICATION

(1) Absolute Maximum Rating

Item	Parameter	Min	Typ	Max	Unit	Notes
V_{DD}	Input Voltage	-0.5	-	7.0	V	
V_I	CMOS input Signal Voltage	-0.5	-	V_{DD}+0.5	V	
V_O	CMOS output Signal Voltage	-0.5	-	V_{DD}+0.5	V	
T_{STG}	Storage temperature	-40	-	+125	℃	
T_{LSTG}	Lead Temperature(Soldering, 4sec)	-	-	+260	℃	

※ Notes : this can be destroyed over the maximum rating, LPL didn't assure the secure of component.
All function of this component must be operated under normal operating condition

2. Normal Operating Condition

Item	Parameter	Min	Typ	Max	Unit	Notes
V_{DD}	Input Voltage	4.5	5.0	5.5	V	
V_{IL}	CMOS Input Signal Low Voltage	-0.5	-	0.3*V_{DD}	V	
V_{IH}	CMOS Input Signal High Voltage	0.7*V_{DD}	-	V_{DD}+0.5	V	
V_{OL}	CMOS Output Signal Low Voltage	-	-	V_{SS}+0.1	V	
V_{OH}	CMOS Output Signal High Voltage	V_{DD}-0.1	-	-	V	
T_{OPR}	Operating Temperature	-30	25	85	℃	
T_{REOPR}	Reliability Operating Temperature	-10	25	85	℃	

10. Screen Display range

1) NTSC (N_T = 'H', ATMN = 'L')

(1) Horizontal Direction

a1) FULL Display MODE

a2) Normal Display

a3) WIDE Display

(2) Vertical Direction (refer to page 17)

b1) FULL Display MODE : 23H ~ 256H

b2) CINEMA Display MODE : 54H ~ 229H

b3) WIDE2 Display MODE : 50H ~ 236H

2) PAL (N_T = 'L', ATMN = 'L')

(1) Horizontal Direction

a1) FULL Display MODE

a2) Normal Display

a3) WIDE Display

(2) Vertical Direction (refer to page 18)

b1) FULL Display MODE : Display 28H ~300H [eliminate (14n +1, 14n + 7)].

b2) CINEMA Display MODE : Display 47H ~ 280H

b3) WIDE2 Display MODE : Display 35H ~303H [eliminate (22n +1. 22n +16)].

11. MODE Setting

Table 3. Mode Setting

MODE3	MODE2	MODE1	MODE	Description	Source	Notes
H	H	H	FULL MODE	Display evenly by controlling frequency evenly of whole display under vertical, horizontal range of input signal. It uses 16:9 wide input. Display wide horizontally in case of the display ratio 4:3.	16:9 image	Fig. 3-1
H	H	L	WIDE1 MODE	Change horizontal Clock to make image output of center display similar with image input to loose incompatibility with center display under 4:3 Full mode.	16:9 image	Fig. 3-2
L	H	H	NORMAL MODE	Display to make same with real display size under input 4:3 display signal, which Left/right side displayed black.	4:3 Image	Fig. 3-3
H	L	L	CINEMA MODE	The main display area of wide signal(16:9) such like Letter focus size.Use Full mode horizontally, use more wide than usual vertically to make similar with real image	Letter Focus Wide Input	Fig. 3-4
L	L	H	WIDE2 MODE	Make the display same with WIDE1 horizontally and use CINEMA vertically to control center display under 4:3 display mode. Sort of vertical signal can't be seen.	16:9 image	Fig. 3-5
L	L	L	test	Test mode	test	test
L	H	L	test	Test mode	test	test
H	L	H	test	Test mode	test	test

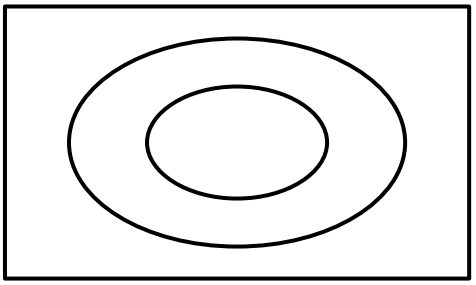


Fig. 3-1 FULL Display MODE

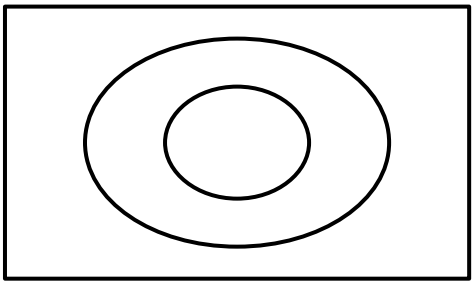


Fig. 3-2 WIDE Display MODE

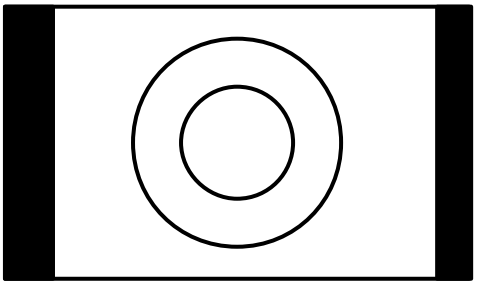


Fig. 3-3 NORMAL Display MODE

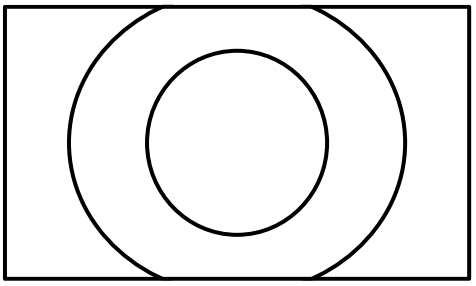


Fig. 3-4 CINEMA Display MODE

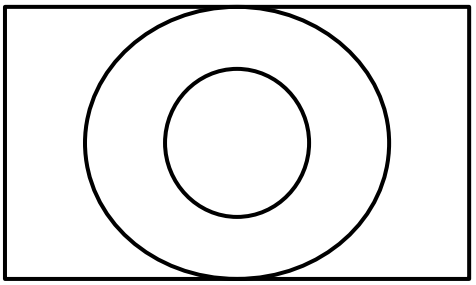


Fig. 3-5 WIDE2 Display MODE

12. DIV, HSY, HSYSC, RBLK Generation

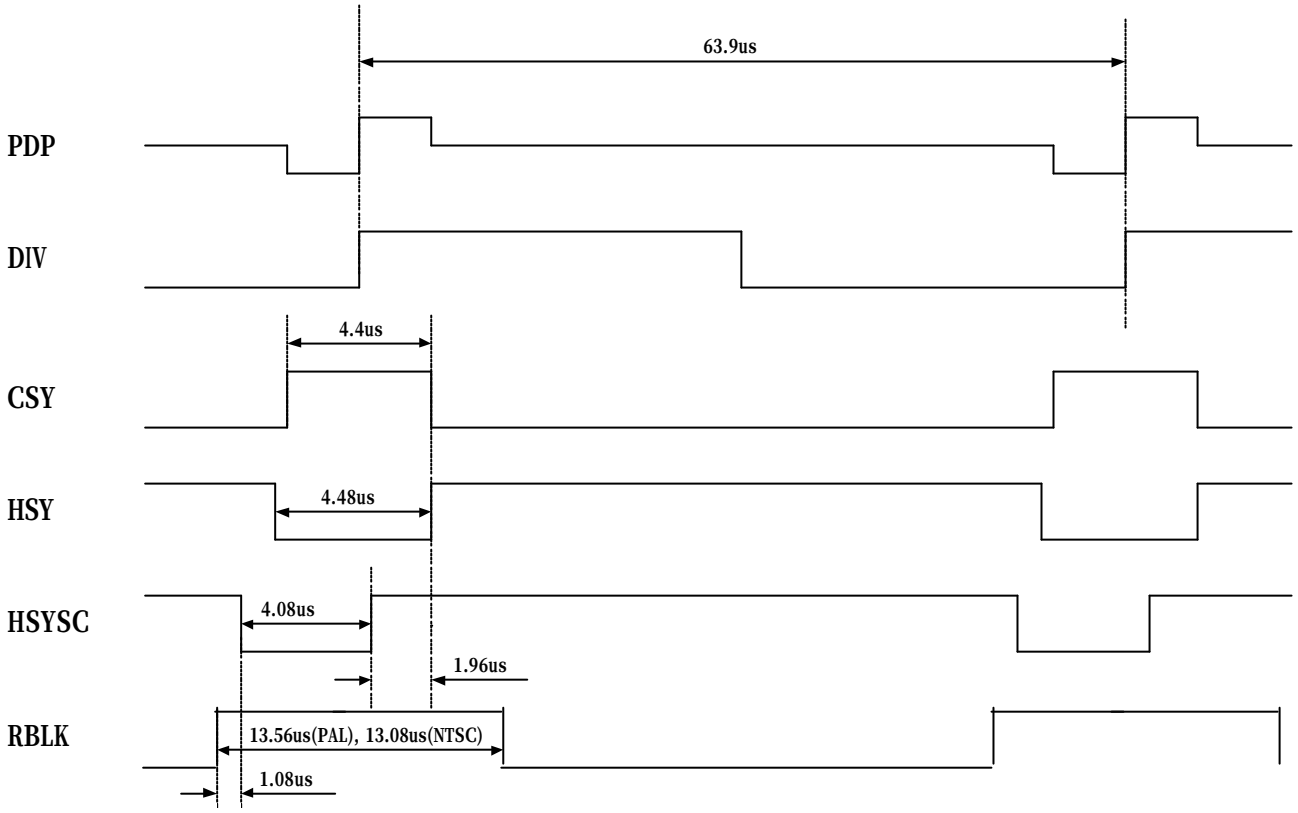
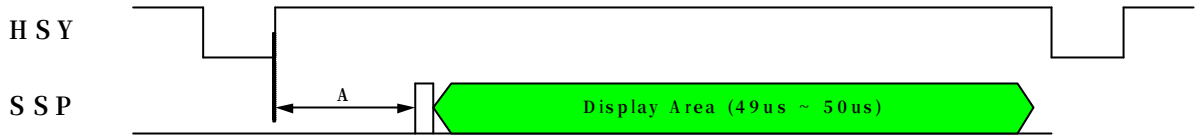


Fig. 4 DIV, HSY,HSYSC Generation

13. Horizontal Display Position

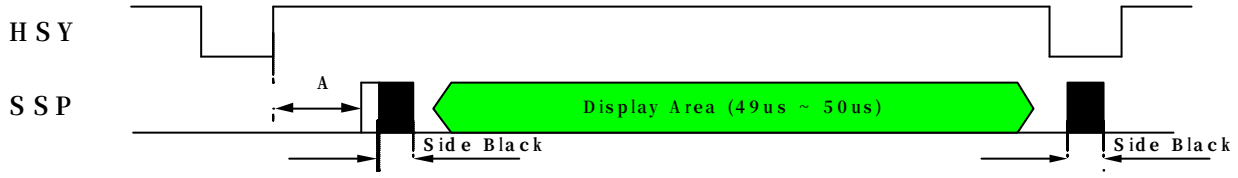
(1) Full/CINEMA/WIDE2 Mode



■ SSP Position (A)

SSP CONTROL		NTSC		PAL		Unit	Notes
SSP_S2	SSP_S1	Successive	Simultaneous	Successive	Simultaneous		
L	L	62	19	66	21	Used Clock	-
L	H	63	20	67	22	Used Clock	-
H	L	64	21	68	23	Used Clock	-
H	H	61	22	69	24	Used Clock	-
Used Clock		Successive Mode		Simultaneously Mode			
		11.95Mhz(83.66ns)		3.984Mhz(250.98ns)			

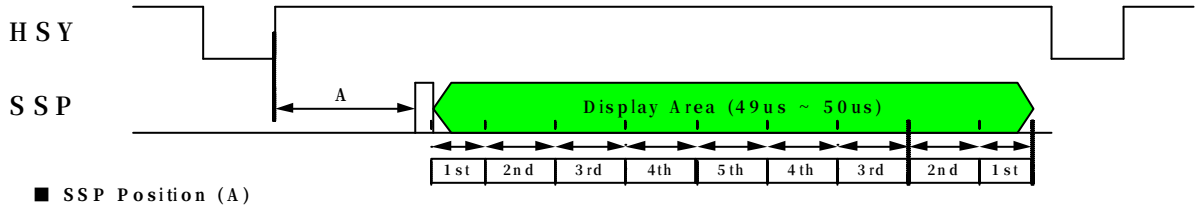
(2) Normal Mode



■ SSP Position (A)

SSP CONTROL		NTSC		PAL		Unit	Notes
SSP_S2	SSP_S1	Successive	Simultaneous	Successive	Simultaneous		
L	L	10	13	9	14	Used Clock	-
L	H	11	14	10	15	Used Clock	-
H	L	12	15	11	16	Used Clock	-
H	H	9	12	8	13	Used Clock	-
Used Clock		Successive Mode			Simultaneously Mode		
		Display Area	Side Black		Display Area	Side Black	
		8.96Mhz(111.55ns)	23.9Mhz(41.83ns)		2.99Mhz(334.64ns)	11.95Mhz(83.66ns)	

(3) Wide1 Mode



■ SSP Position (A)

SSP CONTROL		NTSC		PAL		Unit	Notes
SSP_S2	SSP_S1	Successive	Simultaneous	Successive	Simultaneous		
L	L	65	21	61	18	Used Clock	-
L	H	66	22	62	19	Used Clock	-
H	L	67	23	63	20	Used Clock	-
H	H	64	20	60	17	Used Clock	-

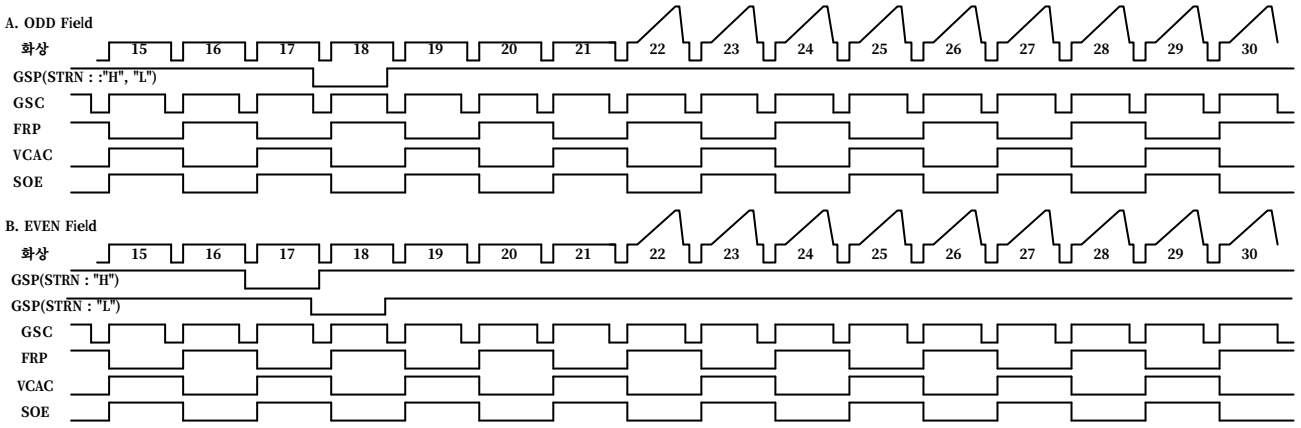
Used Clock	Successive Mode					Simultaneously Mode				
	1st	2nd	3rd	4th	5th	1st	2nd	3rd	4th	5th
	13.02M	12.5M	11.95M	11.43M	11.03M	4.35M	41.6M	39.9M	38.3M	36.8M

Notes : When LRS "H" SSPL output SSPR high impedance
When LRS "L" SSPH output SSPL high impedance

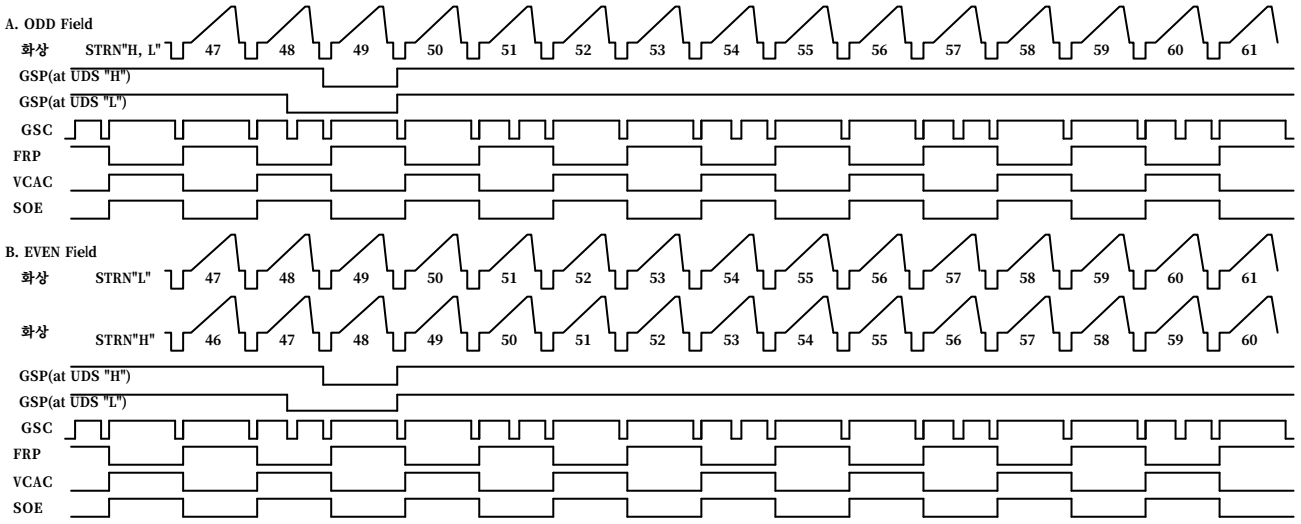
Fig. 5 Horizontal Display Position

14. Vertical Display Method(NTSC)

(1)Vertical 23H ~ 256H



(2)Vertical From54H to 229H



(3)Vertical From50H to 236H

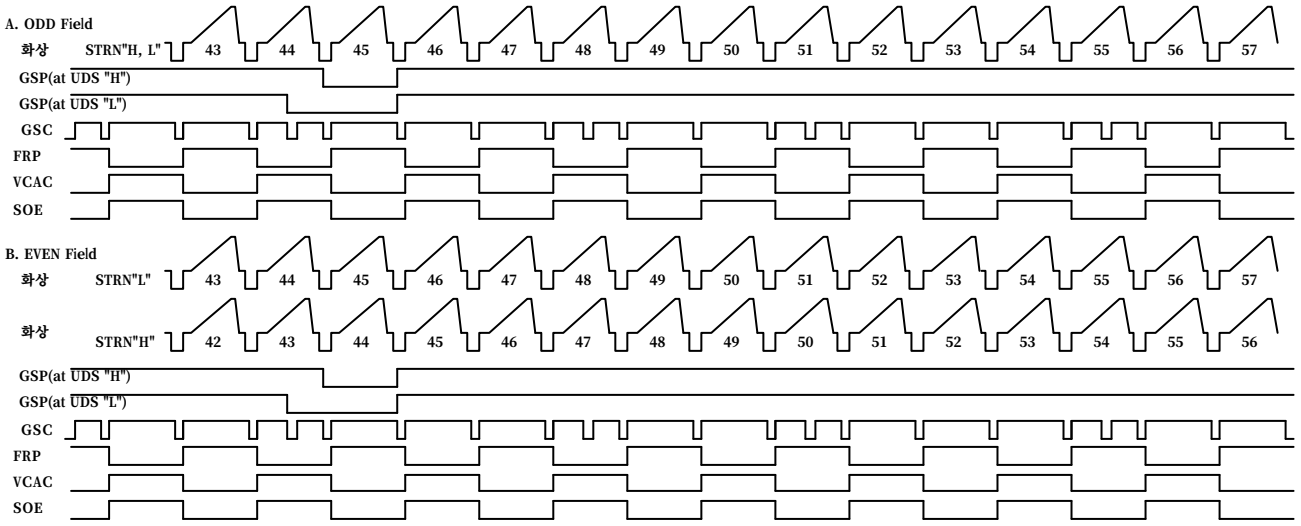


Fig. 6 Vertical Display Position(NTSC)

15. Vertical Display Method(PAL)

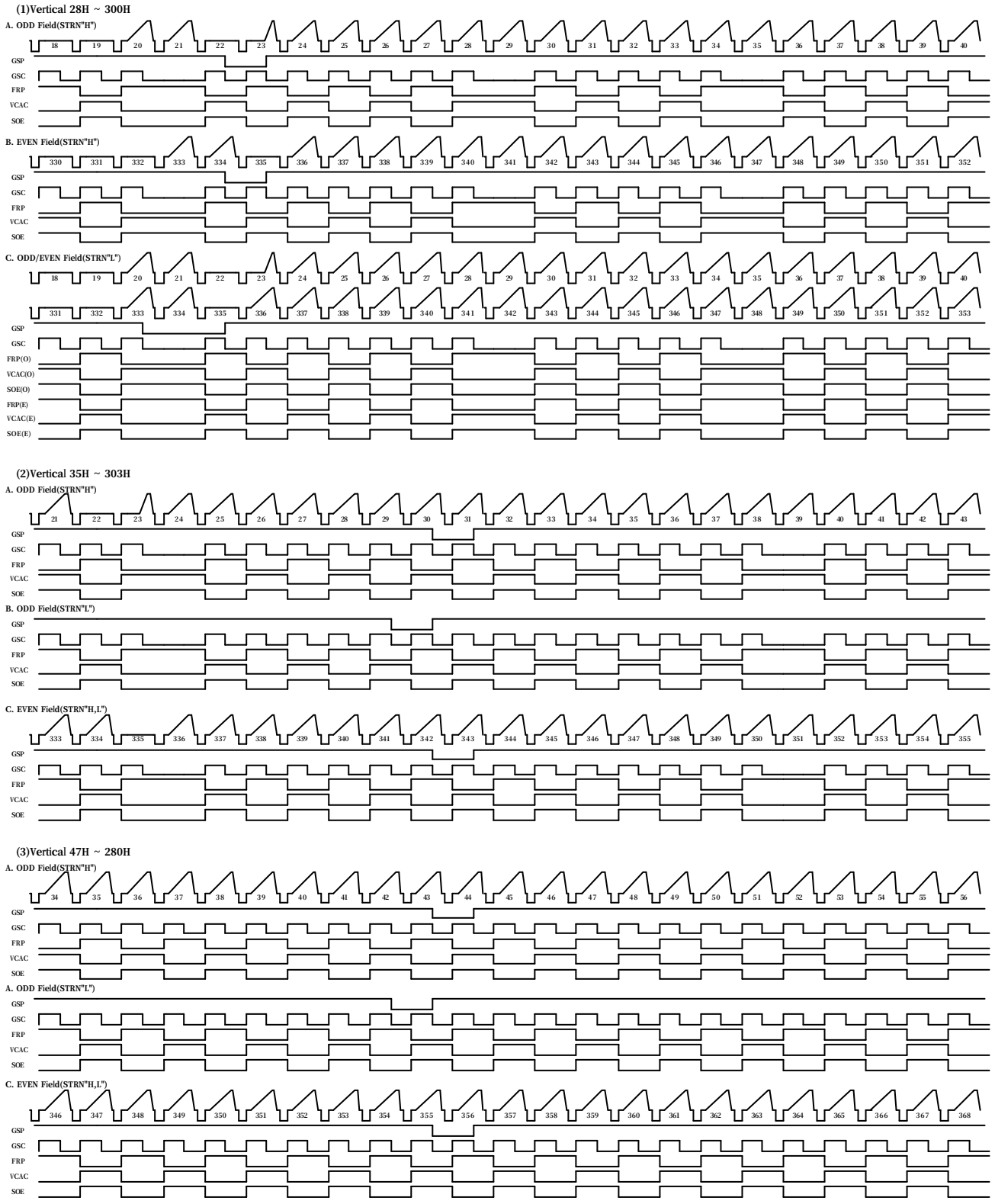


Fig.7 Vertical Display Position(PAL)

16. Control Option

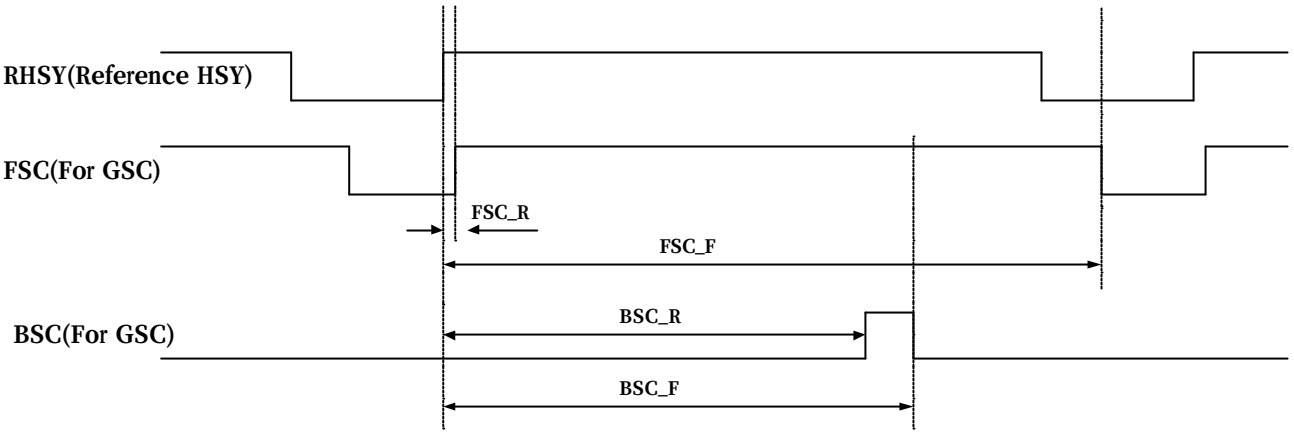


Fig. 8 Control Option

Table 4. Control Option

GOE_S	FSC_R	FSC_F	Unit	Note
H	4	1456	Main Clock	1)
L	0	1440	Main Clock	1)

GSS_S	BSC_R	BSC_F	Unit	Note
H	850	880	Main Clock	2)
L	420	450	Main Clock	2)

Notes. 1), 2) This signal used for GSC Signal.

When UDS input high and Vertical expansion Display, internal GSC generated. which is modulated by display position.

17. Package

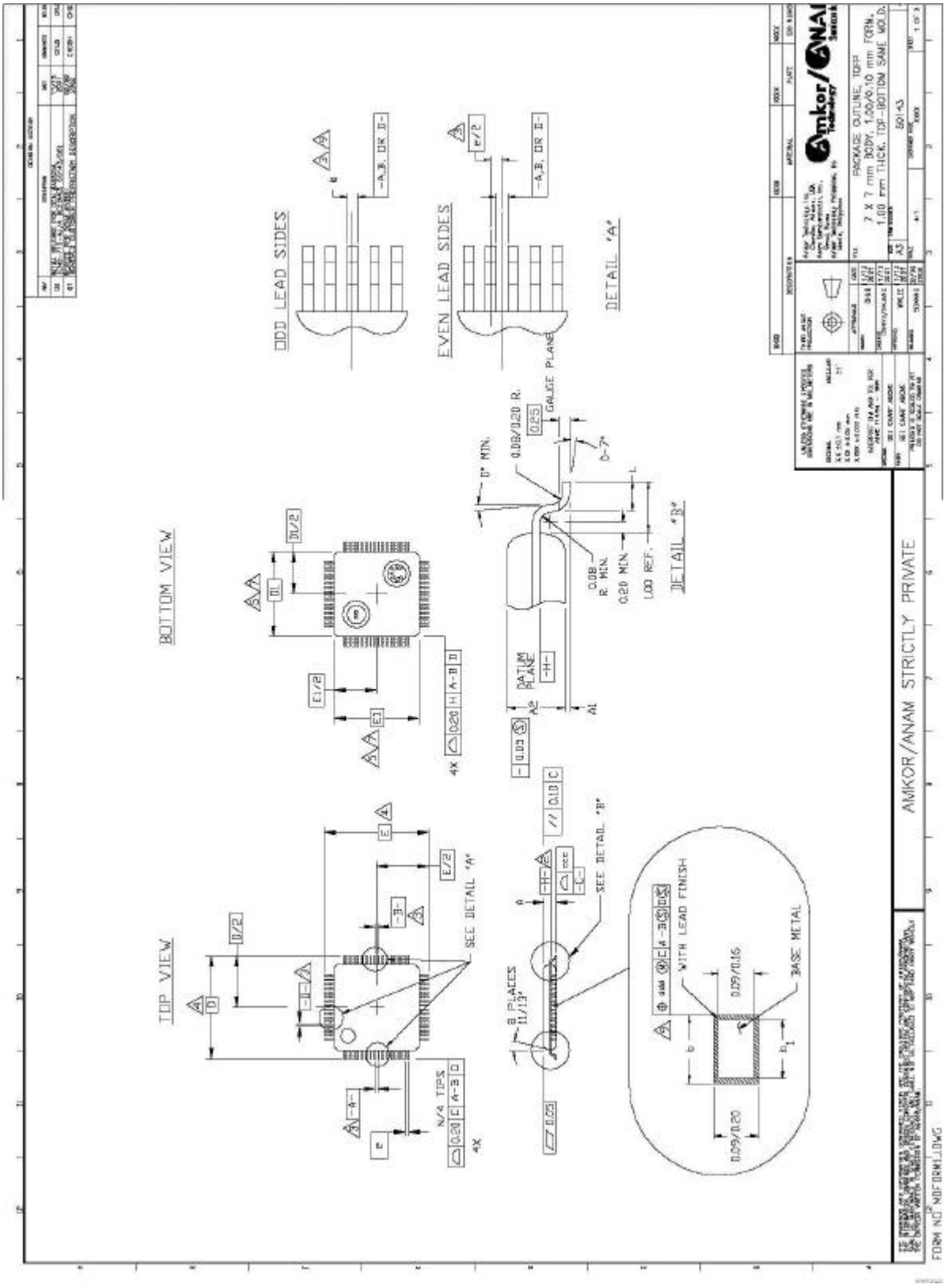


Fig. 9 Package

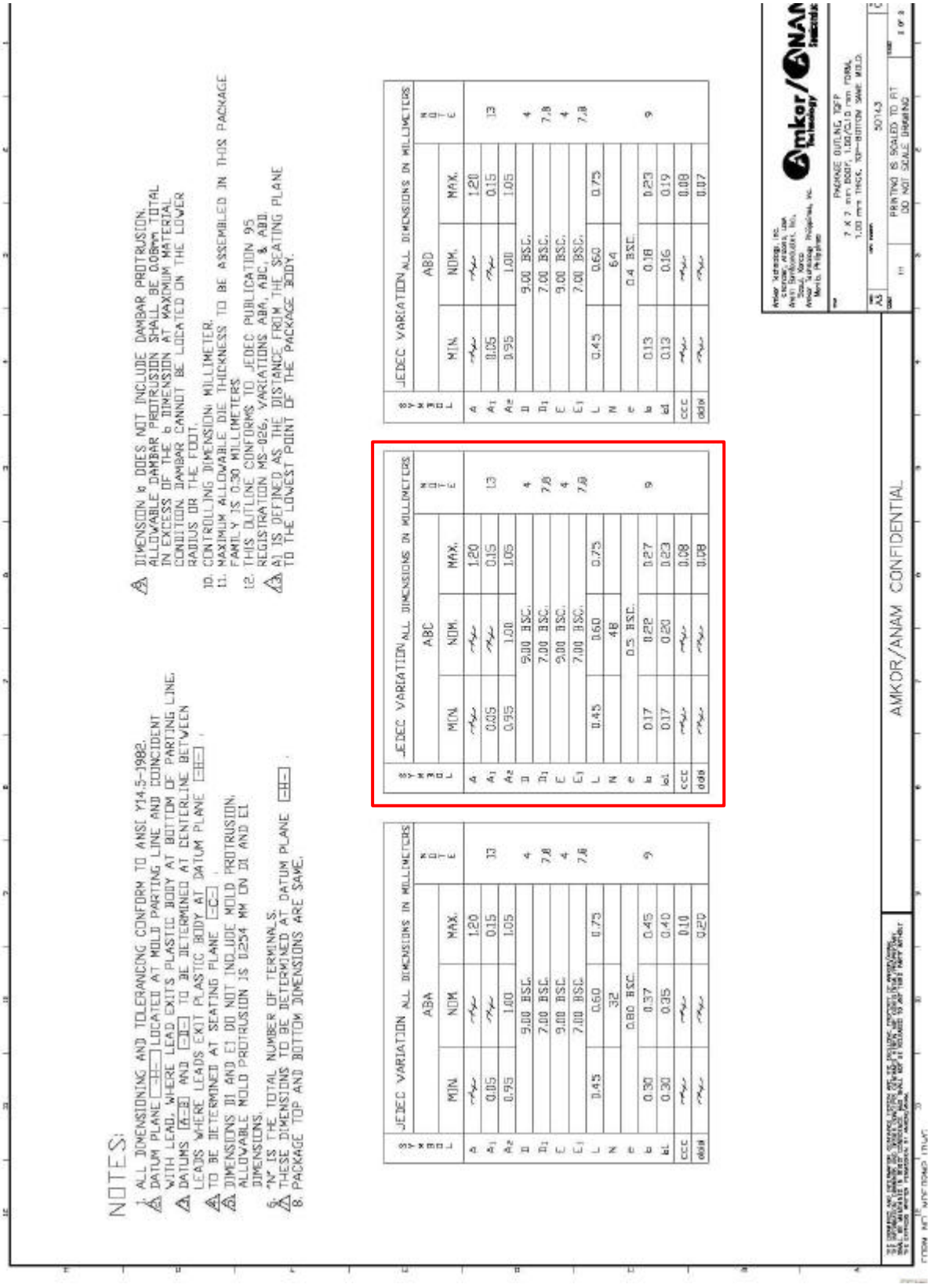


Fig. 10 Package

18. Application Circuit

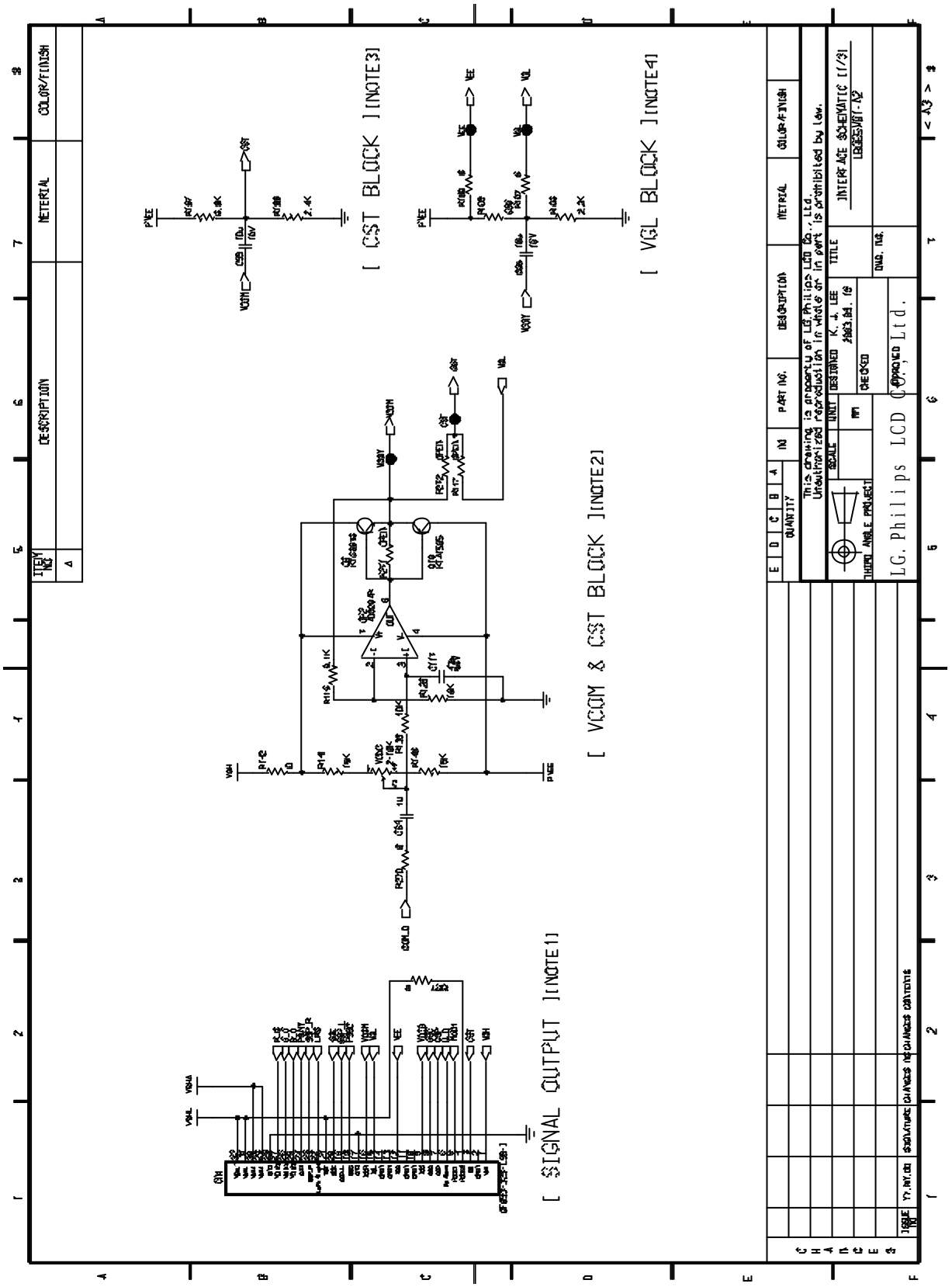


Fig. 11 Application Circuit

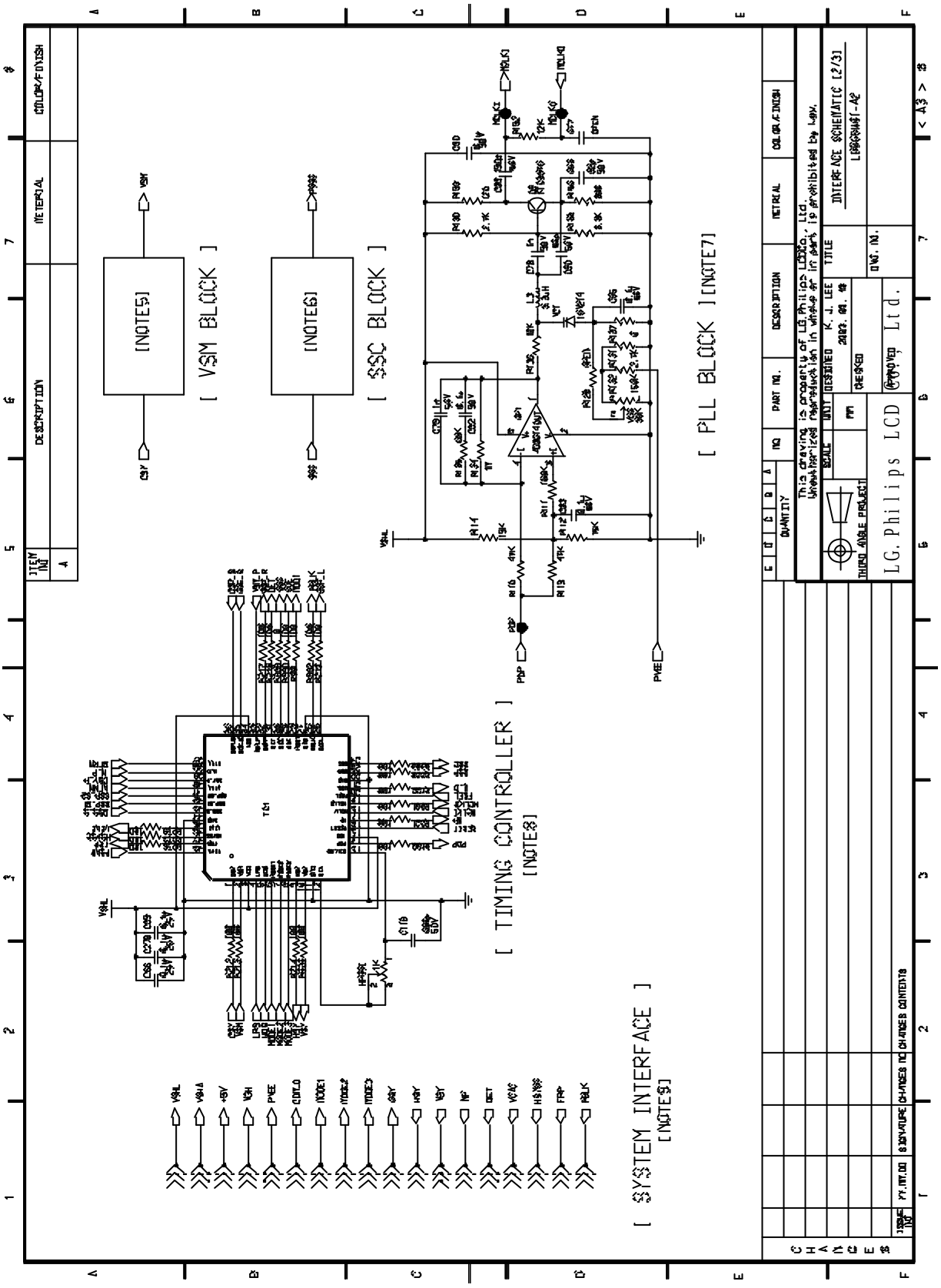


Fig. 12 Application Circuit

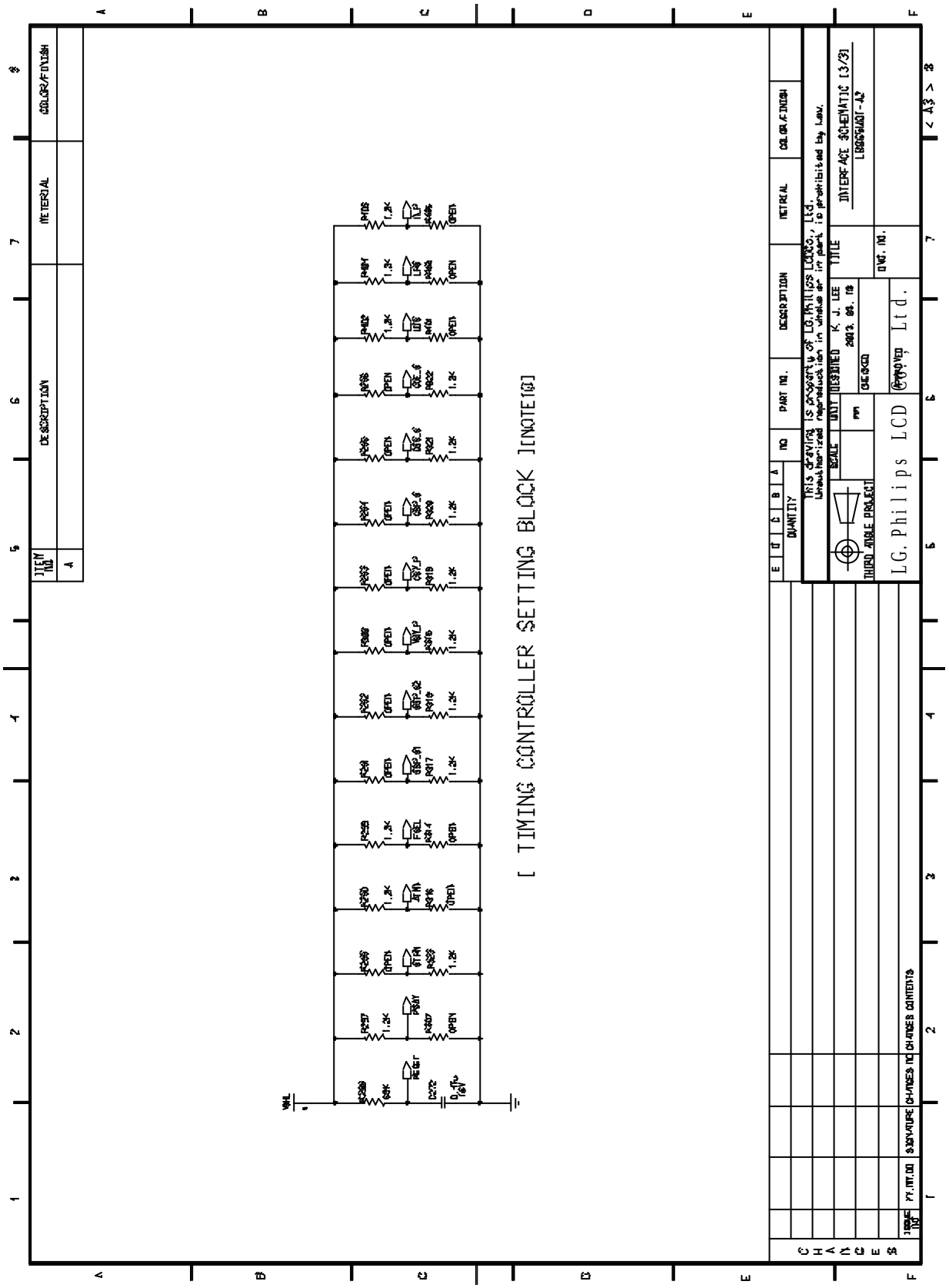


Fig. 13 Application Circuit

19. Application Notes

[NOTE] This is for your reference and it could need to optimize R, C values according to the system.
All of condition for LCD operating ,not mentioned in this sheet, should follow CAS of LCD.

[NOTE 1] SIGNAL OUTPUT Block is connected with input of LCM(6.5") and the signal name which is interfaced with LCM is followed CN1.(Not port name)
VSHL,VSHA,VSS,VCC,VGH is the power for operating LCM, the circuit should be composed to meet the condition of CAS.

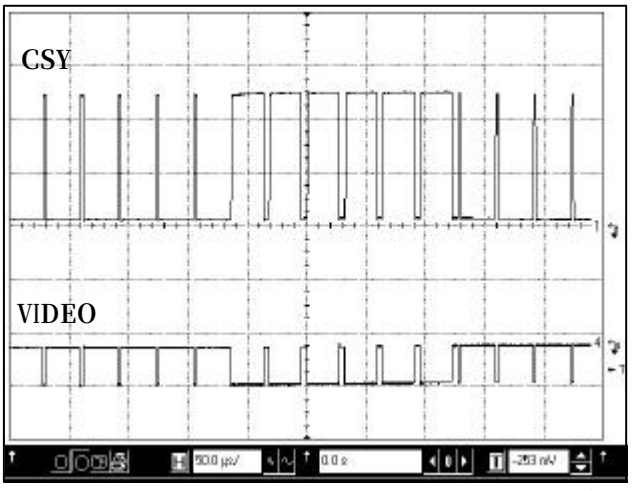
[NOTE 2] COM_O is the voltage which is generated from Video decoder for operating LCD, AC voltage of VCOM and level of DC voltage, which is generated from this, should be optimized to meet CAS.

[NOTE 3,4] CST and VGL Block , which is for applying LCM to use VCOM, should also be optimized to meet CAS. If you use PAL signal, Coupling capacitance, has an effect on display quality, should be optimized.

[NOTE 5] CSY ,which put in VSM signal, must meet [Table 1].

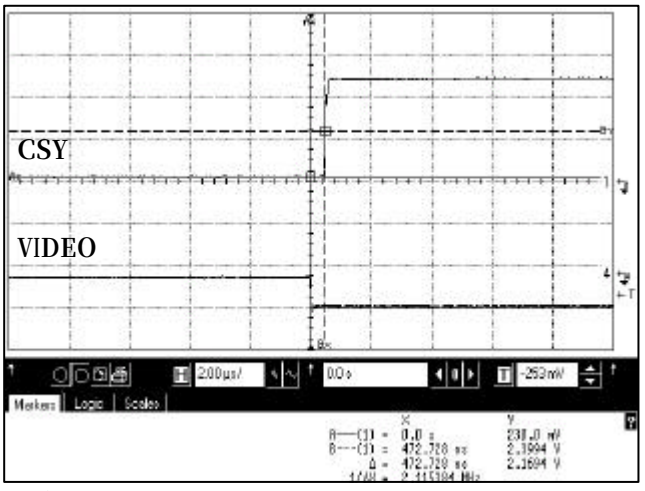
[Table 1]

CSY signal	MIN	TYP	MAX
Voltage level	3.0V	5.0V	5.5V
Delay time against CSY falling time	0us	0.5us	1.0us



[Video In vs. CSY]

→ zoom →

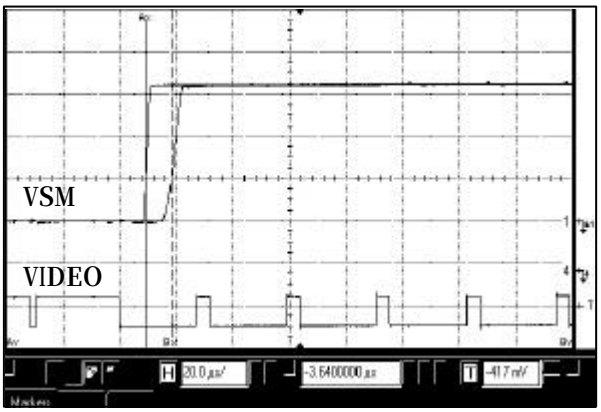


[Delay time of REFERENCE circuit]

[NOTE 5-1] "VSM" which is output of VSM circuit must meet [Table 2].
If it can't, it's possible to appear noise on display.
When you check delay time of VSM signal, the basis of voltage level is 1.5V.

[Table 2]

VSM signal	MIN	TYP	MAX
Delay time against VSY falling time	9.5us	-	18.5us

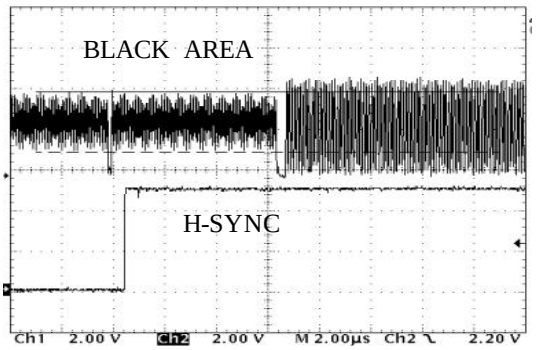


주의) If VSM signal delay,
VSM meet at least [Table 3]

[Table 3] [VSM signal MARGIN]

VSM signal	MIN	TYP	MAX
VSY falling time against delay time	44.0us	-	52.8us

[NOTE 6] SSC should follow HOLD time and SET UP mentioned in CAS,
LEVEL of SIDE BLACK also should meet [Table 4] in 4:3 Mode and FULL MODE,
by using appropriate Filter and the wave form is sine,



[The wave form of SIDE BLACK section in 4:3]

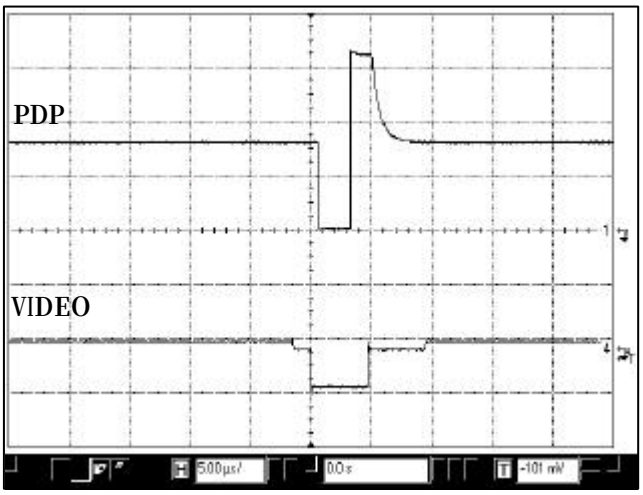
[Table 4]

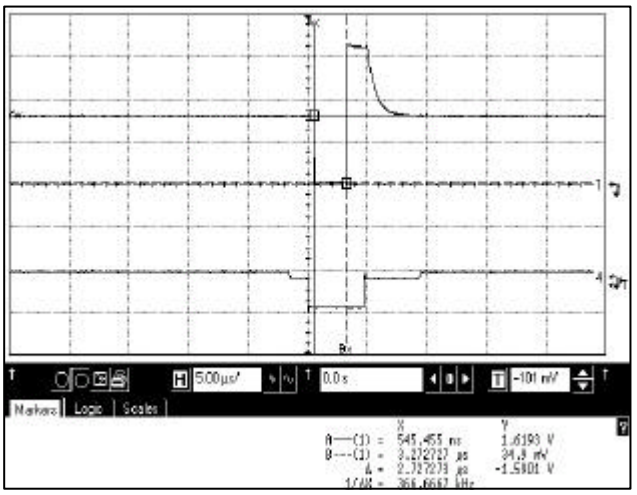
SPEC / MODE	MIN.	TYP.	MAX.
4:3	2.5V	-	5.0V
FULL	3.0V	-	5.0V

[NOTE 7] PDP signal, input signal of PLL circuit, should meet [Table 5] when no video signal.
When video signal applied, PDP signal is optimized when it check in 25th line of "Odd Frame" and then Low section of PDP is within Sync blank as below

[Table 5]

PDP	MIN	TYP	MAX
No signal	3.1V	3.3V	3.5V

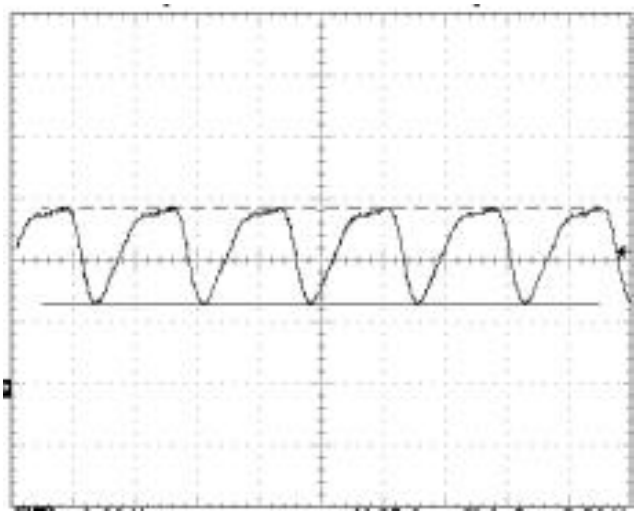




[NOTE 7-1] Final output of MCLKI in PLL block should follow [Table 6]

[Table 6]

MCLKI	MIN	TYP	MAX
DC level	2.2V	2.3V	2.4V
AC lever	1.5V	2.0V	5.0V



[MCLKI of Reference circuit when no video signal]

[NOTE 7-2] PLL circuit

1st proposal) When VCO is fixed - no use variable resistor - (Refer to PLL circuit of Fig.12,[Table 7])

R137= 0Ω, R128= Open

2nd proposal) When VCO is controlled to use variable resistor (Refer to PLL circuit of Fig.12,[Table 7])

R137=Open, R128=0Ω

Notes1) The power of PLL circuit for VCO must be stable as based on 1H.

Notes 2) After you control R131,137 to be optimized, to became Anode voltage of VC1, −2.27V ± 0.02V, control VCO variable resistor to became the frequency of MCLKI, 23.9㎒.

[Table 7]

L3	C80	C93	Demultiply ratio	B H P(Measure)	BHP/ ratio	MCLKI	Notes
3.3uH	56pF	82pF	1530	64000	41.83	23.9Mhz	Fixed
3.9uH	150pF	100pF	1530	64000	41.83	23.9Mhz	Variable

[NOTE 8] Right and left of H-position become symmetry when PIN12,13 of TCON is connected and C119=Open.
If you need to change H-Position, control HPOSI and C119 ,base on the circuit of Fig 12,

[NOTE 8-1] In case of SHARP Decoder IC(IR3Y29BM), VCAC(PIN45) is connected with 32nd pin, "COMMON FRP".
In case of JRC Decoder IC(NJM2529), VCAC(PIN45) is connected with 64th pin, "VCOMIN"
If you use other company's IC, you should connect with same function pin.

[NOTE 8-2] In case of SHARP Decoder IC(IR3Y29BM), HSYSC(PIN46) is connected with 34th pin, "SYNC IN".
In case of JRC Decoder IC(NJM2529), HSYSC(PIN46) is connected with 57th pin, "HSYIN".
If you use other company's IC, you should connect with same function pin.

[NOTE 8-3] N_P(PIN38) is for choosing NTSC/PAL, If you set ATMN(PIN40) to 'H',
It can be chosen NTSC/PAL automatically, If you set ATMN to 'L', It can be chosen NTSC, PAL as N_P Option

[NOTE 8-4] RBLK(PIN26) is for H-BLANKING of Video Decoder
to make blanking left and right in 4:3 MODE

[NOTE 9]Capacitance for ripple filter, which is used in VGL circuit, should maintain min.40uF.
If it's under, Horizontal line of PAL signal can occur.

[NOTE 9-1]VSHL(VSHA),VSS,VCC,VGH should follow CAS of LCD.
The power sequence ,when power on, also must follow CAS.

- POWER ON : VSH → VSS → VCC → VGL→ VGH
- POWER OFF : VGH → VGL → VCC → VSS → VSH
(VSHA=VAHL=VSH= +5V)

[NOTE 9-2] DET pin is output pin of LOGIC level when no signal and this can be used if you need.

[NOTE 9-3] The display size as MODE1,2,3 of Logic is mentioned at page 12~14.

[NOTE 9-4] NP can generate switching signal for controlling of NTSC/PAL changing based on the condition of [NOTE 8-3],if the decoder doesn't have function to detect NTSC/PAL.

[NOTE 10] If the display has tremble due to difference of resolution between LCD and TV STRN(PIN31) should be optimized.

[NOTE 10-1] PSAM and LRS is connected with PIN48,PIN4 of TIMING CONTROLLER and PSAM, LRS of SINGANL OUTPUT[NOTE1].

※ Component List (Fig. 11 ~ 13)

No	Description of Specification	Reference	Qty
1	CAPACITOR,CHIP[CERAMIC M/L HD RF/S], 1NF 50V K X 1608 R/TP, S	C73 C78 C79	3
2	CAPACITOR,CHIP[CERAMIC M/L HD RF/S], 0.1UF 25V Z F 1608 R/TP, S	C66 C85 C270	3
3	CAPACITOR,CHIP[CERAMIC M/L HD RF/S], 0.1UF 50V K X7R 1608 R/TP, S	C75 C82 C83 C90 C95	5
4	CAPACITOR, HIGH-DIELECTRIC, 10UF, 10 Volt, K PER, X5R(JB), 3216 R/TP, S	C64 C65 C99	3
5	CAPACITOR,CHIP[CERAMIC M/L TC RF/S], 82PF 50V J NP0 1608 R/TP, S	C93	1
6	CAPACITOR,CHIP[CERAMIC M/L TC RF/S], 150PF 50V J NP0 1608 R/TP, S	C89	1
7	CAPACITOR,CHIP[CERAMIC M/L TC RF/S], 56PF 50V J NP0 1608 R/TP, S	C80	1
8	CAPACITOR,CHIP[CERAMIC M/L TC RF/S], 47PF 50V J NP0 1608 R/TP, S	C117	1
9	CAPACITOR,CHIP[CERAMIC M/L TC RF/S], 680PF 50V J NP0 1608 R/TP, S	C119	1
10	IC,ANALOG DEVICE, AD820AR-REEL, S	OP2	1
11	IC,ANALOG DEVICE, AD8614ART-REEL7 , 5PIN SOT-23 TP OPAMP 1.45[MAX], S	OP1	1
12	INDUCTOR,CHIP, 3.3uH	L3	1
13	SISTOR,CHIP, 0 OHM 1/16W 1608 5% D R/TP, S	R107 R109 R137 R142 R270 R371 R989	7
14	RESISTOR,CHIP, 100 OHM 1/16W 1608 1% D R/TP, S	R218 R219 R220 R221 R276 R278 R182 R183 R212 R213 R214 R217 R279 R281 R282 R920 R990 R991 R992	19
15	5 RESISTOR,CHIP, 10K OHM 1/16W 1608 1% D R/TP, S	R120 R136 R139	3
16	RESISTOR,CHIP, 100K OHM 1/16W 1608 1% D R/TP, S	R111	1
17	RESISTOR,CHIP, 12K OHM OHM 1/16W 1608 1% D R/TP, S	R152	1
18	RESISTOR,CHIP, 1M OHM 1/16W 1608 1% D R/TP, S	R134	1
19	RESISTOR,CHIP, 120 OHM 1/16W 1608 1% D R/TP, S	R153	1
20	RESISTOR,CHIP, 1.2K OHM 1/16W 1608 1% D R/TP, S	R319 R320 R321 R322 R323 R402 R297 R299 R315 R290 R317 R318 R404 R406	14
21	RESISTOR,CHIP, 15K OHM 1/16W 1608 1% D R/TP, S	R114 R140 R141	3
22	RESISTOR,CHIP, 150K OHM 1/16W 1608 1% D R/TP, S	R132	1
23	RESISTOR,CHIP, 16K OHM 1/16W 1608 1% D R/TP, S	R112	1
24	RESISTOR,CHIP, 2.2K OHM 1/16W 1608 1% D R/TP, S	R106	1
25	RESISTOR,CHIP, 2.4K OHM 1/16W 1608 1% D R/TP, S	R188	1
26	RESISTOR,CHIP, 2.7K OHM 1/16W 1608 1% D R/TP, S	R130 R131	2
27	RESISTOR,CHIP, 3.3K OHM 1/16W 1608 1% D R/TP, S	R133	1
28	RESISTOR,CHIP, 390 OHM 1/16W 1608 1% D R/TP, S	R156	1
29	RESISTOR,CHIP, 47K OHM 1/16W 1608 1% D R/TP, S	R110 R113 R124	3
30	RESISTOR,CHIP, 680 OHM 1/16W 1608 1% D R/TP, S	R108	1
31	RESISTOR,CHIP, 6.8K OHM 1/16W 1608 1% D R/TP, S	R187	1
32	RESISTOR,CHIP, 68K OHM 1/16W 1608 1% D R/TP, S	R135 R288	2
33	RESISTOR,CHIP, 9.1K OHM 1/16W 1608 1% D R/TP, S	R119	1
34	RESISTOR,CHIP, 100OHM 5% 1/16W 3216 R/TP, S	AR7	1
35	TRANSISTORR, PNP KTA1505S-Y-RTK, S	Q10	1
36	TRANSISTORR, KTC3876S-Y-RTK , NPN, S	Q8 Q9	2
37	VARACTOR, 1SV214 SMD, S	VC1	1
38	VOLUME, 10K CVR-32A103, S	VCDC VCO	2
39	VOLUME, PANASONIC, 1K ohm, EVM3WSX80B13, S	HPOSI	1