Rockwell

10951
Bargraph and Numeric Display Controller

DESCRIPTION

The Rockwell 10951 Bargraph and Numeric Display Controller is an LSI general purpose display controller designed to interface to bargraph and numeric displays (vacuum fluorescent or LED).

The 10951 will drive 16-segment bargraph or seven-segment plus comma and decimal numeric displays with up to 16 display positions. The controller accepts command and data input words on a clocked serial input line. Commands control the on/off duty cycle, starting character position and number of characters to display. Encoded data words display bargraph position (single segment or increasing bar length), numbers, comma, decimal and selected upper and lower case letters. No external drive circuitry is required for displays that operate on 20 mA of drive current up to 50 volts. A 64 x 16-bit segment decoder provides character set decoding for the display.

ORDERING INFORMATION

Part Number	Package Type	Drive Voltage	Temperature Range (°C)
10951P-40	Plastic	40V	0 to +70
10951P-50	Plastic	50V	0 to +70
10951PE-40	Plastic	40V	−40 to +85
10951PE-50	Plastic	50V	−40 to +85

FEATURES

- 16 segment drivers plus decimal point and comma tail drivers
- 16 digit drivers
- Up to 66 kHz data rate
- Direct digit drive of 20 mA for up to 50 volt displays
- Supports vacuum fluorescent or LED displays
- Serial data input for 8-bit display and control data words
- 64 x 16-bit PLA provides data decoding driving
  - — Any 1 of 16 bargraph segments
  - — 1 to 16 bargraph segments
  - — Ten seven-segment numeric characters (0–9)
  - — Comma and decimal
  - — Eight upper and lower case seven-segment characters
- Command functions
  - — Duty cycle adjust
  - — Character position select
  - — Number of characters
- 40-Pin DIP package

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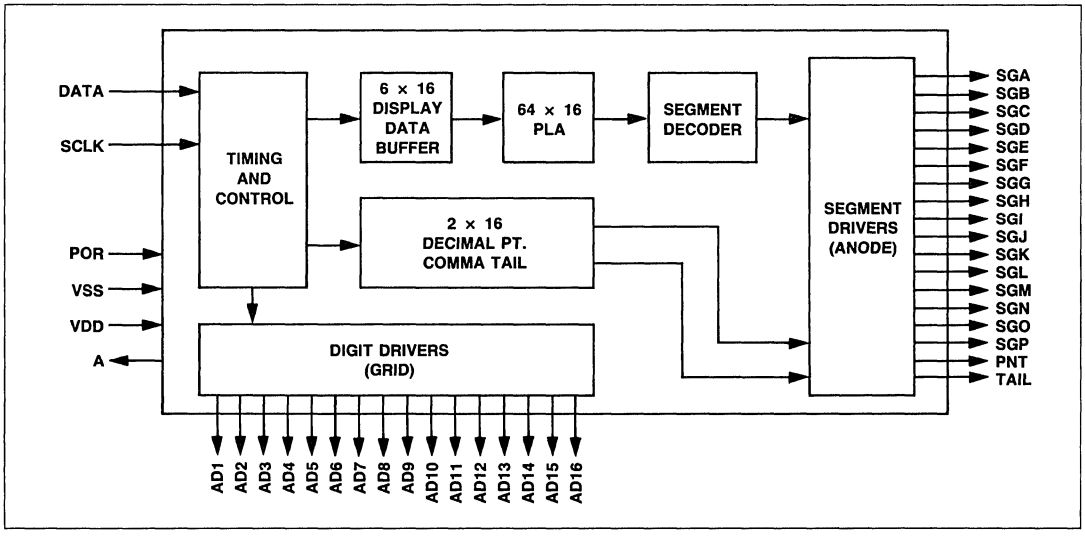
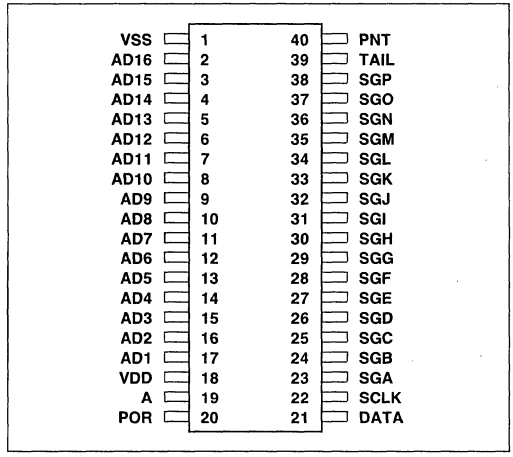


10951 Block Diagram

INTERFACE DESCRIPTION

10951 Pin Functions

Signal Name	Pin No.	Function
V_{SS}	1	Power and signal reference
AD16–AD1	2–17	Digits 16 through 1 driver outputs
V_{DD}	18	DC power connection
A	19	A clock output used for testing
POR	20	Power-on reset input
DATA	21	Serial data input
SCLK	22	Serial data clock input
SGA–SGP	23–38	Segments A through P driver outputs
TAIL	39	Comma tail driver output
PNT	40	Decimal point driver output



10951 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

All voltages are specified relative to V_{SS}.

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+0.3 to −20	V
Operating Current	I_{DD}	7	mA
Input Voltage	V_{IN}	+0.3 to −20	V
Output Voltage	V_{OUT}	+0.3 to −50	V
Output Current Digits	I_D	20	mA
Output Current Segments	I_S	10	mA
Operating Temperature			
Commercial	T_C	0 to +70	°C
Industrial	T_I	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	10	pF

***NOTE:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

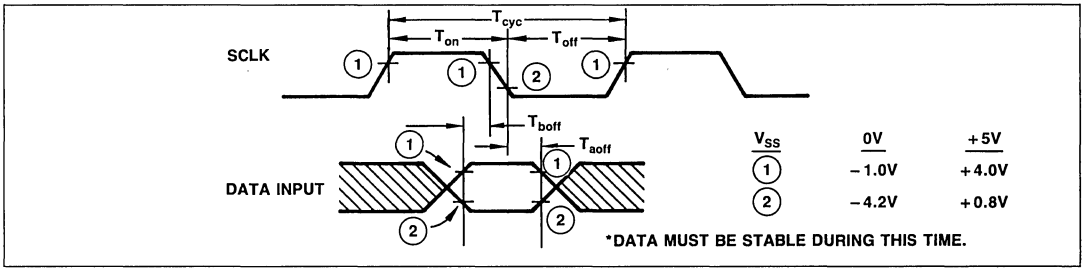
DC CHARACTERISTICS

Parameter	Limits (V_{SS} = 0) Min	Typ	Max	Limits (V_{SS} = +5V) Min	Typ	Max	Conditions	Unit
Supply Voltage (V_{DD})	−16.5	−15.0	−13.5	−11.5	−10.0	−8.5		V
Power Dissipation		40	100		40	100		mW
Input DATA,SCLK,								
Logic "1"	−1.0		+0.3	+4.0		+5.3		V
Logic "0"	V_{DD}		−4.2	V_{DD}		+0.8		
Input POR								
Logic "1"	−3.0		+0.3	+2.0		+5.3		
Logic "0"	V_{DD}		−10.0	V_{DD}		−5.0		
Output Digit and Segment Strobes Driver On								
Commercial			−1.5			+3.5	At 10 mA	V
Industrial			−1.7			+3.3		V
Driver Off 10951-40	−40		−35	−35		−30	Actual value determined by external circuit	V
Driver Off 10951-50	−50		−45	−45		−40		V
Output Leakage			10			10	Per driver at driver off	μA
Input Leakage			10			10		μA

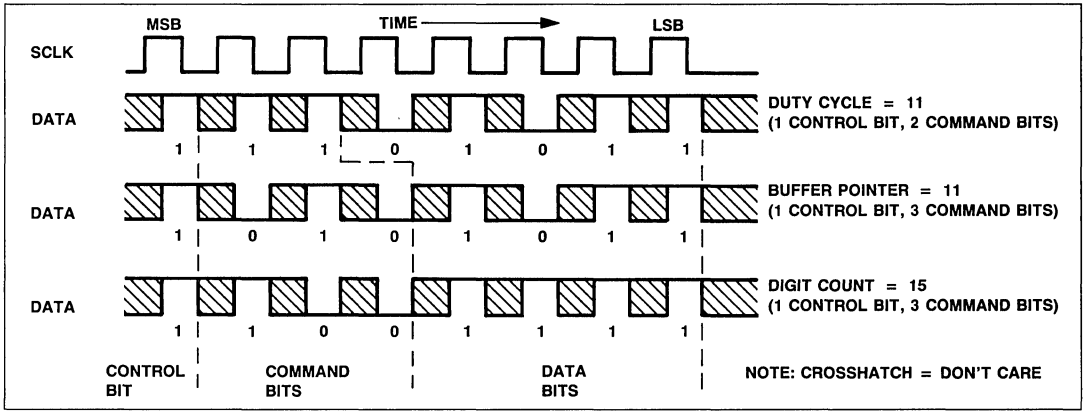
Note: All outputs require Pulldown Resistors.

AC CHARACTERISTICS

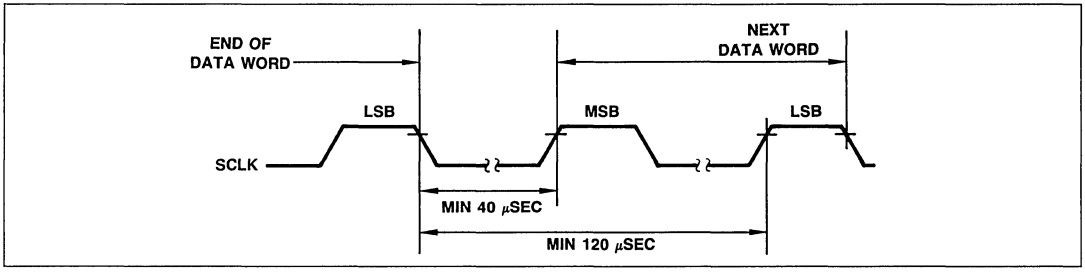
Parameter	Symbol	Min	Typ	Max	Unit
SCLK Clock					
On Time	T_{on}	1.0		20.0	μs
On Time	T_{off}	1.0			μs
Data Input Sample Time					
Before SCLK Clock Off	T_{boff}	200			ns
After SCLK Clock Off	T_{aoff}	100			ns



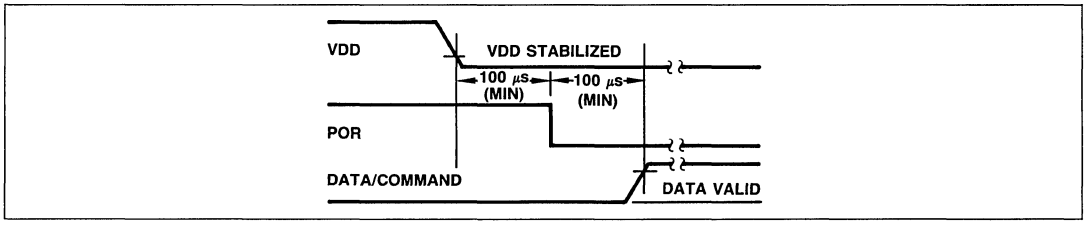
SCLK and Serial Data Timing



SCLK and Serial Data (Control Word) Examples



Data Word LSB/MSB Timing



Power-On Reset

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FUNCTIONAL DESCRIPTION

The 10951 receives commands and data on a serial input line clocked externally by a separate clock input line. The controller decodes the commands from control data words, decodes the data words in accordance with an internal 64 x 16-bit programmable logic array (PLA) and turns on and off segment and digit output drivers. The segment output patterns are controlled by the decoded data words while the digit output and segment output timing are controlled by the decoded control words. All timing signals required to control the display are generated in the 10951 device without any refresh input from the host processor.

Input data is loaded into the Display Data Buffer via the Serial Data Input (Data) channel. Internal timing and control blocks synchronize the segment and digit output signals to provide the proper timing for the multiplexing operation. The 16 x 64 PLA decodes 8-bit data words to drive the 16 segment, comma and decimal point drivers. The decoded data words will drive 16 segments to display bargaph patterns (single segment and multiple segment for increasing length displays) or seven-segment patterns to display numbers, selected upper and lower case letters, comma and decimal point.

Input data is loaded into the 10951 as a series of 8-bit words with the most significant bit (MSB), bit 7, first. If the MSB is a logic 1 (this bit is referred to as the control bit C), the loaded word is a control data word. If the C bit of any word is a logic 0, the loaded word is a display data word. The following paragraphs describe the format and functions of these control and display data words.

INPUT CONTROL DATA WORDS

When the C-Bit (bit 7) of the 8-bit input word is a logic 1, bits 5 and 6 are decoded into one of four control commands while data associated with the command are extracted from bits 0–4. There are four control codes which perform the following display functions:

- Load the Display Data Buffer pointer,
- Load the Digit Counter,
- Load the Duty Cycle register,
- Enable the Test Mode.

Table 1 lists the control codes and their functions.

Buffer Pointer Control

The Buffer Pointer Control code allows the Display Data Buffer pointer to be set to any digit position so that individual characters may be modified. The Buffer Pointer is loaded with a decimal equivalent value 2 less than the desired value (i.e., to point to the digit controlled by AD6 of the display, a value of 4 is entered). See Table 2 for a complete list of the Buffer Pointer values.

Digit Counter Control

The Digit Counter Control code is normally used only during initialization routines to define the number of character positions to be controlled. This code maximizes the duty cycle for any display. If 16 characters are to be controlled, enter a value of 0 (zero). Otherwise, enter the value desired.

Duty Cycle Control

The Duty Cycle Control code is used to turn the display on and off, and to adjust display brightness. As shown in the block diagram, the time slot for each character is 32 clock cycles. The segment and digit drivers for each character are on for a maximum of 31 cycles with a 1 cycle inter-digit off-time. The Duty Cycle Control code contains a 5-bit numeric field which modifies the on-time for the driver outputs from 0 to 31 cycles. A duty cycle of 0 puts both the segment and digit drivers into the off state. Figure 1 shows the timing characteristics for the segment outputs.

Test Mode Enable

The Test Mode Enable code is a device test function only. If executed, it will lock the device in the Test Mode. This mode can be disabled only by performing a power-on reset.

If this mode is activated, the digit time is reduced from 32 to 4 clock cycles to speed up the output driver sequencing time for ease in testing.

Table 1. Control Data Words

8-Bit Control Word		Function
C-Bit	7-Bit Code	
1	010NNNN[1]	Buffer Pointer Control (Position of character to be changed)
1	100NNNN[1]	Digit Counter Control (Number of characters to be output)
1	11NNNNN[2]	Duty Cycle Control (On/off and brightness control)
1	00NNNNN[3]	Test Mode Enable (Not a user function)

Note:
1. NNNN is a 4-bit binary value representing the digit number to be loaded.
2. NNNNN is a 5-bit binary value representing the number of clock cycles each digit is on.
3. This code is a device test function only. If executed it will lock the device in the Test Mode. Test Mode can be disabled only by performing a power-on reset.

Table 2. Buffer Pointer Control Codes

Hex Code	Pointer Value	Character Controlled By
A0	0	AD2
A1	1	AD3
A2	2	AD4
A3	3	AD5
A4	4	AD6
A5	5	AD7
A6	6	AD8
A7	7	AD9
A8	8	AD10
A9	9	AD11
AA	10	AD12
AB	11	AD13
AC	12	AD14
AD	13	AD15
AE	14	AD16
AF	15	AD1

INPUT DISPLAY DATA WORDS

Display data words are loaded as 8-bit format codes. There are 64 codes available (with the C-bit set to 0 to indicate a display data word).

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented before each data word is stored in the Display Buffer except for decimal point and comma words. The decimal point and comma words do not cause the Buffer Pointer to increment and thus are always associated with the previous character entered. To enter a character position out of the normal sequence, use the Buffer Pointer control command before entering the display data word. It is not necessary to use the Buffer Pointer control command to cycle back to position 1 when less than 16 character positions are being used (Digit Counter $\neq$ 0).

DIGIT DRIVERS (AD1–AD16)

The sixteen Digit Drivers (AD1 – AD16) are used to select each of the display digits sequentially during a refresh scan. Display segments will be illuminated when both the Digit Drivers and Segment Drivers for a particular character are energized simultaneously. The timing characteristics of both the digits and segments are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

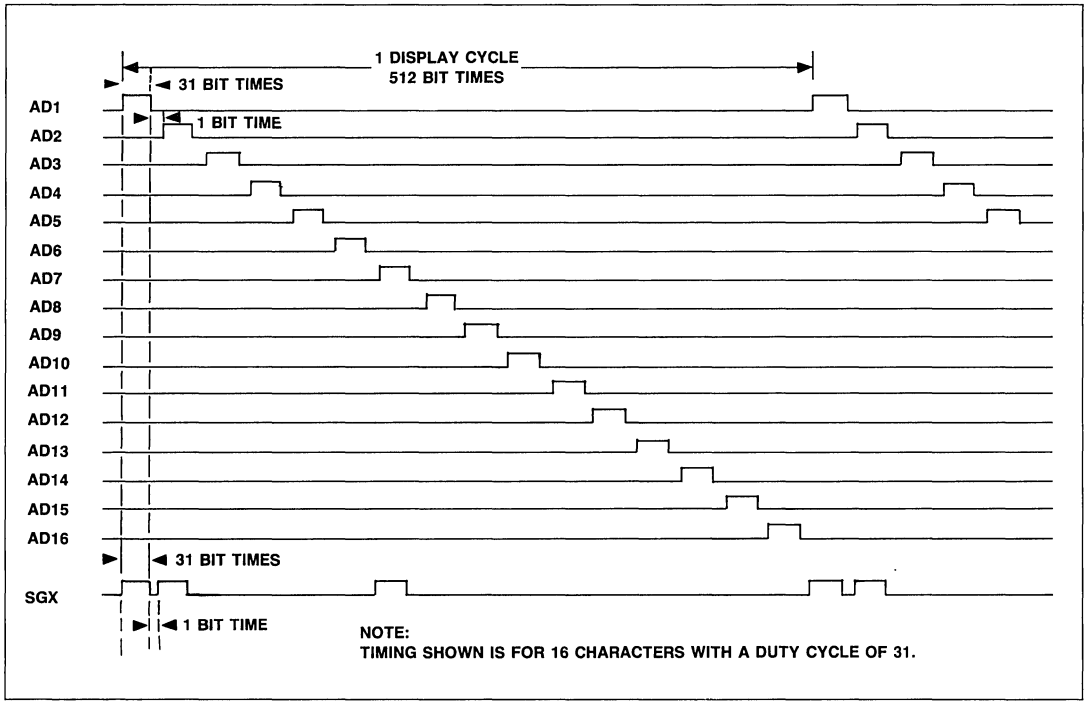

Figure 1. Display Scan Timing Diagram (Duty Cycle)

POWER-ON RESET (POR)

The Power-On Reset (POR) initializes the internal circuits of the 10951 when power (V_{DD}) is applied. The following conditions are established after a Power-On Reset:

a. The Digit Drivers (AD1-AD16) are in the off state (floating).
b. The Segment Drivers (SGA-SGP) are in the off state (floating). This includes PNT and TAIL.
c. The Duty Cycle is set to 0.
d. The Digit Counter is set to 16 (a bit code value of 0).
e. The Buffer Pointer points to the character controlled by AD1.

SEGMENT DRIVERS (SGA–SGP)

Sixteen (16) Segment Drivers are provided (SGA-SGP), plus the decimal point (PNT) and comma tail (TAIL). The segment, PNT and TAIL outputs are internally decoded from the 8-bit characters in the Display Data Buffer by means of a 64 x 16-bit PLA. The driver allocations for the 16-segment bargraph display and the seven-segment alphanumeric character plus comma and decimal point are shown in Figure 2. The input codes associated with seven-segment alphanumeric, comma and decimal point display are also shown in Figure 2. The complete set of 8-bit codes for the bargraph and alphanumeric display is shown in Table 3. Note that only segment drivers SGA-SGG are used to drive the seven-segment characters. Segment drivers SGH-SGP may be used for other purposes as decoded in accordance with Table 3. Figure 3 shows the total allocation of the 16-segment drivers as they would appear on a 7-segment display or a 16-segment bargraph display. Timing characteristics for the segment outputs are shown in Figure 1. See POR for the Power-On Reset state of these drivers.

TYPICAL SYSTEM HOOK-UP

Figure 4 shows the 10951 as it would be connected to a V-F display when driven by a host system. E_K is determined by the V-F display specifications and R_C is selected to provide proper biasing current for zeners. Pull down resistors R_A and R_G are determined by the interconnection capacitance between the 10951 and the display.

Table 3. 10951 Data Codes

Input Code								Function	Segment Driver Output Patterns (1 = On)																
7	6	5	4	3	2	1	0		SGA	SGB	SGC	SGD	SGE	SGF	SGG	SGH	SGI	SGJ	SGK	SGL	SGM	SGN	SGO	SGP	PNT	TAIL
0	X	0	0	0	0	0	0	Segment A On	1																	
0	X	0	0	0	0	0	1	Segment B On		1																
0	X	0	0	0	0	1	0	Segment C On			1															
0	X	0	0	0	0	1	1	Segment D On				1														
0	X	0	0	0	1	0	0	Segment E On					1													
0	X	0	0	0	1	0	1	Segment F On						1												
0	X	0	0	0	1	1	0	Segment G On							1											
0	X	0	0	0	1	1	1	Segment H On								1										
0	X	0	0	1	0	0	0	Segment I On									1									
0	X	0	0	1	0	0	1	Segment J On										1								
0	X	0	0	1	0	1	0	Segment K On											1							
0	X	0	0	1	0	1	1	Segment L On												1						
0	X	0	0	1	1	0	0	Segment M On													1					
0	X	0	0	1	1	0	1	Segment N On														1				
0	X	0	0	1	1	1	0	Segment O On															1			
0	X	0	0	1	1	1	1	Segment P On																1		
0	X	0	1	0	0	0	0	Segment A On	1																	
0	X	0	1	0	0	0	1	Segments A&B On	1	1																
0	X	0	1	0	0	1	0	Segment A-C On	1	1	1															
0	X	0	1	0	0	1	1	Segment A-D On	1	1	1	1														
0	X	0	1	0	1	0	0	Segment A-E On	1	1	1	1	1													
0	X	0	1	0	1	0	1	Segment A-F On	1	1	1	1	1	1												
0	X	0	1	0	1	1	0	Segment A-G On	1	1	1	1	1	1	1											
0	X	0	1	0	1	1	1	Segment A-H On	1	1	1	1	1	1	1	1										
0	X	0	1	1	0	0	0	Segment A-I On	1	1	1	1	1	1	1	1	1									
0	X	0	1	1	0	0	1	Segment A-J On	1	1	1	1	1	1	1	1	1	1								
0	X	0	1	1	0	1	0	Segment A-K On	1	1	1	1	1	1	1	1	1	1	1							
0	X	0	1	1	0	1	1	Segment A-L On	1	1	1	1	1	1	1	1	1	1	1	1						
0	X	0	1	1	1	0	0	Segment A-M On	1	1	1	1	1	1	1	1	1	1	1	1	1					
0	X	0	1	1	1	0	1	Segment A-N On	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
0	X	0	1	1	1	1	0	Segment A-O On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
0	X	0	1	1	1	1	1	Segment A-P On	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
0	X	1	0	0	0	0	0	Number 0	1	1	1	1	1	1		1	1	1	1	1						
0	X	1	0	0	0	0	1	Number 1		1	1					1	1	1	1	1						
0	X	1	0	0	0	1	0	Number 2	1	1		1	1		1	1	1	1	1	1						
0	X	1	0	0	0	1	1	Number 3	1	1	1	1			1	1	1	1	1	1						
0	X	1	0	0	1	0	0	Number 4		1	1			1	1	1	1	1	1	1						
0	X	1	0	0	1	0	1	Number 5	1		1	1		1	1	1	1	1	1	1						
0	X	1	0	0	1	1	0	Number 6	1		1	1	1	1	1	1	1	1	1	1						
0	X	1	0	0	1	1	1	Number 7	1	1	1			1	1	1	1	1	1	1						
0	X	1	0	1	0	0	0	Number 8	1	1	1	1	1	1	1	1	1	1	1	1						
0	X	1	0	1	0	0	1	Number 9	1	1	1	1		1	1	1	1	1	1	1						
0	X	1	0	1	0	1	0	Letter P	1	1			1	1	1						1	1	1	1		
0	X	1	0	1	0	1	1	Letter L				1	1	1							1	1	1	1		
0	X	1	0	1	1	0	0	Semicolon								1	1	1	1	1					1*	1*
0	X	1	0	1	1	0	1	Blank								1	1	1	1	1						
0	X	1	0	1	1	1	0	Decimal													1	1	1	1	1**	
0	X	1	0	1	1	1	1	Blank													1	1	1	1		
0	X	1	1	0	0	0	0	Number 0	1	1	1	1	1	1							1	1	1	1		
0	X	1	1	0	0	0	1	Number 1		1	1										1	1	1	1		
0	X	1	1	0	0	1	0	Number 2	1	1		1	1		1						1	1	1	1		
0	X	1	1	0	0	1	1	Number 3	1	1	1	1			1						1	1	1	1		
0	X	1	1	0	1	0	0	Number 4		1	1			1	1						1	1	1	1		
0	X	1	1	0	1	0	1	Number 5	1		1	1		1	1						1	1	1	1		
0	X	1	1	0	1	1	0	Number 6	1		1	1	1	1	1						1	1	1	1		
0	X	1	1	0	1	1	1	Number 7	1	1	1			1							1	1	1	1		
0	X	1	1	1	0	0	0	Number 8	1	1	1	1	1	1	1						1	1	1	1		
0	X	1	1	1	0	0	1	Number 9	1	1	1	1		1	1						1	1	1	1		
0	X	1	1	1	0	1	0	Letter A	1	1	1		1	1	1						1	1	1	1		
0	X	1	1	1	0	1	1	Letter b			1	1	1	1	1						1	1	1	1		
0	X	1	1	1	1	0	0	Letter C	1			1	1	1							1	1	1	1		
0	X	1	1	1	1	0	1	Letter d		1	1	1	1		1						1	1	1	1		
0	X	1	1	1	1	1	0	Letter E	1			1	1	1	1						1	1	1	1		
0	X	1	1	1	1	1	1	Letter F	1				1	1	1						1	1	1	1		

Any 1 of 16 Segments

Bargraph Codes

1 to 16 Segments

Alphanumeric and Special Codes

Notes:

* Sets comma and decimal outputs for last character entered.

** Sets decimal output for last character entered.

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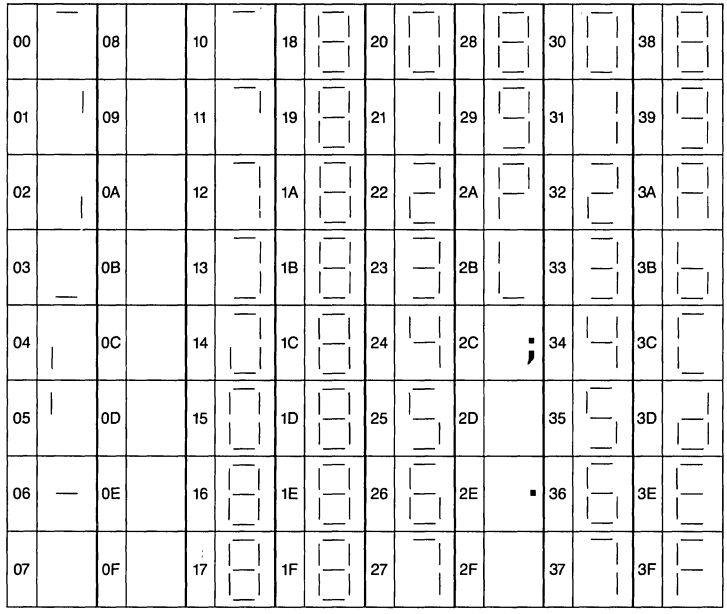

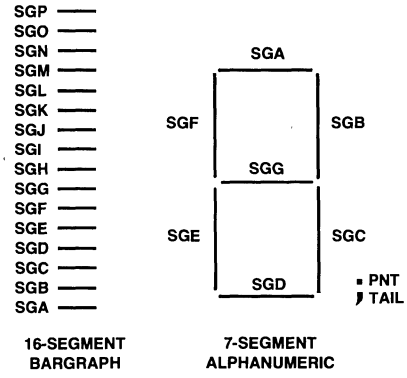

Figure 2. Segment Allocation and 7-Segment Alphanumeric Codes

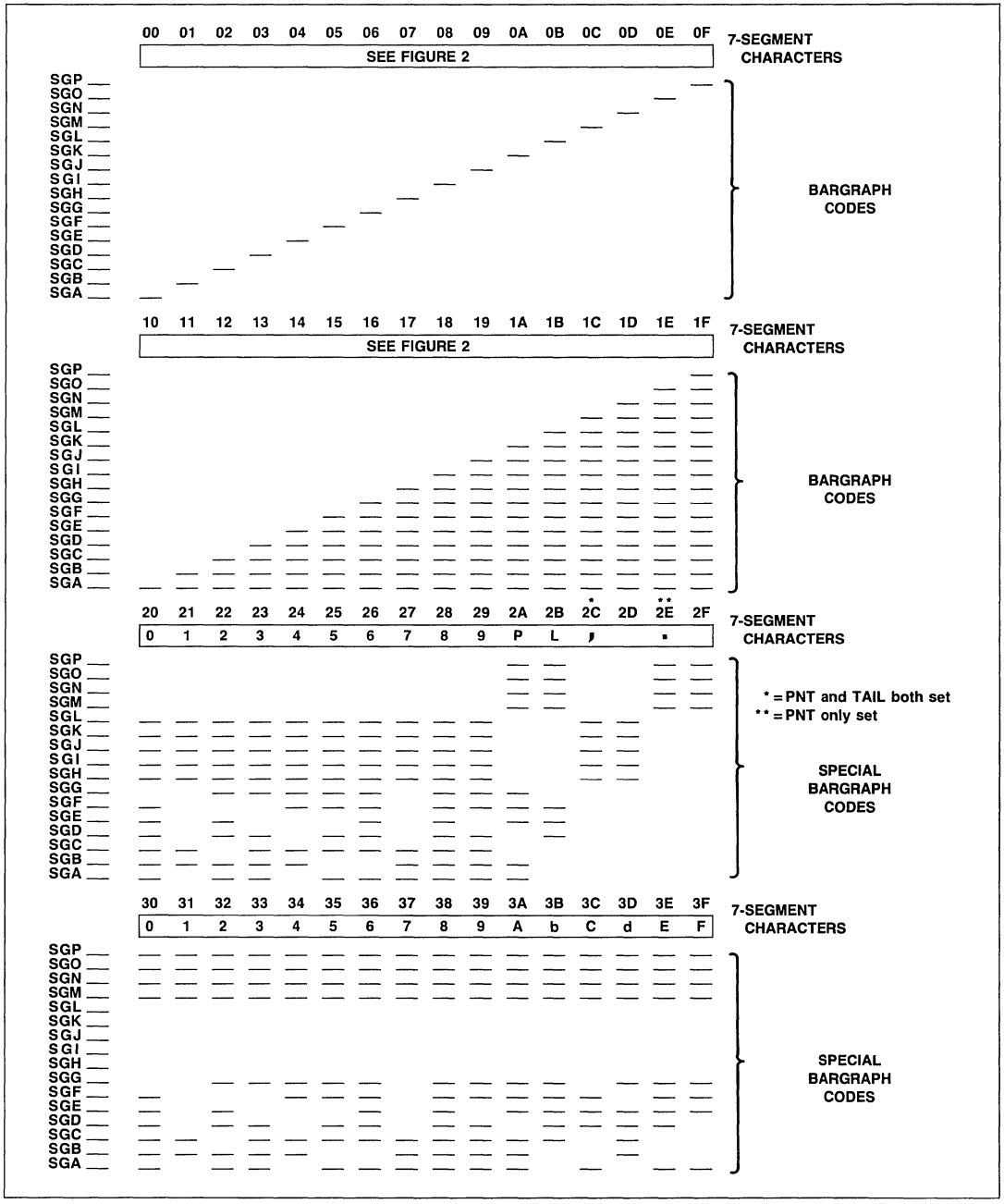

Figure 3. Total Character Allocation for Bargraph or 7-Segment Displays

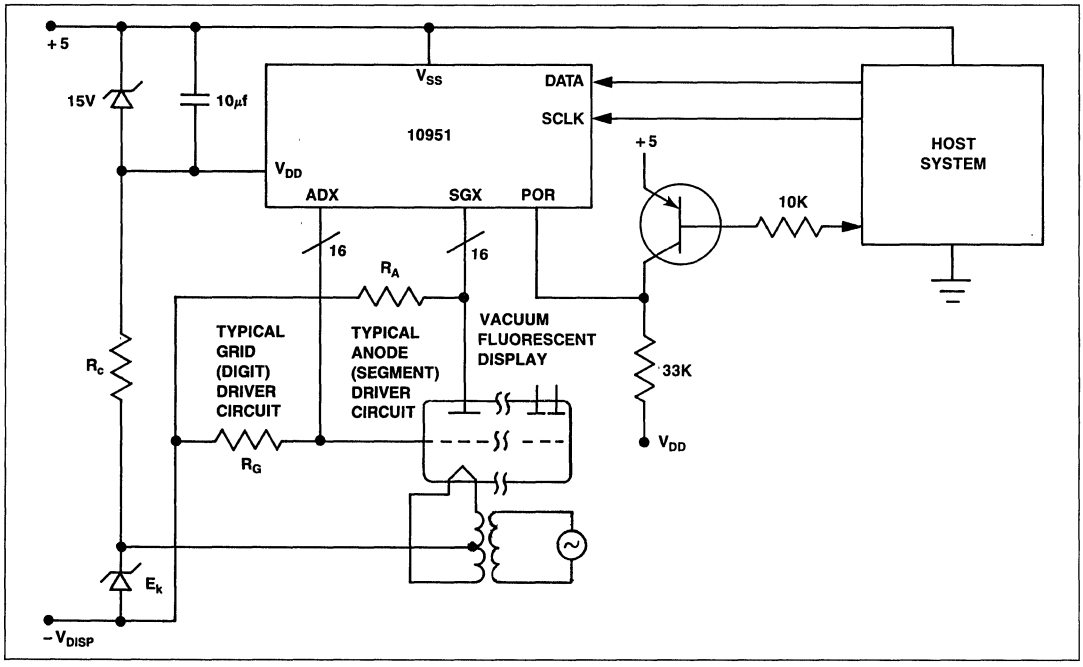

Figure 4. Partial System Schematic