Rockwell

10955
Segmented Display Controller/Driver

DESCRIPTION

The 10955 Segmented Display/Driver is a MOS/LSI device capable of directly driving both the grids and anodes of multiplexed vacuum-fluorescent segmented displays. All timing circuits (including a clock generator) required to control the display drivers are contained within the device. The 10955 can drive segmented displays with 8 or 16 grids (characters) and 8, 16, or 24 anodes (segments). A serial interface allows for a host microprocessor to transmit commands and display data to the 10955 directly.

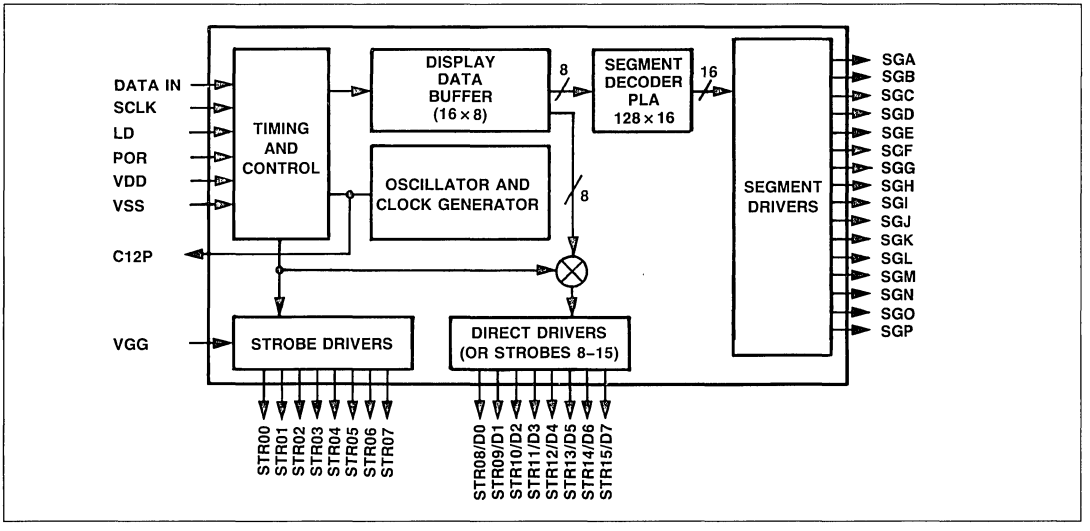
A 128 x 16 bit PLA provides coding for both 16-segment and 14-segment alphanumeric ASCII code character sets (all caps only). The PLA is divided into lower 64 and upper 64 code sets. Only one set can be selected at a time. In lower set mode the 16-segment display characters are selected. In upper set mode the 14-segment display characters are selected. The PLA can also be bypassed so that data words from the host microprocessor are loaded directly into segment drivers without decoding by the PLA. This mode is especially useful for creating special display patterns such as bar graph displays. Bypass mode is limited to eight drivers per data word.

FEATURES

- 8- or 16-character display driver
- 8-, 16-, or 24-segment drivers
- Average data rate 66 kHz
- Single character burst rate 500 kHz
- Direct digit drive of 20 ma for up to 40 or 50 volt vacuum-fluorescent serial displays
- 128 x 16-bit PLA provides 16- or 14-segment alpha-numeric character set
- Internal clock generator circuit
- Serial host interface
- PLA bypass mode
- 40-pin DIP

ORDERING INFORMATION

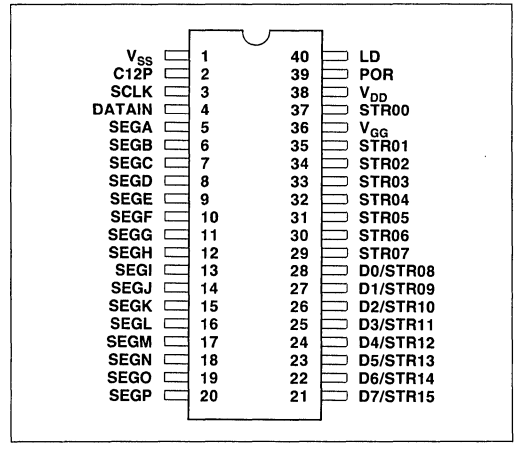
Part Number	Package Type	Drive Voltage	Temperature Range (°C)
10955P-40	Plastic	40V	0 to +70
10955P-50	Plastic	50V	0 to +70
10955PE-40	Plastic	40V	−40 to +85
10955PE-50	Plastic	50V	−40 to +85



10955 Block Diagram

INTERFACE DESCRIPTION

Signal Name	Pin No.	Function
V_{SS}	1	Power and signal reference
C12P	2	Test clock—factory test
SCLK	3	Serial input data clock
DATAIN	4	Serial data input
SEGA-SEGP	5–20	Segments A through P driver outputs
D7/STR15–D0/STR08	21–28	Direct segment outputs or strobe outputs
STR07–STR00	29–35, 37	Strobe outputs
V_{GG}	36	Display voltage
V_{DD}	38	Logic supply voltage
POR	39	Power on reset
LD	40	Data Load Strobe



10955 Pin Configuration

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

All voltages are specified relative to V_{SS}.

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+0.3 to −25	V
Operating Current	I_{DD}	8	mA
Input Voltage	V_{IN}	+0.3 to −25	V
Display Voltage	V_{GG}	+0.3 to −50	V
Operating Temperature			
Commercial	T_C	0 to +70	°C
Industrial	T_I	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C
Input Capacitance	C_{IN}	5	pF
Output Capacitance	C_{OUT}	10	pF

***Note:** Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{DD} = −18.0 to −22.0 Vdc, V_{SS} = 0 Vdc, TA = 0°C to +70°C (commercial) or −40°C to +85°C (industrial), unless otherwise noted. All voltages referenced to V_{SS}.)

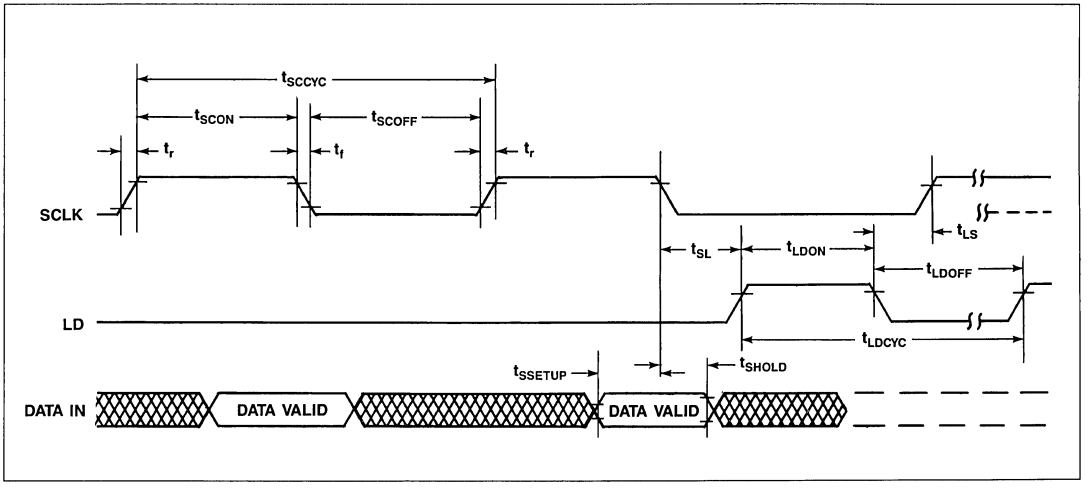
Parameter	Symbol	Min.[4]	Typical[3]	Max.[4]	Unit
Operating Current, Logic	I_{DD}				mA
Commercial		—	3.2	6.4	
Industrial		—	4.0	8.0	
Operating Current Display	I_{GG}				
1 strobe plus 24 segments @ V_{OH}					
Commercial		—	—	6.5	mA
Industrial		—	—	8.0	mA
1 strobe plus 16 segments @ V_{OH}					
Commercial		—	—	4.3	mA
Industrial		—	—	5.3	mA
All display drivers					
@ V_{GG} and 85°C		—	—	320	μA
Display Voltage	V_{GG}				V
10955-40		−40.0	—	—	
10955-50		−50.0	—	—	
Input Leakage (at −20V)	I_{IL}	—	—	10	μA
Input (DATAIN, LD, SCLK)					V
Logic "1"	V_{IH}	−1.2	−0.5	+0.3	
Logic "0"	V_{IL}	V_{DD}	−6.0	−4.2	
Input POR					V
Logic "1"	V_{IHPO}	−3.0	—	+0.3	
Logic "0"	V_{ILPO}	V_{DD}	−12.0	−10.0	
Output (C12P)					V
Logic "1"	V_{OHSY}	−0.7	—	+0.3	
Logic "0"[1]	V_{OLSY}	V_{DD}		—	
Output (Strobe STR00–07, D0–D7, SGA–SGP)					V
Logic "1" (I_{Load} = 10 mA)	V_{OH}	−1.5	−1.0	V_{SS}	
Logic "1" (I_{Load} = 20 mA)[2]	V_{OH}	—	−2.0	V_{SS}	
Logic "0" (I_{Load} = 0 mA)	V_{OL}	V_{GG}	0.5 + V_{GG}	0.95 × V_{GG}	

Notes:
1. Open drain driver. Requires external pull-down resistor for testing only.
2. STR00–STR07 only (also for D0–D7 when used as character drivers)
3. Typical measured at V_{DD} = 20.0V and Y_A = 25°C.
4. Max. values are most positive limits. Min. values are most negative limits.

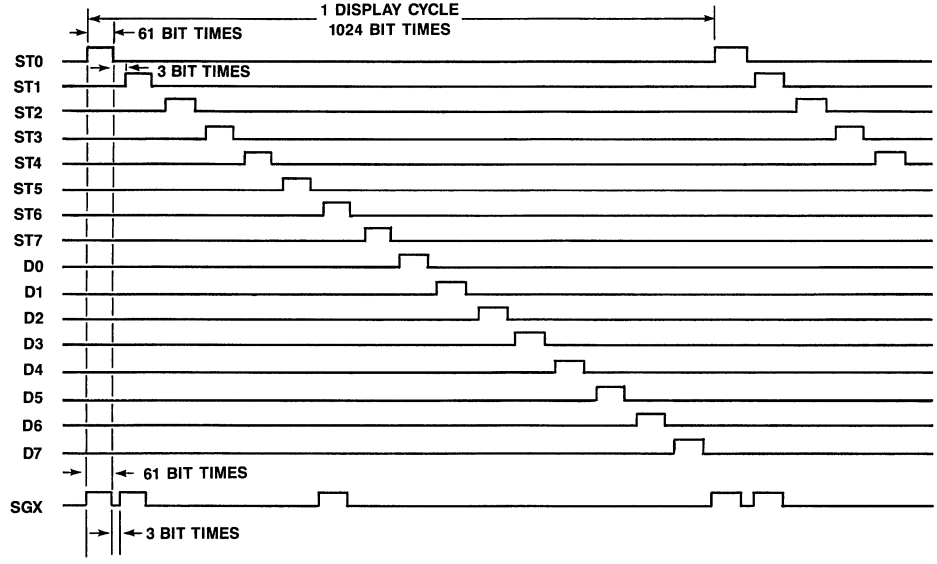
AC CHARACTERISTICS

Characteristic	Symbol	Min.	Max.	Unit
Clock Timing Cycle Time	t_{CYC}			
Commercial		6.66	23.0	usec
Industrial		5.88	24.0	usec
HOST INTERFACE TIMING				
Serial Clock (SCLK)				
On Time	t_{SCON}	1.2	40.0	usec
Off Time	t_{SCOFF}	1.0	—	usec
Cycle Time	t_{SCCYC}	2.2	—	usec
Serial Data (DATAIN)				
Set-up Time	t_{SSETUP}	400	—	nsec
Hold Time	t_{SHOLD}	400	—	nsec
Serial Clock to LD Time	t_{SL}	600	—	nsec
LD to Serial Clock	t_{LS}	400	—	nsec
Data Load (LD)				
On Time	t_{LDON}	1.0	—	usec
Off Time (Commercial	t_{LDOFF}	46.0	—	usec
Off Time (Industrial)	t_{LDOFF}	48.0	—	usec
Cycle Time (Commercial)	t_{LDCYC}	69.0	—	usec
Cycle Time (Industrial)	t_{LDCYC}	72.0	—	usec

Note:
t_r and t_f = rise and fall time of clocking signals which are 10 to 30 nsec.



Serial Interface Timing Waveforms



Notes:
1. t_{CYC} = 2 bit times.
2. Timing shown is for 16 characters with a duty cycle of 61.

Display Scan Timing Diagram

FUNCTIONAL DESCRIPTION

All timing signals required to control the display are generated by the 10955 device after the display buffer and control registers have been loaded from the host processor. In the following functional description, refer to the 10955 block diagram.

Input data is loaded into the Display Data Buffer via the serial data input channel. Internal timing and control logic synchronize the digit output signals with the segment output signals to provide the proper timing for the multiplexing operation. The segment decoding is performed in a 128 x 16 PLA character code set.

CHARACTER DRIVERS (STR00-STR07)

The eight character (grid) drivers are used to select the display character positions sequentially during a refresh scan. Display characters are illuminated when the character driver for a particular character position and the segment (anode) drivers are energized simultaneously.

DISCRETE DRIVERS (D0-D7)

The function of these eight drivers depends on the display mode. In some modes these drivers act as segment (anode) drivers loaded directly from the Data Buffer (RAM). In other modes these drivers are used as extra character (grid) drivers (STR8-STR15). See Display Modes for further discussion of these driver functions.

SEGMENT DRIVERS (SGA-SGP)

Depending on the display mode, the sixteen segment drivers are loaded through an 8 x 16 PLA decoder or directly from the Data Buffer RAM.

SYSTEM CLOCK

Each 10955 device has its own on-board oscillator and clock generator.

POWER-ON RESET

The Power-On Reset (POR) input initializes the internal circuits of the 10955. This is normally performed when power (VDD) is applied. The following conditions are established by application of POR:

a. The grid and anode drivers (STR00-STR07, D0-D7, and SGA-SGP) are in the off state.

b. Duty Cycle register is set to zero.
c. The Digit Counter is set to 32 digits.
d. The Buffer Pointer is set to zero.
e. The Digit Time is set to 64.
f. The PLA Bypass/Sixteen Digit display mode is set.

At power on, the 10955 is held in an internal halt mode. This allows the host system to load the control registers and the data buffer without flashing invalid data on the display.

During the initial rise time of VDD at power turn-on, the magnitude of VGG should not exceed the magnitude of VDD.

HOST SYSTEM INTERFACE

Input data is loaded into the 10955 via a serial data input channel as a series of nine-bit words.

After nine bits of data (with the most significant bit first) have been shifted into the data buffer, a pulse on the LD signal loads the data into an internal buffer and informs the 10955 that a new data word is available. After the LD pulse, a new data word may be shifted in while the 10955 is processing the first word.

The following sections describe the format and functions of the input words which may contain either control data or display data.

Display Data Words

Display data words are loaded as nine bit codes. The lower eight bits (7-0) are data. The ninth bit (the most significant) is always a zero (0).

Sixteen display data words must be entered to completely load the Display Data Buffer. The Buffer Pointer is automatically incremented after each data word is stored in the buffer. The Buffer Pointer will automatically reset to character position 0 when its value is equal to the programmed digit count value. The Buffer Pointer may be set to any desired value with the Buffer Pointer Control Word. This permits arbitrary loading of the Display Data Buffer.

Control Words

Control words are distinguished from display words by the fact that the most significant bit is always a one. Control words and their functions are defined below.

8	7	6	5	4	3	2	1	0	BIT
			DATA						DUTY CYCLE, DIGIT COUNT, BUFFER POINTER
1	CODE			PLA MODE		CONFIG.	DIGIT TIME		← CONTROL REGISTER
	0	1	X	X	X	X	X	X	DUTY CYCLE CONTROL
	1	0	0	X	X	X	X	X	DIGIT COUNT CONTROL
	1	1	0	0	X	X	X	X	BUFFER POINTER CONTROL
	0	0	0	X	X	X	X	X	CONTROL REGISTER
									(5 bits coded as shown below)
	0	0	0	X	X	Y	0	0	64 cycles per grid
	0	0	0	X	X	Y	0	1	16 cycles per grid
	0	0	0	X	X	Y	1	0	32 cycles per grid
	0	0	0	X	X	Y	1	1	8 cycles per grid
	0	0	0	X	X	0	Z	Z	16 digit configuration
	0	0	0	X	X	1	Z	Z	8 digit and two output
	0	0	0	0	0	Y	Z	Z	PLA bypass
	0	0	0	0	1	Y	Z	Z	Reserved for upgrade
	0	0	0	1	0	Y	Z	Z	Lower 64 PLA (64U)
	0	0	0	1	1	Y	Z	Z	Lower 64 PLA (64L)

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Buffer Pointer

The Buffer Pointer Control code sets the Display Data Buffer Pointer. The five least significant bits of the code are loaded into the Buffer Pointer to select the character position as shown in Table 1.

Table 1. Load Buffer Pointer Codes

Load Code Value	Pointer Value	Character Position Selected
C0	00	0
C1	01	1
C2	02	2
C3	03	3
C4	04	4
C5	05	5
C6	06	6
C7	07	7
C8	08	8
C9	09	9
CA	0A	10
CB	0B	11
CC	0C	12
CD	0D	13
CE	0E	14
CF	0F	15

Note: D0–DF (Not Used)

Digit Count Control

The Digit Count Control command defines the number of character positions (grids) to be controlled. This code is normally used only during initialization routines, but it may also be used in conjunction with the Duty Cycle Control code to extend the range of brightness control. Strobing begins at character position 0 and proceeds thru the last position specified. If more than 16 grids are selected (17–32), extra time slots are generated for these phantom strobes. When the phantom strobes are active, strobes 0 through 15 are off so the displayed data is not affected although the duty cycle is decreased as each phantom strobe is added. The code, digit count value, and number of grids controlled by the Digit Counter are shown in Table 2.

Table 2. Load Digit Counter Control Codes

Code	Digit Counter Value	No. of Grids Controlled
80	00	32
81	01	1
82	02	2
83	03	3
84	04	4
85	05	5
86	06	6
87	07	7
88	08	8
89	09	9
8A	0A	10
8B	0B	11
8C	0C	12
8D	0D	13
8E	0E	14
8F	0F	15
90	10	16
91	11	17
92	12	18
93	13	19
94	14	20
95	15	21
96	16	22
97	17	23
98	18	24
99	19	25
9A	1A	26
9B	1B	27
9C	1C	28
9D	1D	29
9E	1E	30
9F	1F	31

Duty Cycle

The Duty Cycle Control code is used to turn on and off the display, to adjust display brightness, or to modify display timing. The time slot for each character is 8, 16, 32, or 64 internal cycles (an internal cycle = 1/2 t_{CYC} as selected by the Digit Time codes in the control register. The segment and digit drivers for each character may be turned on for a maximum of 5, 13, 29, or 61 cycles with a 3 cycle mandatory inter-digit off time. The lower six bits of the Duty Cycle Control code are loaded into the Duty Cycle Register. Resultant duty cycles (on-times and off-times) are shown in Table 3.

Table 3. Duty Cycle Control Codes

	Digit Time = 8		Digit Time = 16		Digit Time = 32		Digit Time = 64	
Code	On	Off	On	Off	On	Off	On	Off
40	—	8	—	16	—	32	—	64
41	—	8	—	16	—	32	—	64
42	—	8	—	16	—	32	—	64
43	1	7	1	15	1	31	1	63
44	2	6	2	14	2	30	2	62
45	3	5	3	13	3	29	3	61
46	4	4	4	12	4	28	4	60
47	5	3	5	11	5	27	5	59
48	5	3	6	10	6	26	6	58
49	5	3	7	9	7	25	7	57
4A	5	3	8	8	8	24	8	56
4B	5	3	9	7	9	23	9	55
4C	5	3	10	6	10	22	10	54
4D	5	3	11	5	11	21	11	53
4E	5	3	12	4	12	20	12	52
4F	5	3	13	3	13	19	13	51
50	5	3	13	3	14	18	14	50
51	5	3	13	3	15	17	15	49
52	5	3	13	3	16	16	16	48
53	5	3	13	3	17	15	17	47
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
5B	5	3	13	3	25	7	25	39
5C	5	3	13	3	26	6	26	38
5D	5	3	13	3	27	5	27	37
5E	5	3	13	3	28	4	28	36
5F	5	3	13	3	29	3	29	35
60	5	3	13	3	29	3	30	34
61	5	3	13	3	29	3	31	33
62	5	3	13	3	29	3	32	32
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
7C	5	3	13	3	29	3	58	6
7D	5	3	13	3	29	3	59	5
7E	5	3	13	3	29	3	60	4
7F	5	3	13	3	29	3	61	3

Control Register

There is a 5-bit control register, which can be loaded by the control word, 000XXYZZ. The lower 5 bits of this control word are loaded into the control register.

The least significant two bits of the control register set the total Digit Time for each character during the refresh cycle. Four values can be set using the codes, 8, 16, 32, or 64 cycles per grid. The default value set at power-on is 64 cycles per grid. Under conditions where the display can be subjected to quick movements during viewing (e.g. portable or vehicle mounted applications) it may be necessary to increase the refresh rate by selecting 8, 16 or 32 cycles per grid with the appropriate control codes.

The middle bit of the 5 bit control register determines the sixteen digit or eight digit configurations. The two most significant bits select one of the four PLA Modes.

DISPLAY MODES

The 10955 can operate in any of eight display modes which control the maximum number of active strobes and segments and the manner in which the RAM Data Buffer is decoded onto the segment drivers.

16 Digit Configuration

If the third bit of the control register is zero or is reset by the POR signal, the 16 digit configuration is selected. In this case, a maximum of 16 segments and 16 strobes are provided. The 16 words in the RAM Data Buffer correspond to the 16 strobes. The 8 data bits of each word are sent to the PLA for decode.

8 Digit Configuration

If the third bit of the control register is a one, the 10955 is configured into the 8 digit mode. In this case, a maximum of 8 strobes and 24 segments are allowed. The 8-bit words in the RAM Data Buffer are grouped into 8 word pairs which correspond to strobes STR0–STR7: 0-1, 2-3, 4-5, 6-7, 8-9, 10-11, 12-13, and 14-15. The data in the even-numbered word of each pair is loaded into the direct-output segment drivers (D0–D7). The data in the odd-numbered word of each pair is decoded in the segment PLA decoder before being loaded into the 16-segment output drivers (SGA–SGP).

PLA Bypass Mode

If both of the most significant bits of the control register are zero, the PLA Bypass Mode is selected. In this mode, the PLA is bypassed. Each data word is loaded directly into the segment drivers without being decoded by the PLA. Since there are only 8 data bits but 16 drivers, each data bit is loaded into two adjacent drivers which can be connected externally to provide twice the current drive of an individual driver. The data bits/segments selection allocation is as follows:

Data bit	7	6	5	4	3	2	1	0
Segments	O,P	M,N	K,L	I,J	G,H	E,F	C,D	A,B

Upper 64 PLA Mode (64U)

In this mode (bit 5 = 1, bit 4 = 0) the Upper 64 out of the 128 codes are used, (i.e., 64 to 127). Since 64 codes can be specified by a 6-bit word, the most significant two bits of the 8-bit word from the RAM are not used. However, the most significant two bits of the display data are brought out directly to SEGO and SEGP outputs. Therefore, the 64 codes can be decoded to the 16-segment outputs, or only 14-segment outputs leaving two for direct output from the RAM.

Lower 64 PLA Mode (64L)

This mode (bit 5 = 1, bit 4 = 1) is similar to the Upper 64 PLA Mode, but only the lower 64 codes (0–63) out of the 128 codes are used. The 64L and 64U PLA modes allow two independent sets of 64 codes to be programmed into one chip. In running the display, only one set can be selected at a time.

Fourth PLA Mode

A fourth PLA mode is reserved for future expansion of the 10955. This code (bit 5 = 0, bit 4 = 1) should not be used. Selecting this PLA mode may result in non-defined characters appearing on the display.

PLA CHARACTER SET CODES

Figure 1 shows the 16-segment and 14-segment driver assignments for the corresponding segmented displays. Figure 2 shows the 16-segment and 14-segment PLA character set patterns coded into the 10955.

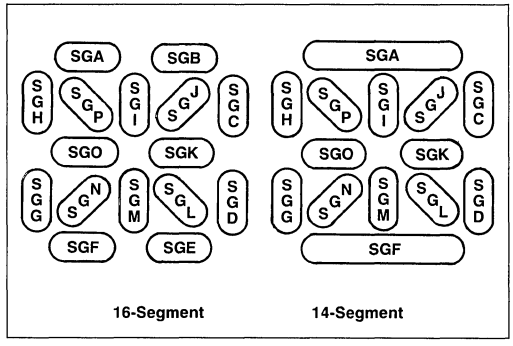
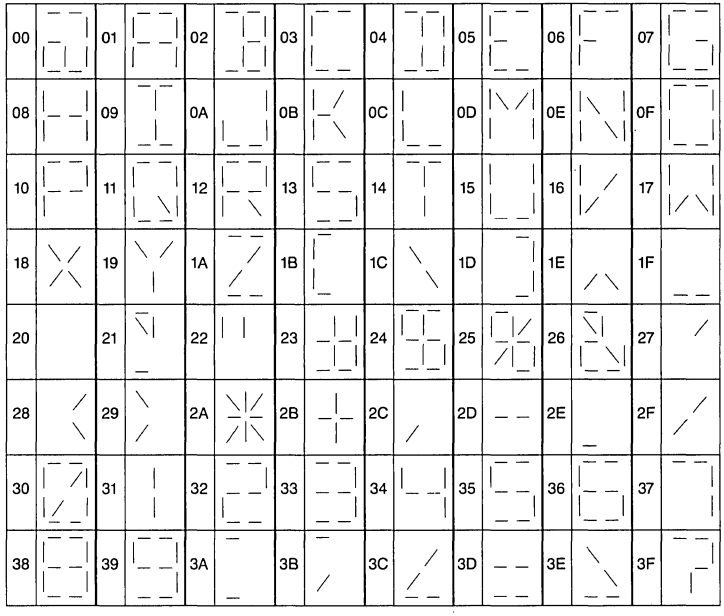
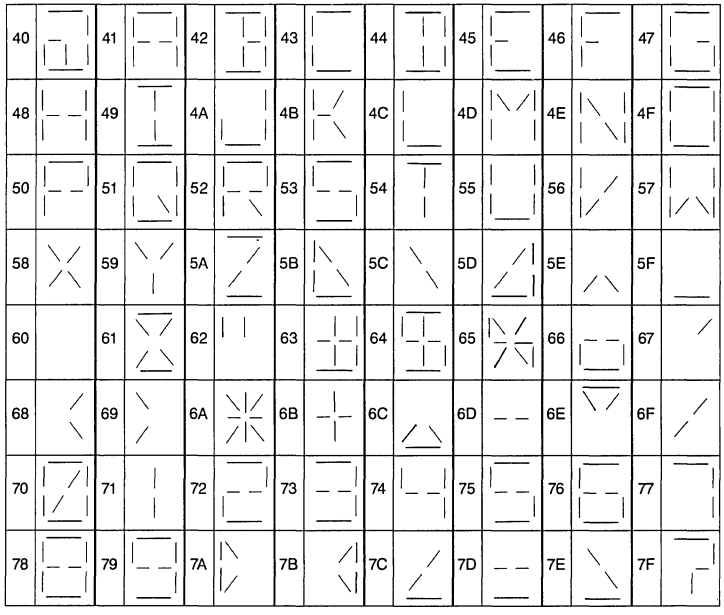


Figure 1. Segment Driver Assignments



16-Segment PLA Patterns

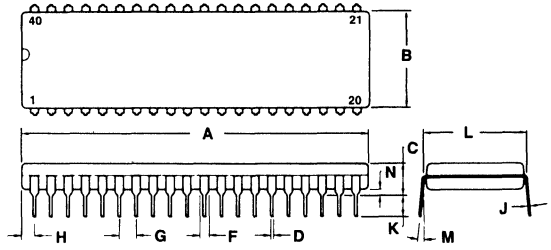


14-Segment PLA Patterns

Figure 2. 16- and 14-Segment PLA Character Sets

PACKAGE DIMENSIONS

40-PIN PLASTIC DIP



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.28	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	3.55	5.08	0.140	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.30	4.32	0.130	0.170
L	15.24 BSC		0.600 BSC	
M	7°	10°	7°	10°
N	0.51	1.02	0.020	0.040