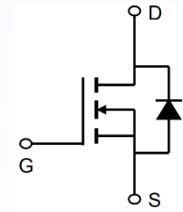


650V N-Channel Enhancement Mode MOSFET

Description

The 10N65F/P is silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.



General Features

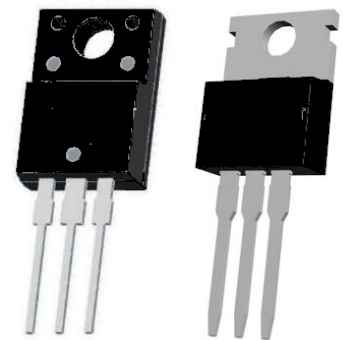
$V_{DS} = 650V$ $I_D = 10A$

$R_{DS(ON)} < 0.9\Omega$ @ $V_{GS}=10V$ (Type: 0.75Ω)

Application

Uninterruptible Power Supply(UPS)

Power Factor Correction (PFC)



Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Value		Unit
		TO-220F	TO-220	
V_{DSS}	Drain-Source Voltage ($V_{GS} = 0V$)	650		V
I_D	Continuous Drain Current	10		A
I_{DM}	Pulsed Drain Current (note1)	58		A
V_{GS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulse Avalanche Energy (note2)	426		mJ
I_{AR}	Avalanche Current (note1)	9		A
E_{AR}	Repetitive Avalanche Energy note1)	41		mJ
P_D	Power Dissipation ($T_C = 25^\circ C$)	32.1		W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55~+150		$^\circ C$
R_{thJC}	Thermal Resistance, Junction-to-Case	4.46		$^\circ C/W$
R_{thJA}	Thermal Resistance, Junction-to-Ambient	46.7		$^\circ C/W$

650V N-Channel Enhancement Mode MOSFET
Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	650	685	--	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = 650V, V _{GS} = 0V, T _J =25°C	--	--	1	μA
IGSS	Gate-Source Leakage	V _{GS} = ±30V	--	--	±100	nA
VGS(th)	Gate-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0	--	4.0	V
RDS(on)	Drain-Source On-Resistance (Note3)	V _{GS} = 10V, I _D = 3.5A	--	0.75	0.9	Ω
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	--	1037	--	pF
C _{oss}	Output Capacitance		--	138	--	
C _{rss}	Reverse Transfer Capacitance		--	5.3	--	
Q _g	Total Gate Charge	V _{DD} =520V, I _D = 9A, V _{GS} = 10V	--	19	--	nC
Q _{gs}	Gate-Source Charge		--	7.3	--	
Q _{gd}	Gate-Drain Charge		--	8.5	--	
td(on)	Turn-on Delay Time	V _{DD} =325V, I _D = 7A, R _G = 25Ω	--	18	--	ns
t _r	Turn-on Rise Time		--	30	--	
td(off)	Turn-off Delay Time		--	61	--	
t _f	Turn-off Fall Time		--	36	--	
I _S	Continuous Body Diode Current	T _C = 25 °C	--	--	9.0	A
I _{SM}	Pulsed Diode Forward Current		--	--	36	A
V _{SD}	Body Diode Voltage	T _J = 25°C, I _{SD} = 7A, V _{GS} = 0V	--	--	1.2	V
trr	Reverse Recovery Time	V _{GS} = 0V, I _S = 7A, di _F /dt = 100A/μs	--	431	--	ns
Q _{rr}	Reverse Recovery Charge		--	2.6	--	μC

Note :

- 1、 The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2、 The EAS data shows Max. rating . I_{AS} = 9.0A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25 °C
- 3、 The test condition is Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

650V N-Channel Enhancement Mode MOSFET

Typical Characteristics

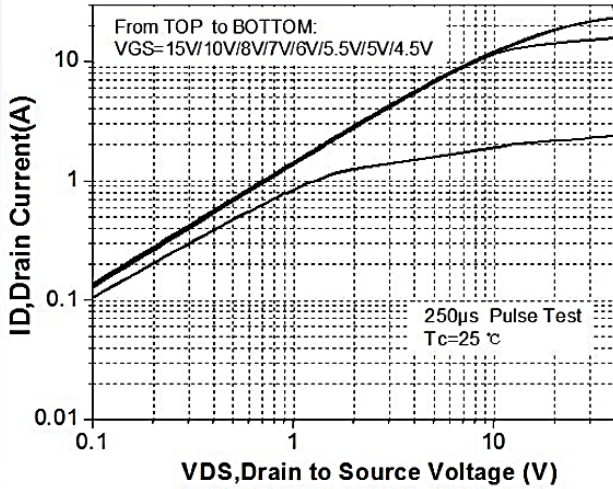


Figure 1. On-Region Characteristics

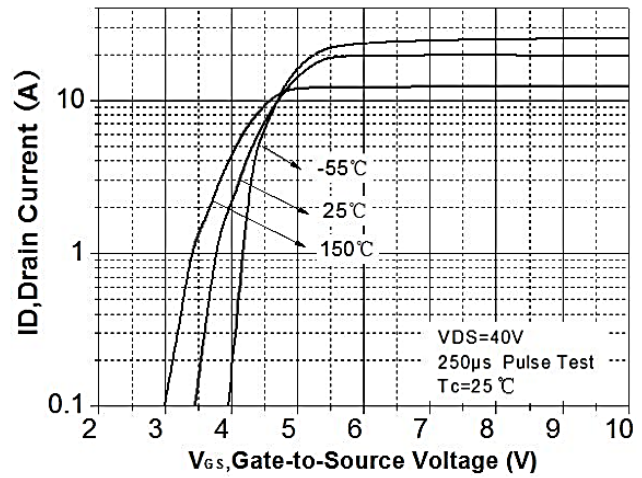


Figure 2. Transfer Characteristics

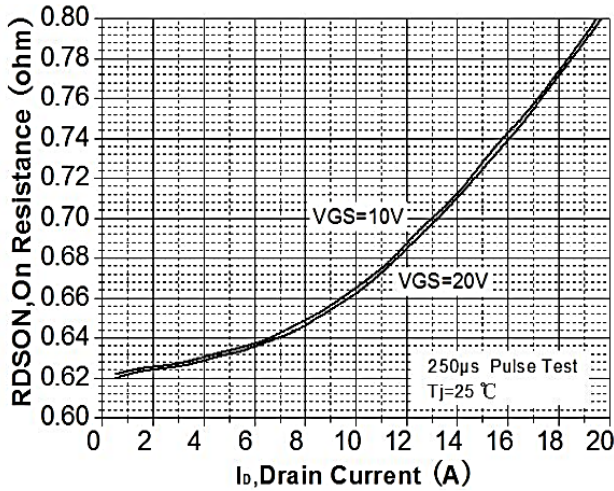


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

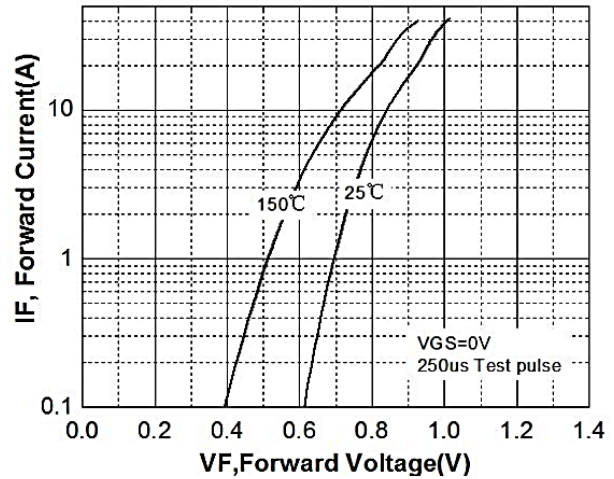


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

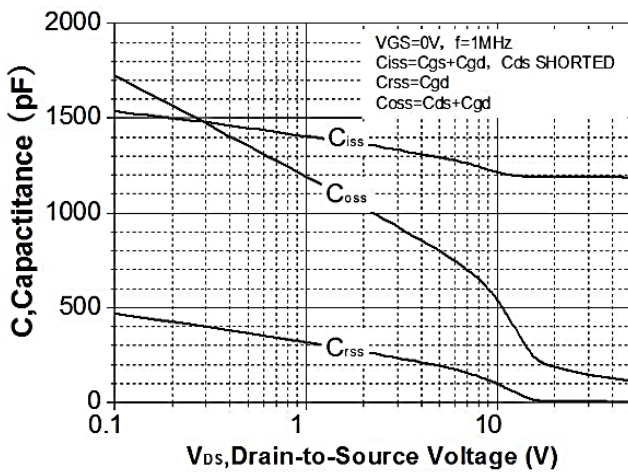


Figure 5. Capacitance Characteristics

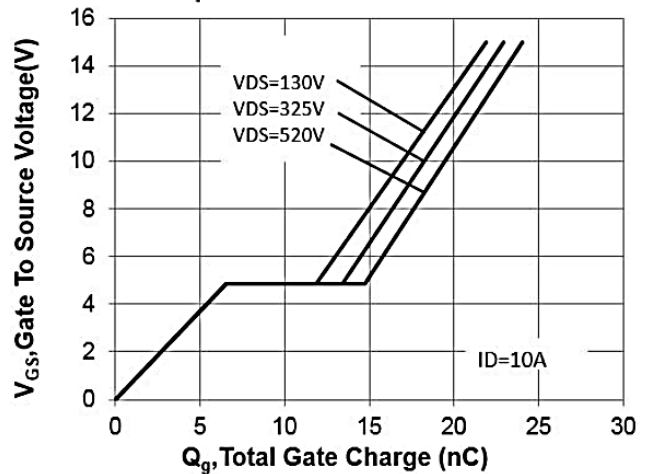


Figure 6. Gate Charge Characteristics

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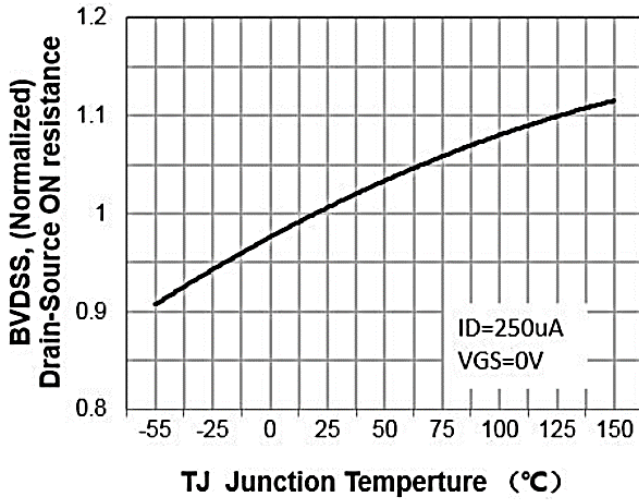


Figure 7. Breakdown Voltage Variation vs Temperature

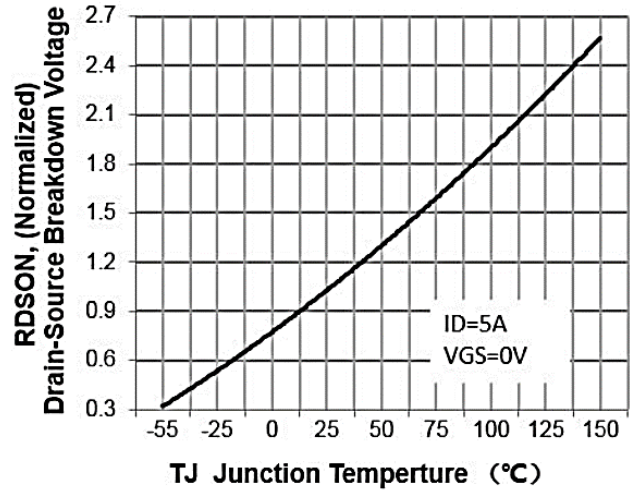


Figure 8. On-Resistance Variation vs Temperature

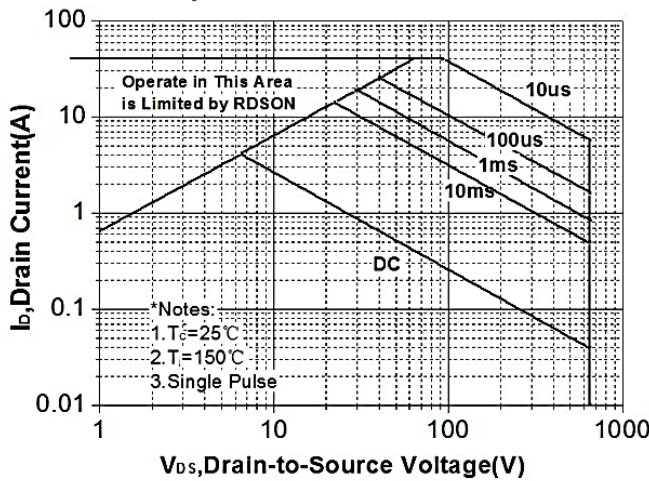


Figure 9. Maximum Safe Operating Area

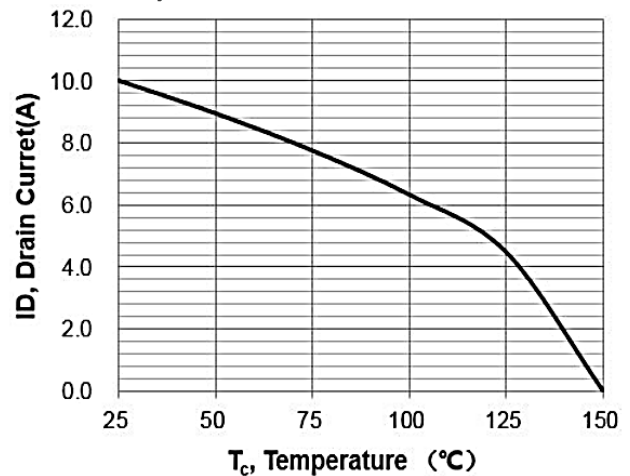


Figure 10. Maximum Drain Current vs Case Temperature

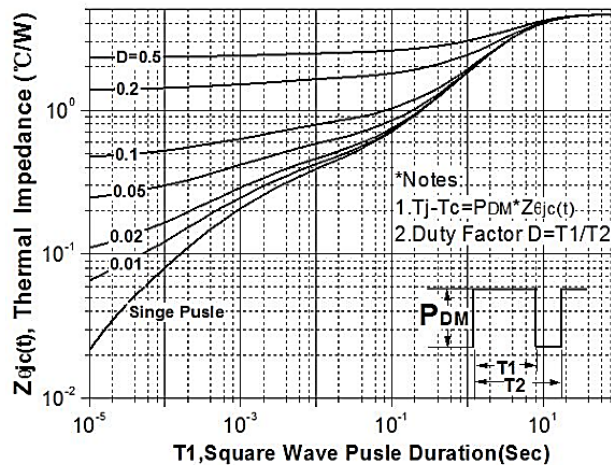
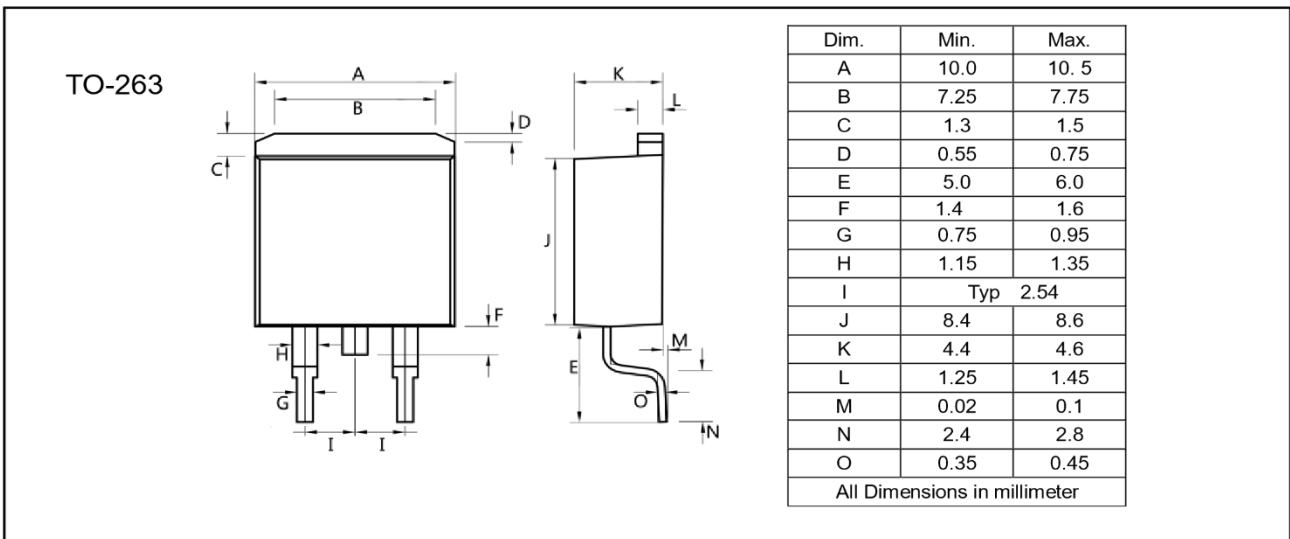
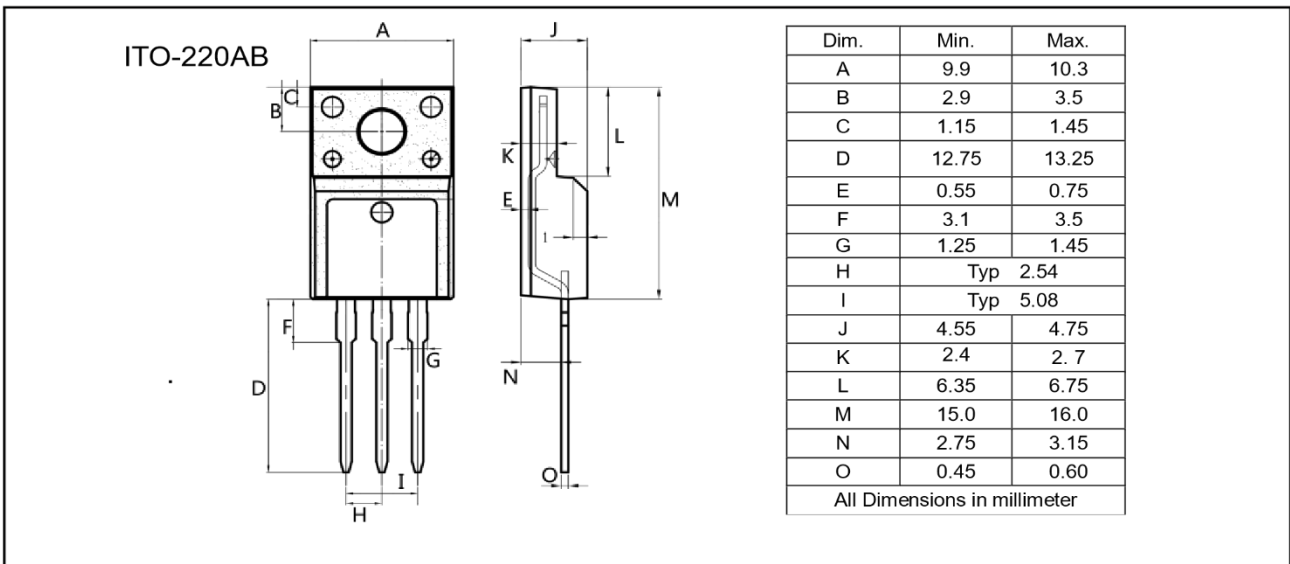
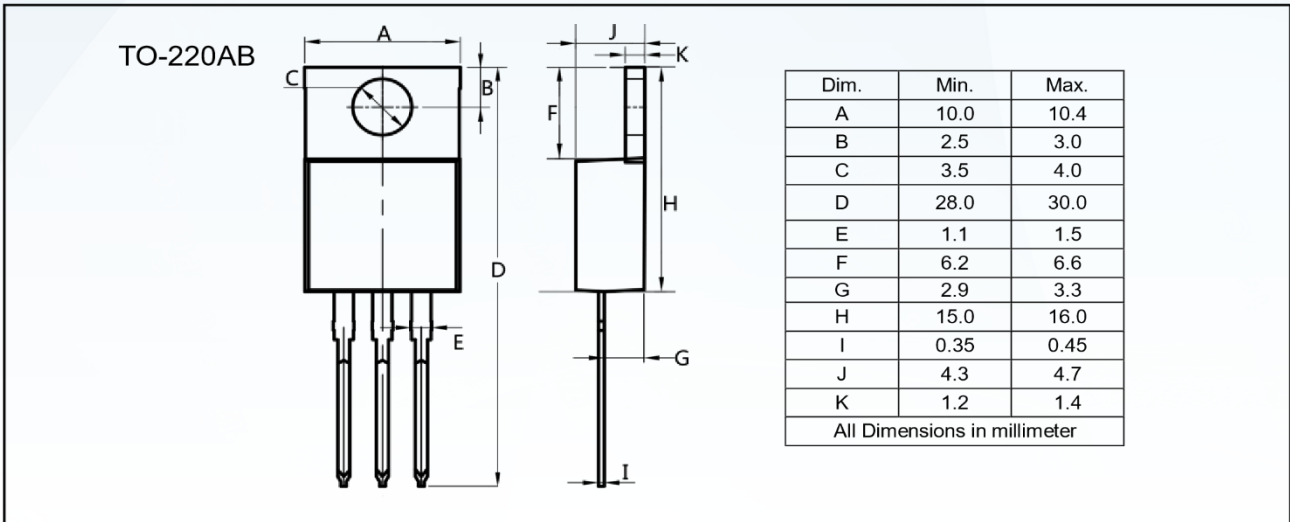


Figure 11. Transient Thermal Response Curve

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