FAIRCHILD
A Schlumberger Company

11C01
Dual 5-4 Input OR/NOR Gate

11C ECL Product

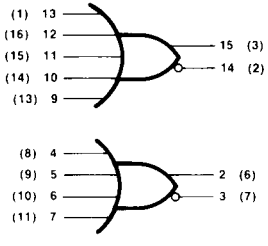
Description

The 11C01 is a voltage-compensated ECL dual 5-4 input OR/NOR gate. The circuit has standard internal voltage compensation with DC parameters identical to 10K ECL devices.

Pin Names

D_{1a}-D_{1e}, D_{2a}-D_{2d}	Data Inputs
Q_1, $\overline{Q_1}$, Q_2, $\overline{Q_2}$	Outputs

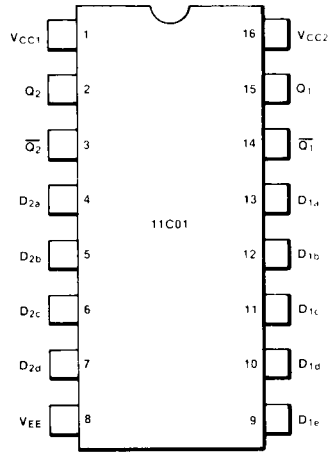
Logic Symbol



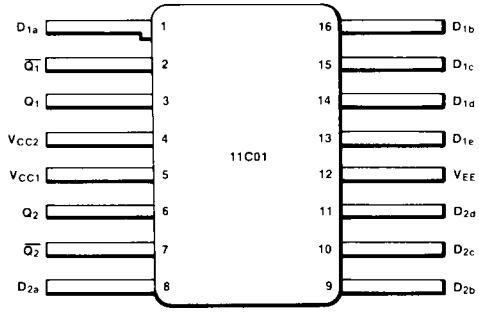
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
( ) = Flatpak

Connection Diagrams

16-Pin DIP (Top View)



16-Pin Flatpak (Top View)



Ordering Information

Package	Outline	Order Code
Ceramic DIP	4J	DC
Flatpak	3L	FC

Absolute Maximum Ratings Above which the useful life may be impaired

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	-7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	-50 mA
Operating Range	-5.5V to -4.75V
Lead Temperature (Soldering 10 sec.)	300°C

Guaranteed Operating Ranges

Supply Voltage (V_{EE})			Ambient Temperature (T_A)
Min	Typ	Max	
-5.5V	-5.2V	-4.75V	0°C to +75°C

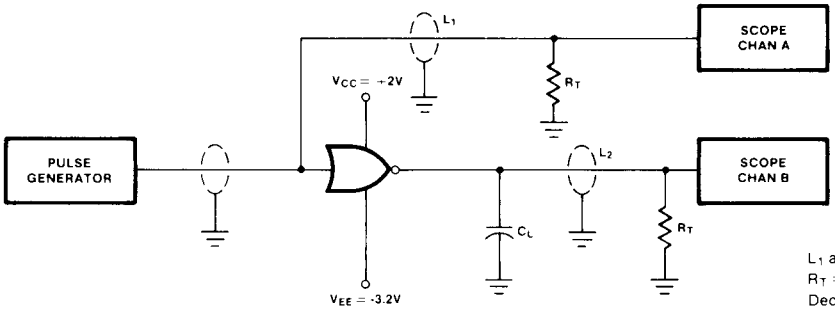
D C Characteristics: V_{EE} = -5.2V, V_{CC} = GND

Symbol	Characteristic	Min	Typ	Max	Unit	T_A	Condition	
V_{OH}	Output Voltage HIGH	-1000 -960 -900		-840 -810 -720	mV	0°C +25°C +75°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ per Truth Table	Loading is 50Ω to -2.0V
V_{OL}	Output Voltage LOW	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C +25°C +75°C		
V_{OHC}	Output Voltage HIGH	-1020 -980 -920			mV	0°C +25°C +75°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ per Truth Table	
V_{OLC}	Output Voltage LOW			-1645 -1630 -1605	mV	0°C +25°C +75°C		
V_{IH}	Input Voltage HIGH	-1145 -1105 -1045		-840 -810 -720	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			350	μA	+25°C	V_{IN} = $V_{IH(Max)}$	
I_{IL}	Input Current LOW	0.5			μA	+25°C	V_{IN} = $V_{IL(Min)}$	
I_{EE}	Power Supply Current	-30	-24		mA	+25°C	Inputs and Outputs Open	

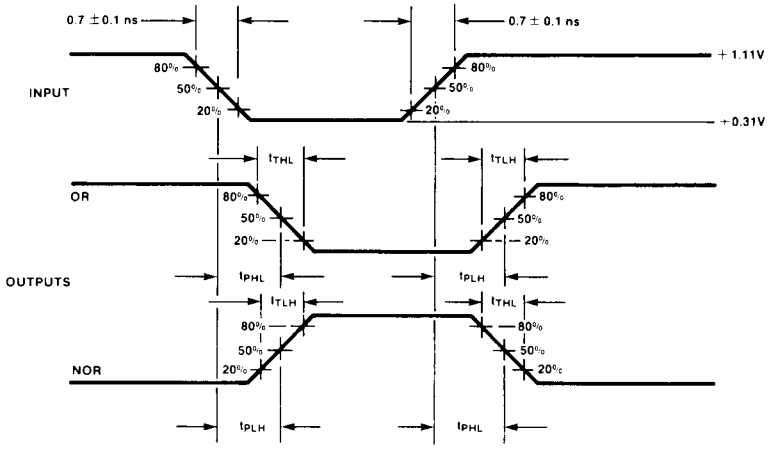
AC Characteristics: V_{EE} = -5.2V, T_A = +25°C

Symbol	Characteristic	Flatpak			DIP			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
t_{PLH}	Propagation Delay, LOW to HIGH	0.45	0.7	0.95	0.60	0.90	1.15	ns	See Figure 1
t_{PHL}	Propagation Delay, HIGH to LOW	0.45	0.7	0.95	0.60	0.90	1.15	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to80%)		0.7	0.95		0.90	1.15	ns	
t_{PHL}	Output Transition Time HIGH to LOW (80% to 20%)		0.7	0.95		0.90	1.15	ns	

Figure 1 Switching Circuit and Waveforms



L_1 and L_2 = equal length 50Ω impedance lines
R_T = 50Ω Termination of scope
Decoupling 0.1 μF from GND to V_{EE} and V_{CC}
$C_L \leq 3pF$



Jig set-up with no circuit under test
$V_{CC1} = V_{CC2}$ = +2.0V
V_{EE} = -3.2V

Truth Table

In					Out	
D_{1a}	D_{1b}	D_{1c}	D_{1d}	D_{1e}	Q_1	$\overline{Q_1}$
L	L	L	L	L	L	H
H	X	X	X	X	H	L
X	H	X	X	X	H	L
X	X	H	X	X	H	L
X	X	X	H	X	H	L
X	X	X	X	H	H	L

In				Out	
D_{2a}	D_{2b}	D_{2c}	D_{2d}	Q_2	$\overline{Q_2}$
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care