

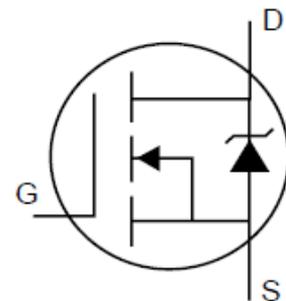
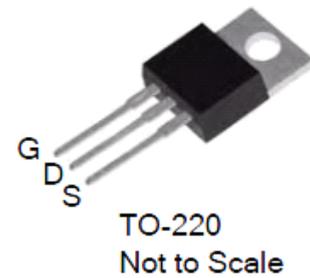
DESCRIPTION

The 120N03 uses advanced trench technology
 And design to provide excellent $R_{DS(ON)}$ with
 Low gate charge . It can be used in a wide
 Variety of applications .

V_{DS}	$R_{DS(ON)}$	I_D
30V	2.5m Ω	120A

GENERAL FEATURES

- $V_{DS} = 30\text{ V}$, $I_D = 120\text{ A}$
 $R_{DS(ON)} < 4\text{ m}\Omega @ V_{GS} = 10\text{ V}$ (Typ:2.5m Ω)
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability



Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

Ordering Information

PART NUMBER	PACKAGE	BRAND
120N03	TO-220	OGFD

Absolute Maximum Ratings (TC=25°C, unless otherwise noted)

Symbol	Parameter	120N03	Units
V _{DS}	Drain-to-Source Voltage	30	V
I _D	Continuous Drain Current	120	A
	Drain Current-Continuous(Tc=100°C)	84	
I _{DM}	Pulsed Drain Current@VG=10V	400	
P _D	Power Dissipation	120	W
V _{GS}	Gate-to-Source Voltage	± 20	V
E _{AS}	Single Pulse Avalanche Energy (L=1mH, IAS=40A)C	350	mJ
T _J and T _{STG}	Operating Junction and Storage Temperature Range	-55 to 175	°C

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
R _{θJC}	Junction-to-Case	--	--	1.25	°C/W	Water cooled heatsink, P _D adjusted for a peak junction temperature of +175°C.

OFF Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
B _{VDS}	Drain-to-Source Breakdown Voltage	30	--	--	V	V _{GS} =0, I _D =250μA
I _{GSS}	Gate-to-Source Forward Leakage	--	--	±100	nA	V _{DS} =0V, V _{GS} =±20V
I _{DSS}	Zero Gate Voltage Drain Current	--	--	1	μA	V _{DS} =30V, V _{GS} =0V

ON Characteristics T_J=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max	Units	Test Conditions
R _{DS(ON)}	Static Drain-to-Source On-Resistance	--	2.5	4.0	mΩ	V _{GS} =10V, I _D =20A
V _{GS(TH)}	Gate Threshold Voltage, Figure 12.	1.0	1.6	3.0	V	V _{DS} =10V, I _D =250μA
G _{fs}	Forward Transconductance	50	---	--	S	V _{DS} =10V, I _D =20A

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C _{iss}	Input Capacitance	--	3550	--	pF	V _{DS} =25V, V _{GS} =0V, f=1.0MHZ
C _{oss}	Output Capacitance	--	1350	--		
C _{rss}	Reverse Transfer Capacitance	--	120	--		
Q _g	Total Gate Charge	--	48	--	nC	V _{DS} =15V, V _{GS} =10V, I _D =20A
Q _{gs}	Gate-to-Source Charge	--	11	--		
Q _{gd}	Gate-to-Drain ("Miller") Charge	--	10	--		

Drain-Source Diode Characteristics

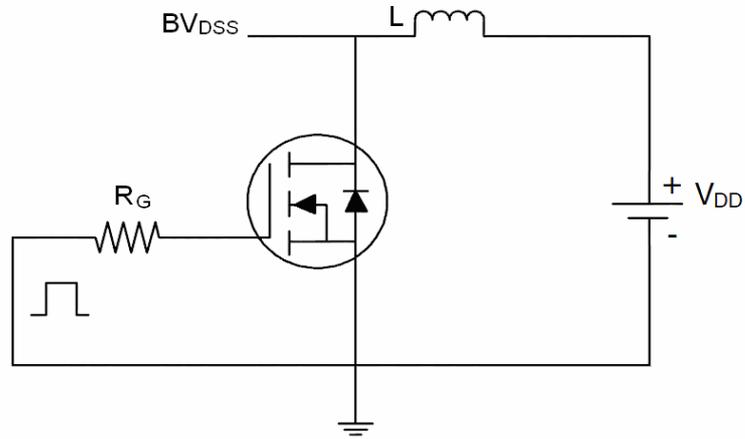
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =20A	--	--	1.2	V
Diode Forward Current	I _S	--	--	--	120	A
Reverse Recovery Time	t _{rr}	T _J =25°C, I _F = 20 A Di/dt = 100 A/μs	--	21	--	nS
Reverse Recovery Charge	Q _{rr}		--	58	--	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

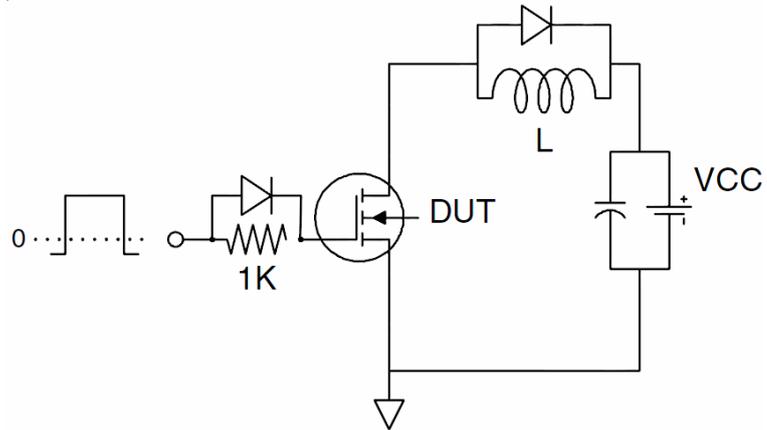
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production.
5. EAS condition: T_J=25°C, V_{DD}=100V, V_G=10V, L=0.5mH, R_g=25Ω.

Test circuit

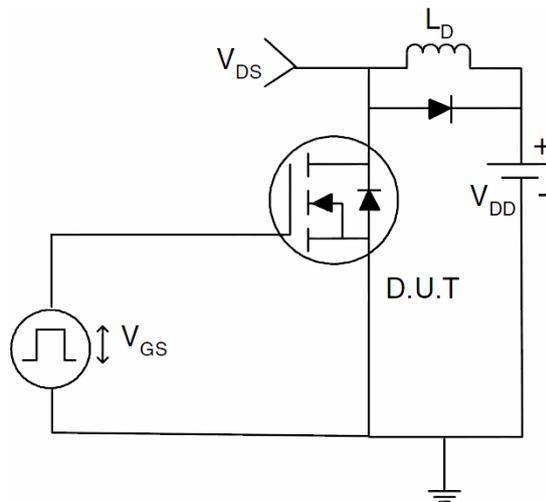
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

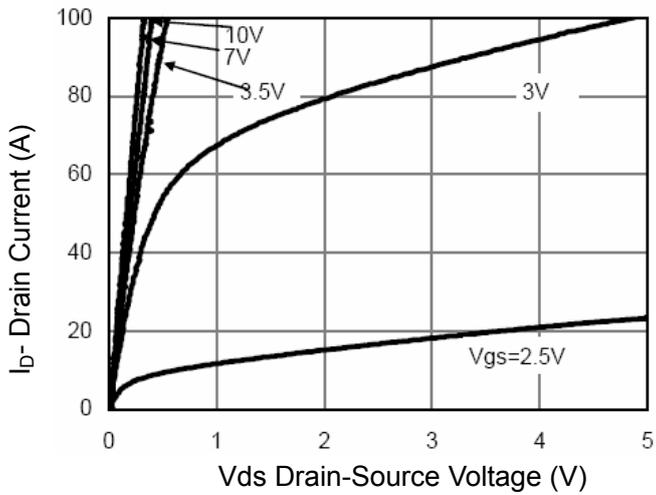


Figure 1 Output Characteristics

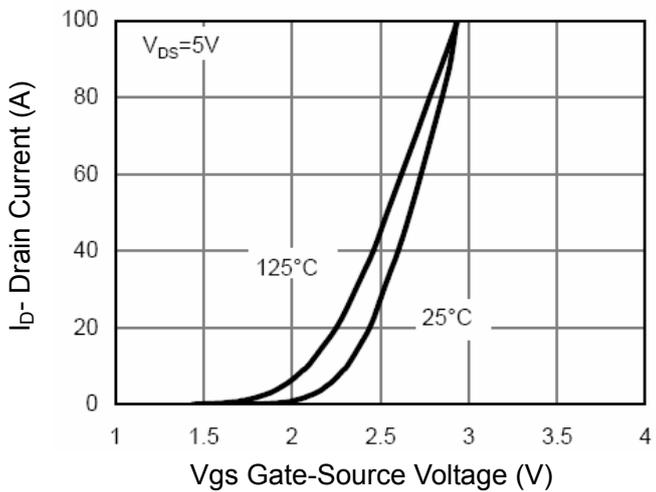


Figure 2 Transfer Characteristics

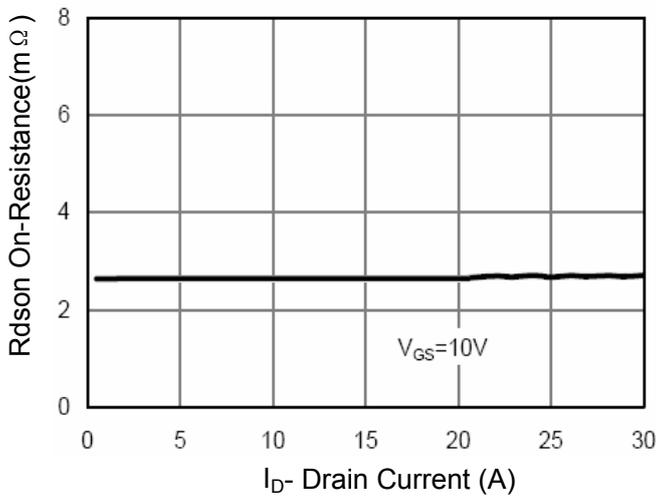


Figure 3 $R_{DS(on)}$ - Drain Current

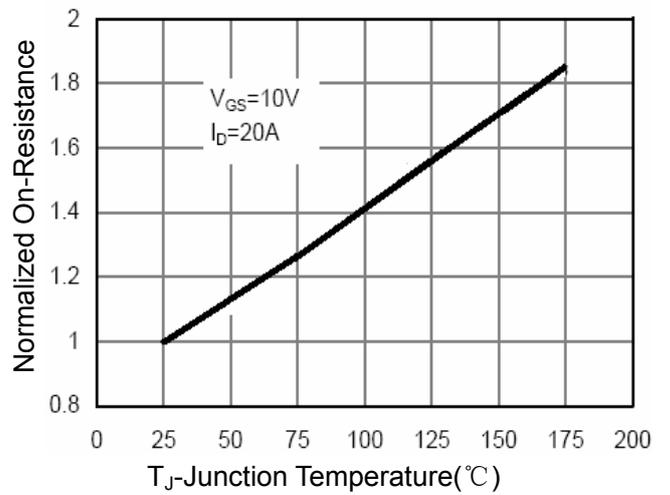


Figure 4 $R_{DS(on)}$ -Junction Temperature

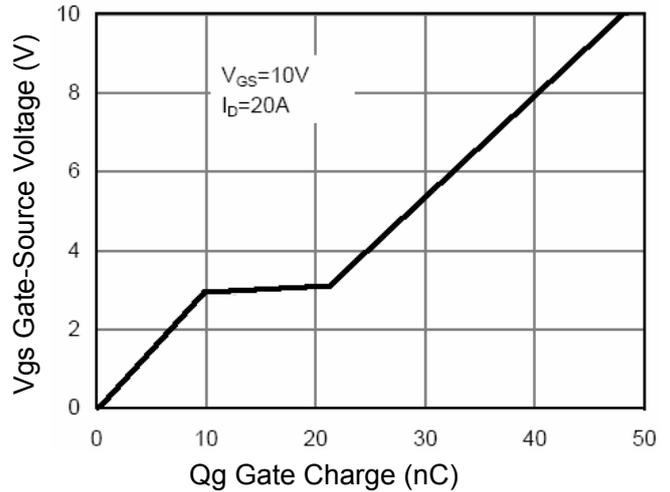


Figure 5 Gate Charge

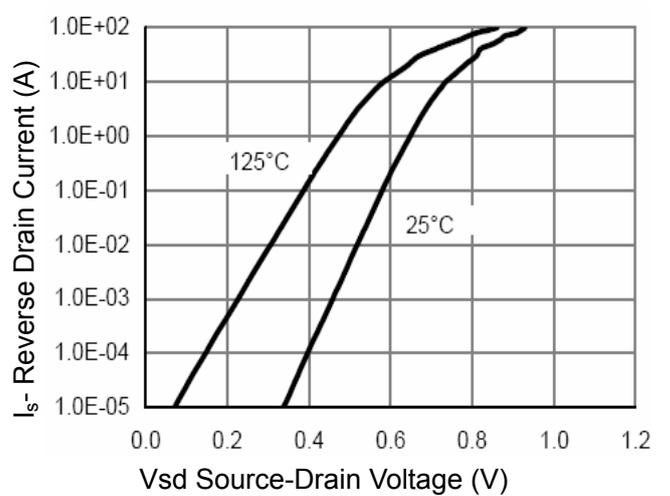


Figure 6 Source- Drain Diode Forward

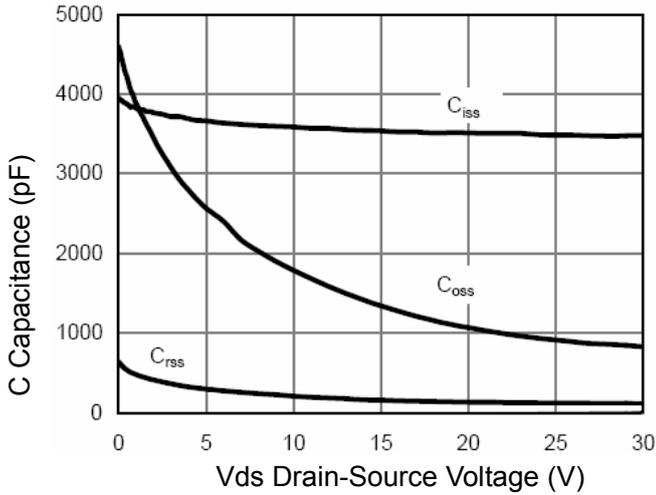


Figure 7 Capacitance vs Vds

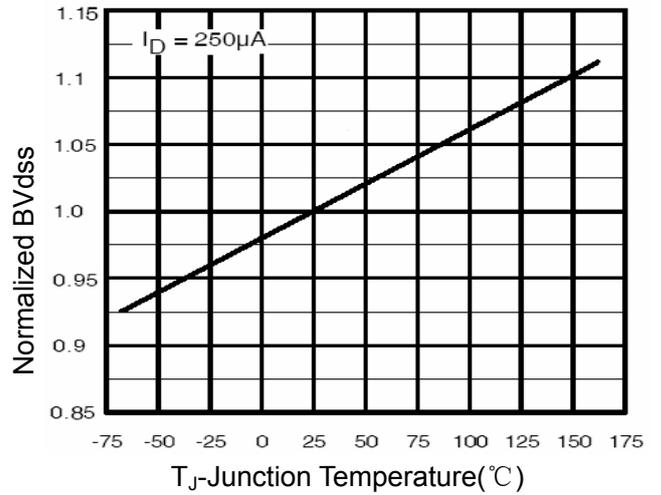


Figure 9 BV_{DSS} vs Junction Temperature

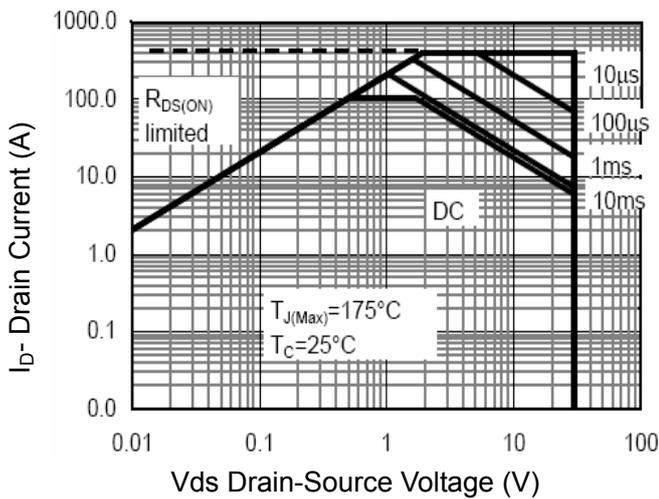


Figure 8 Safe Operation Area

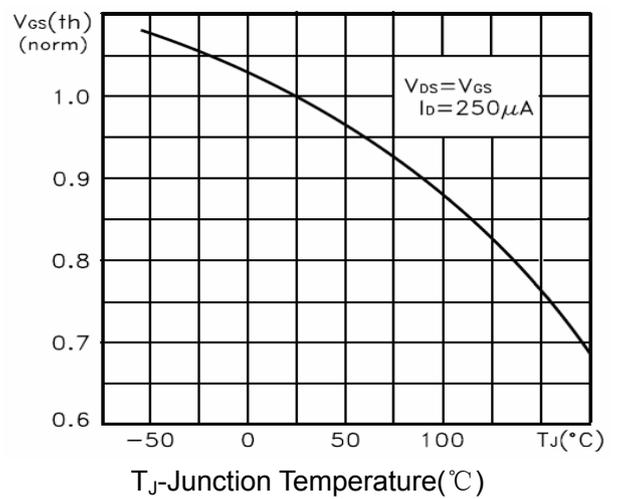


Figure 10 $V_{GS(th)}$ vs Junction Temperature

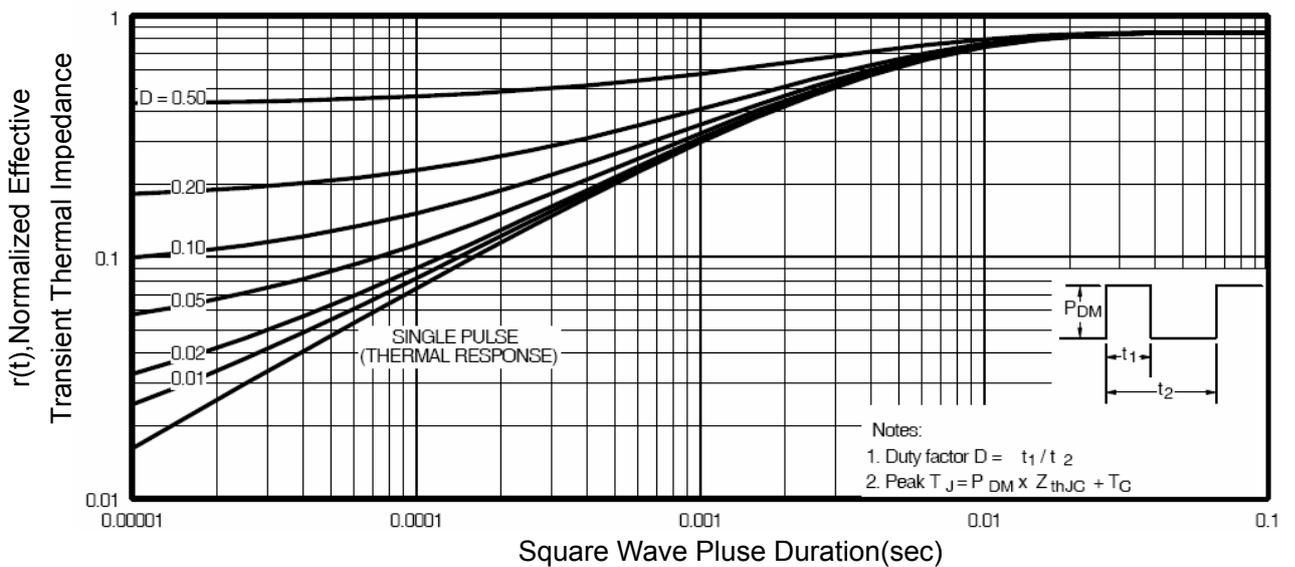


Figure 11 Normalized Maximum Transient Thermal Impedance