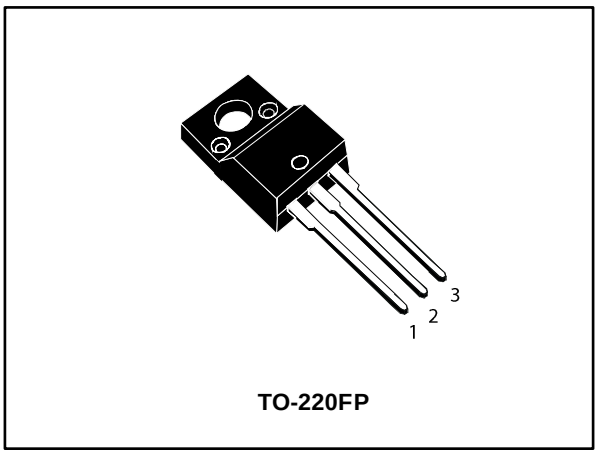
STF12NK65Z

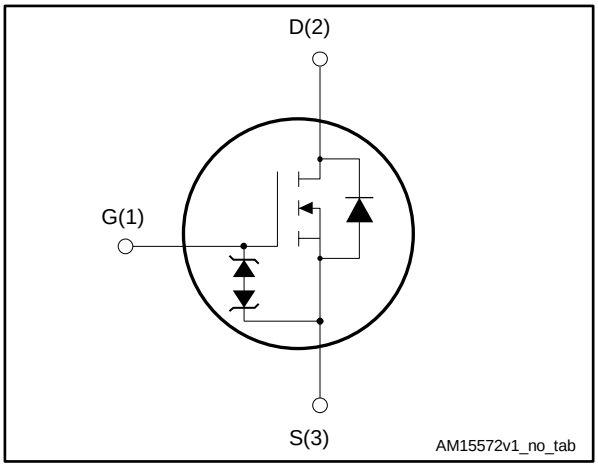
N-channel 650 V, 0.6 Ω typ., 10 A SuperMESH™ Power MOSFET in a TO-220FP package

Datasheet - production data



TO-220FP

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF12NK65Z	650 V	0.7 Ω	10 A	35 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

This high voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF12NK65Z	12NK65Z	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	10	A
I_D	Drain current (continuous) at T_C = 100 °C	6.3	A
I_{DM}(1)	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at T_C = 25 °C	35	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C= 25 °C)	2500	V
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operation junction temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 10 A, di/dt ≤ 200 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	3.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_{JMAX})	10	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	225	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 10 A		0.6	0.7	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	-	1837	-	pF
C_{oss}	Output capacitance		-	208	-	pF
C_{rss}	Reverse transfer capacitance		-	48.8	-	pF
$C_{oss\ eq}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	122	-	pF
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 10 A, V_{GS} = 0 to 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	62.6	-	nC
Q_{gs}	Gate-source charge		-	9.6	-	nC
Q_{gd}	Gate-drain charge		-	36	-	nC
R_G	Intrinsic gate resistance	f = 1 MHz, I_D= 0 A	-	1	-	Ω

Notes:

(1)$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	25	-	ns
t_r	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Fall time		-	11.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
I_{SDM}(1)	Source-drain current (pulsed)		-		40	A
V_{SD}(2)	Forward on voltage	I_{SD} = 10 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 10 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	436		ns
Q_{rr}	Reverse recovery charge		-	3.4		µC
I_{RRM}	Reverse recovery current		-	15.4		A
t_{rr}	Reverse recovery time	I_{SD} = 10 A, di/dt = 100 A/µs, V_{DD} = 60 V , T_J = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	518		ns
Q_{rr}	Reverse recovery charge		-	4.1		µC
I_{RRM}	Reverse recovery current		-	15.9		A

Notes:

(1)Pulsed: pulse duration=300 µs, duty cycle 1.5%.

(2)Pulse width limited by safe operating area.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

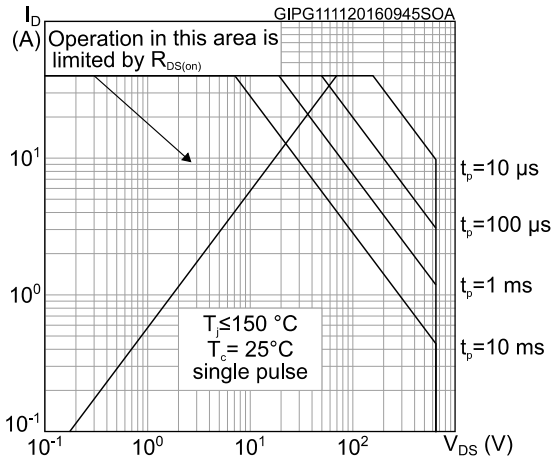


Figure 3: Thermal impedance

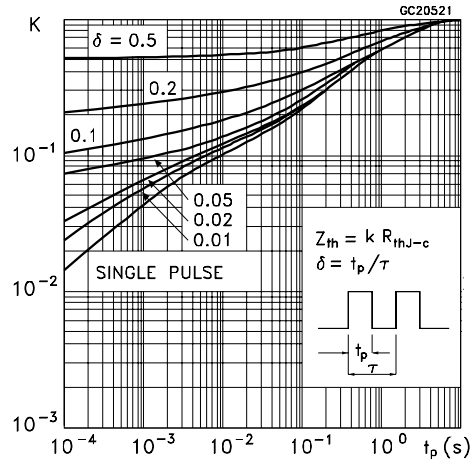


Figure 4: Output characteristics

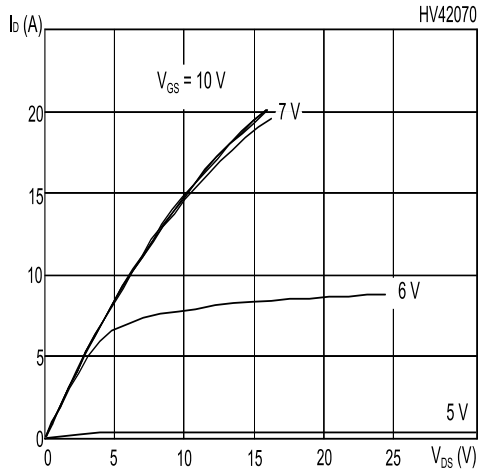


Figure 5: Transfer characteristics

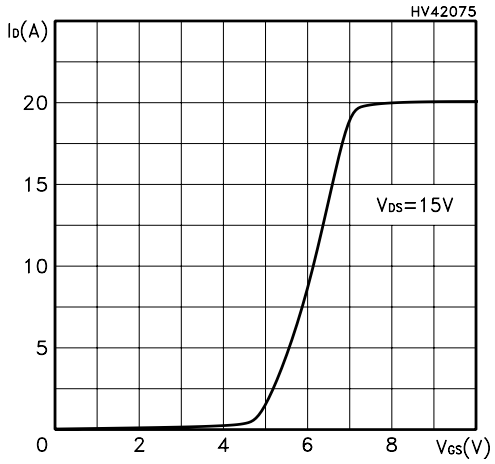


Figure 6: Normalized $V_{(BR)DSS}$ vs. temperature

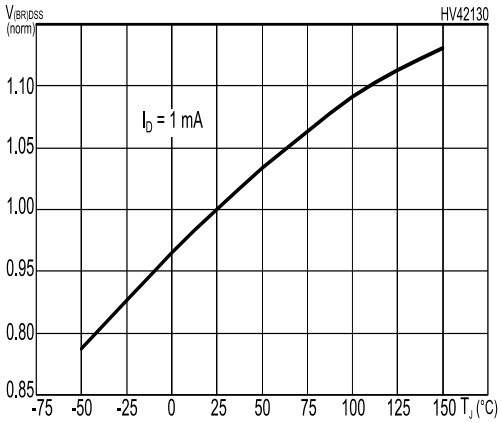


Figure 7: Gate charge vs. gate-source voltage

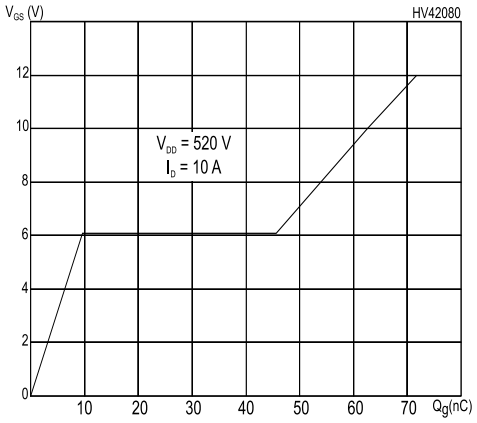


Figure 8: Capacitance variations

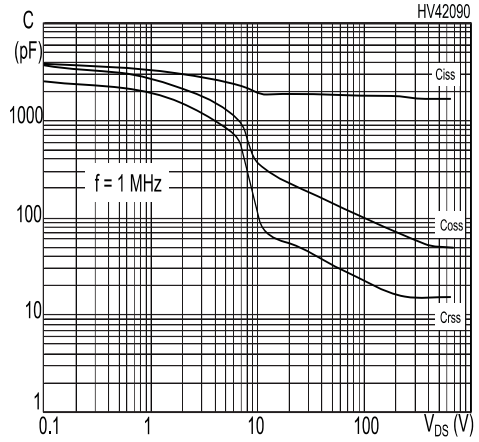


Figure 9: Static drain-source on-resistance

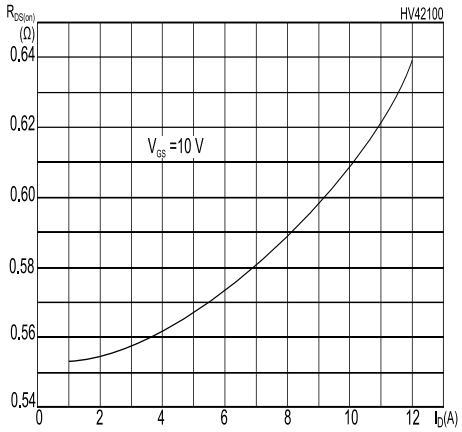


Figure 10: Normalized gate threshold voltage vs. temperature

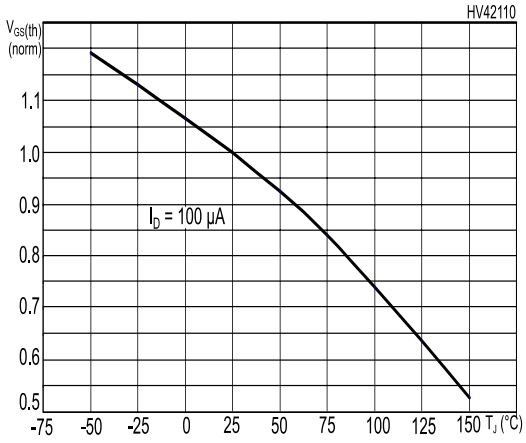


Figure 11: Normalized on-resistance vs. temperature

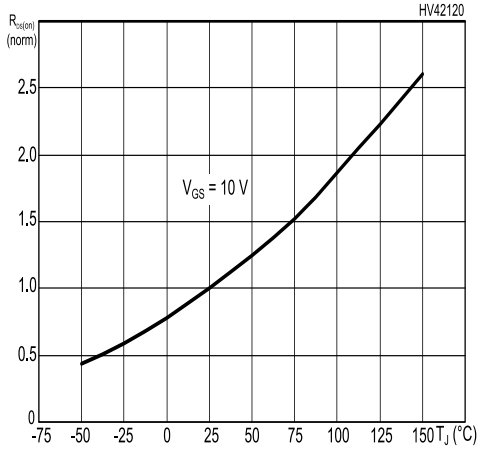


Figure 12: Source-drain diode forward characteristics

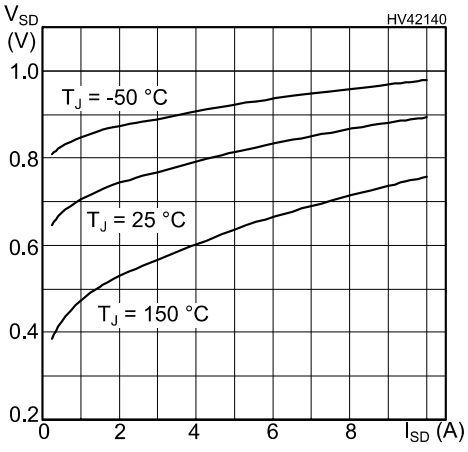
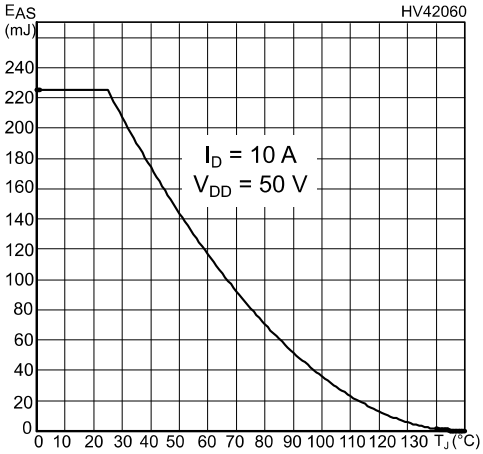


Figure 13: Maximum avalanche energy vs. starting T_J



3 Test circuits

Figure 14: Test circuit for resistive load switching times

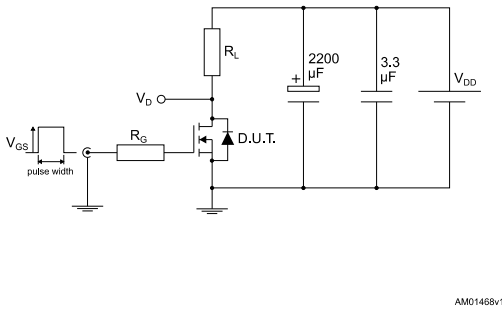


Figure 15: Test circuit for gate charge behavior

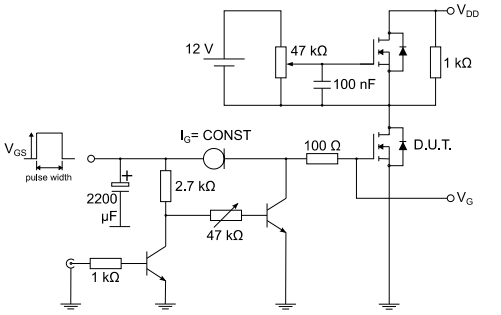


Figure 16: Test circuit for inductive load switching and diode recovery times

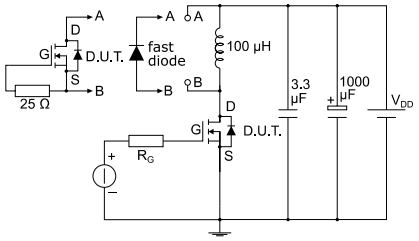


Figure 17: Unclamped inductive load test circuit

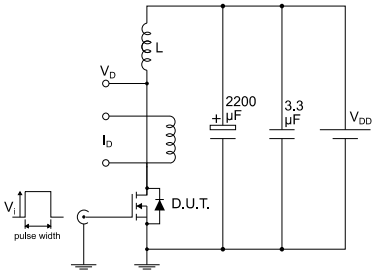


Figure 18: Unclamped inductive waveform

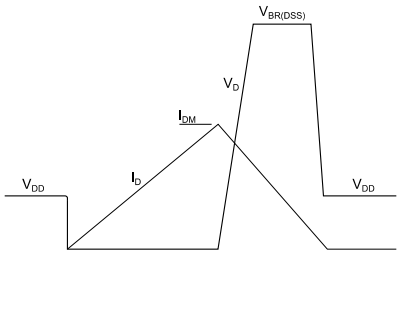
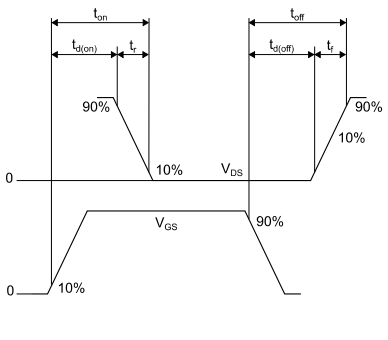


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20: TO-220FP package outline

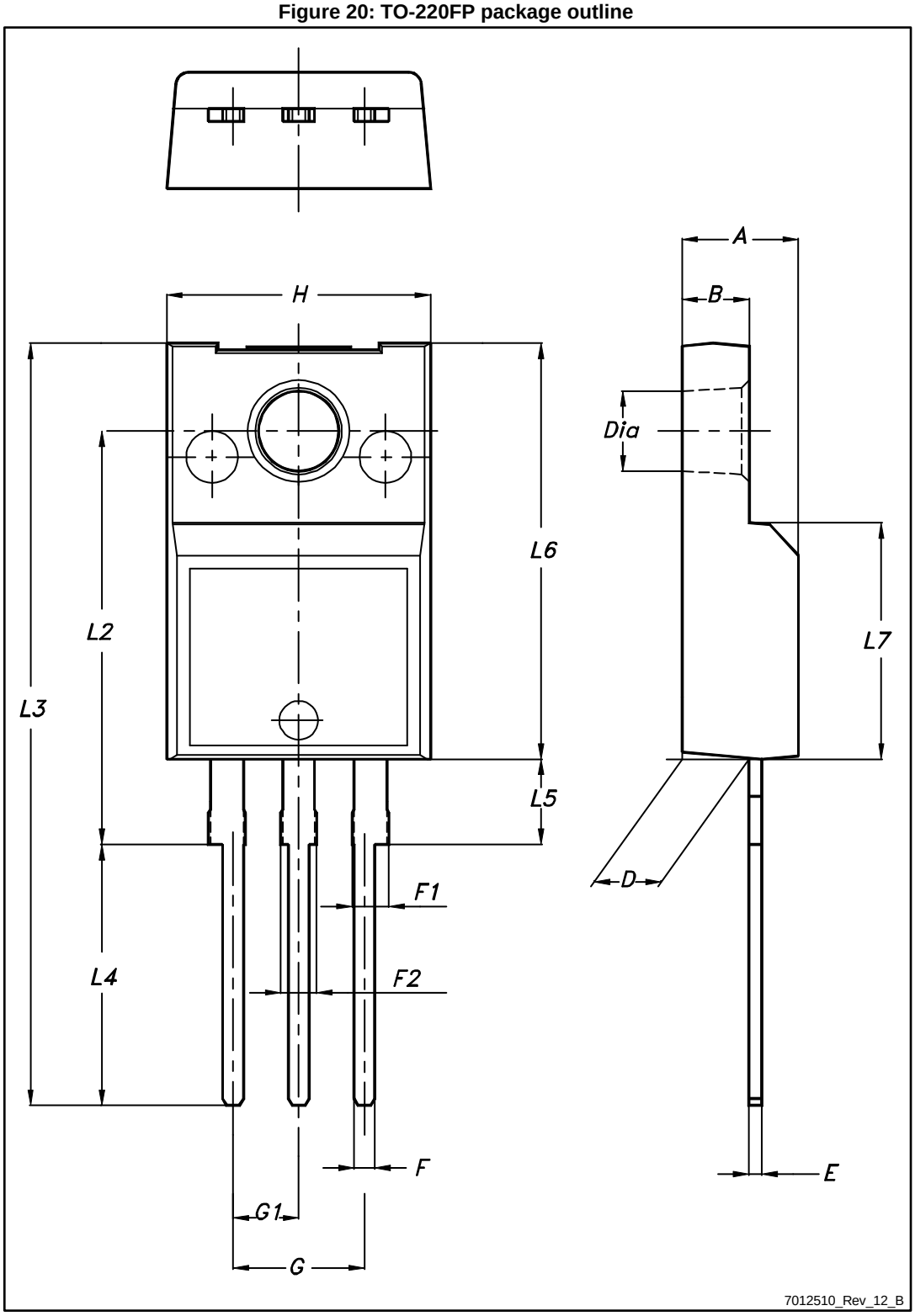


Table 10: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
01-Oct-2010	1	Initial release.
10-Nov-2016	2	Modified title, features and description in cover page Modified *Table 2: "Absolute maximum ratings"*, *Table 3: "Thermal data"*, *Table 5: "On /off states"*, *Table 6: "Dynamic"*, *Table 8: "Source drain diode"*, *Table 9: "Gate-source Zener diode"* Modified *Figure 2: "Safe operating area"* Updated *Section 4.1: "TO-220FP package information"* Minor text changes
05-Apr-2017	3	Datasheet status promoted from preliminary to production data. Updated *Section 2.1: "Electrical characteristics (curves)"*. Minor text changes

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