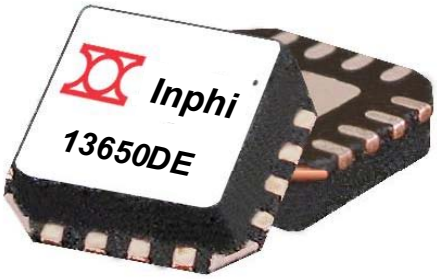
# 13650DE
# 13 Gbps Differential Encoder
# Data Sheet




## Applications

- High-speed (up to 13 Gbps) optical duobinary systems
- High-speed (up to 13 Gbps) optical differential phase shift keying systems (DPSK)
- High-speed (up to 13 GHz) digital logic
- Broadband test and measurement equipment

## Features

- Supports data rates up to 13 Gbps
- Fast rise and fall times typically 15 ps
- Low power consumption: 380 mW
- 290° input phase margin (at 12.5 Gbps)
- Supports single-ended and differential operation
- Output signal swing 1200 mVpp differential
- Single –3.3 V power supply
- Available in plastic QFN package
- Evaluation board available

## Description

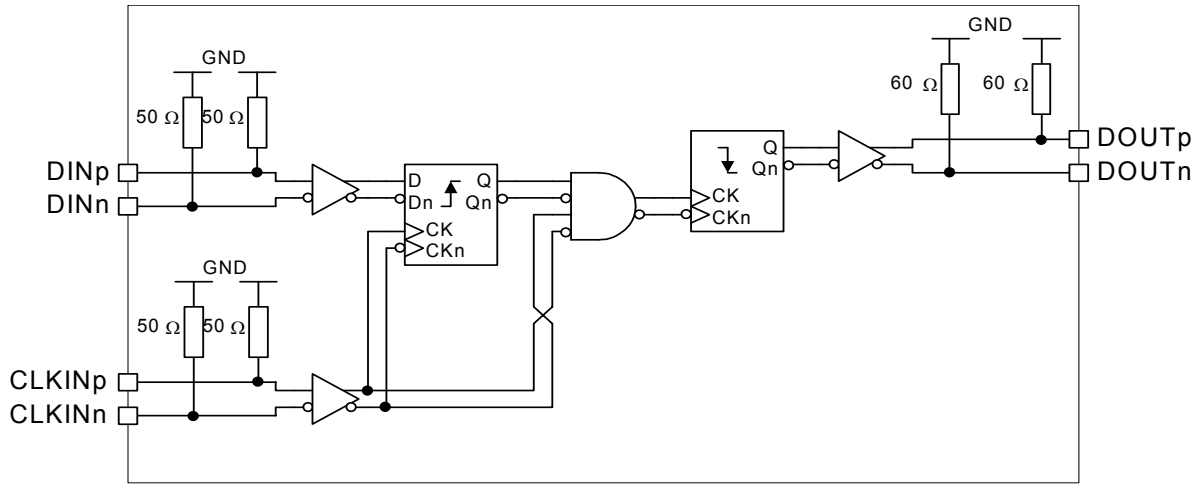
The 13650DE differential encoder performs modulo two addition of the input data bit with the previous output bit. The part operates up to 13 Gbps and retimes the input data before performing the encoding operation, thereby providing a large input phase margin.

The encoder is nominally positive-edge triggered; however, by reversing the positive and negative clock connections, a negative-edge triggered application can be accommodated.

All differential data and differential clock inputs are on-chip DC coupled and terminated with 50 Ω resistors to ground (GND). For direct- coupled applications, the differential data outputs should be terminated off chip with 50 Ω resistors to GND. For applications requiring termination to DC levels other than GND, external AC coupling to a good RF ground is required. See the application note for various termination examples.

The 13650DE operates from a single -3.3 V power supply and dissipates only 380 mW. It is available in a 3 x 3 $mm^2$ quad flat no-lead (QFN) plastic package and is also available on an evaluation board with SMA connectors.

## Block Diagram




## Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{EE}$ | | –3.6 | +0.5 | V |
| Input Signals (Data & Clock) | | | –2 | +1 | V |
| Output Signals | | | –2 | +1 | V |
| Junction Temperature– Die | $T_J$ | | –5 | +175 | °C |
| Case Temperature– Packaged | $T_C$ | | –15 | +125 | °C |
| Shipping/Storage Temperature | $T_{STORE}$ | | –40 | +125 | °C |
| Humidity | RH | | 0 | 100 | % |
| ESD Protection (Human Body Model) | ESD | Clock and Data inputs | 500 | --- | V |
| | | Data outputs | 250 | --- | V |
| | | Power Supply | 500 | --- | V |

## Operating Conditions

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Power Supply Level | $V_{EE}$ | ± 5% Tolerance | –3.465 | –3.300 | –3.135 | V |
| On-Chip Power Dissipation | $P_D$ | | --- | 380 | 500 | mW |
| Power Supply Current | $I_{CC}$ | | --- | 110 | 144 | mA |
| Operating Temperature (Junction) – Die | $T_J$ | | +15 | --- | +125 | °C |
| Operating Temperature (Case) – Package | $T_C$ | Bottom of paddle | –5 | --- | +85 | °C |
| Thermal Resistance – junction to paddle | $R_{JC}$ ($\theta_{JC}$) | Bottom of paddle | --- | 51 | --- | °C/W |

# Electrical Specifications

**WARNING** – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

| Electrical specifications guaranteed when the part is operated within the specified operating conditions. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Conditions** | **Min** | **Typ** | **Max** | **Unit** |
| Maximum Data Rate | | $10^{-12}$ BER (NRZ format) | 13 | --- | --- | Gbps |
| Maximum Clock Frequency | $f_{MAX}$ | | 13 | --- | --- | GHz |
| Minimum Clock Slew Rate | $S_{MIN}$ | At CLKINp/CLKINn crossing | --- | --- | 1 | V/ns |
| Input High Level (Data & Clock) | $V_{IH}$ | | –0.5 | --- | 0.5 | V |
| Input Low Level (Data & Clock) | $V_{IL}$ | | –1.0 | --- | 0 | V |
| Input Amplitude (Data & Clock) | $VIN_{pp}$, $VCLK_{pp}$ | Differential peak-to-peak | 300 | --- | 2000 | mVpp |
| | | Single ended peak-to-peak | 300 | --- | 1000 | mVpp |
| Input Return Loss (Data) [1] | $RL_{IN}$ | < 13 GHz; Input common mode < 0.0 V | 10 | --- | --- | dB |
| | | < 13 GHz; Input common mode < + 0.5 V | 6 | | | dB |
| Input Return Loss (Clock) [1] | $RL_{IN}$ | < 13 GHz | 10 | | | dB |
| Clock Phase Margin | CPM | At 12.5 Gbps | 255 | 290 | --- | deg |
| Data Output Amplitude[2] | $VOUT_{pp}$ | Differential peak-to-peak | 900 | 1200 | 1400 | mVpp |
| Output High Voltage | $V_{OH}$ | DC coupled, GND referenced | –50 | –4 | 0 | mV |
| Output Low Level | $V_{OL}$ | DC coupled, GND referenced | –700 | – 600 | – 450 | mV |
| Output Common Mode | $V_{OCM}$ | DC coupled, GND referenced | --- | –300 | --- | mV |
| Output Rise/Fall Time | $t_r/t_f$ | 20–80% | --- | 15 | 25 | ps |
| Output Return Loss[3] | $RL_{OUT}$ | < 13 GHz | 10 | --- | --- | dB |
| Deterministic Jitter[4,5] | $J_D$ | Peak-to-peak | --- | 2 | 4 | ps |
| Random Jitter[4,5] | $J_R$ | RMS | --- | 0.2 | 0.4 | ps |
| Clock-to-Data Output Delay[4,6] | $t_Q$ | QFN Package | 50 | 65 | 80 | ps |
| Set-up Time[6,7] | $t_{set}$ | Measured at package pins | 12 | 8 | | ps |
| Hold Time[6,7] | $t_{hold}$ | Measured at package pins | 12 | 8 | | ps |

Notes:

[1] Inputs are designed to be a broadband match to 50 Ω impedance and are terminated with a 50 Ω resistor to GND.

[2] Outputs are CML. Values given are based on DC measurements.

[3] Outputs are designed to be a broadband match to 50 Ω impedance and are terminated with a 60 Ω resistor to GND.

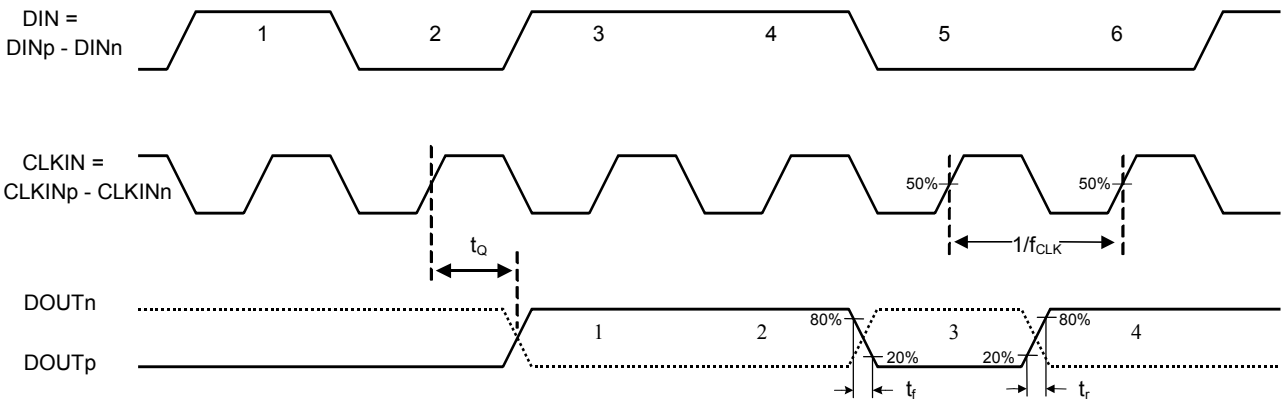
[4] Valid when clock -to -data phase is near center of CPM window.

[5] It should be noted that because the random and deterministic jitter of Inphi's high-speed logic parts are "in the noise" of the measurement techniques used, these specifications are conservative. The deterministic jitter ($J_D$) specified is the peak-to-peak total jitter measured using a $2^{31}$-1 PRBS data pattern. The random jitter ($J_R$) is the RMS jitter measured on a 1010... pattern. The jitter of the source and measurement equipment was not removed from the measured data.

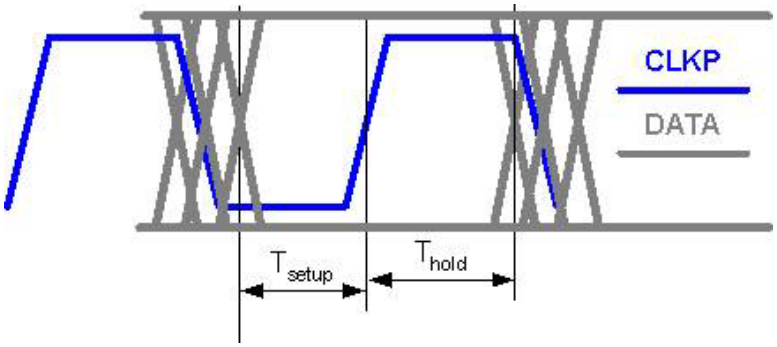
[6] Values based on design simulations.

[7] The setup and hold time specifications were determined from phase margin measurements and the assumption, supported by simulation, that Set-up and Hold times are equal to within a picosecond. See timing diagram on page 4.

# Timing Diagram




### Set-up and Hold Time Definition




# Truth Table

| $DIN_{k-1}$ | $DOUT_{k-1}$ | $DOUT_k$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$DOUT_k = DOUT_{k-1} \oplus DIN_{k-1}$

This equation corresponds to the well-known differential encoder equation $DOUT_k = DOUT_{k-1} \oplus DIN_k$, modified to include a one bit period delay in input data for retiming.

Notes:

DIN = DINp – DINn
DOUT = DOUTp – DOUTn

# DC Operating Characteristics

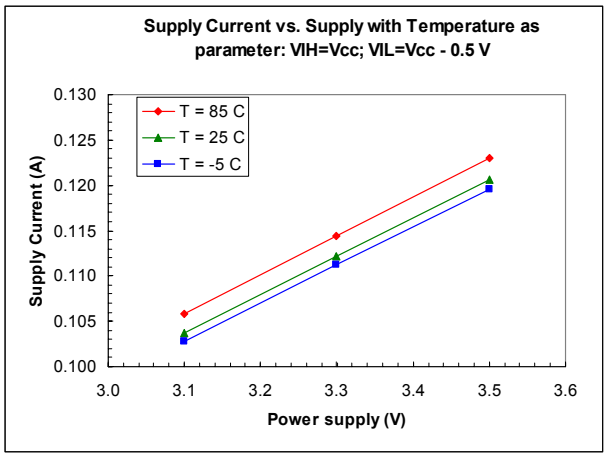



**Figure 1**. Supply current vs. power supply with temperature as parameter

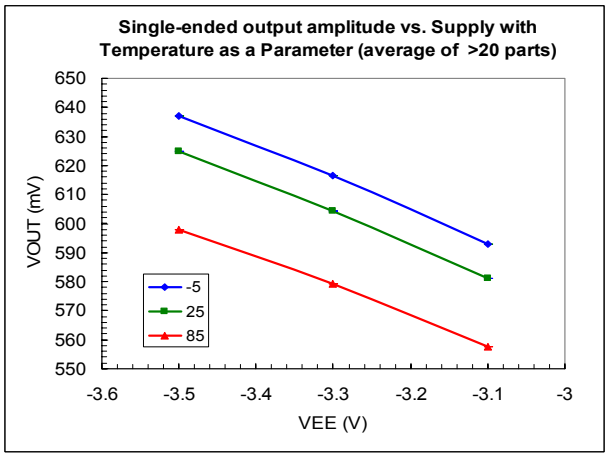



**Figure 2**. Single-ended peak-to-peak output vs. power supply with temperature as parameter

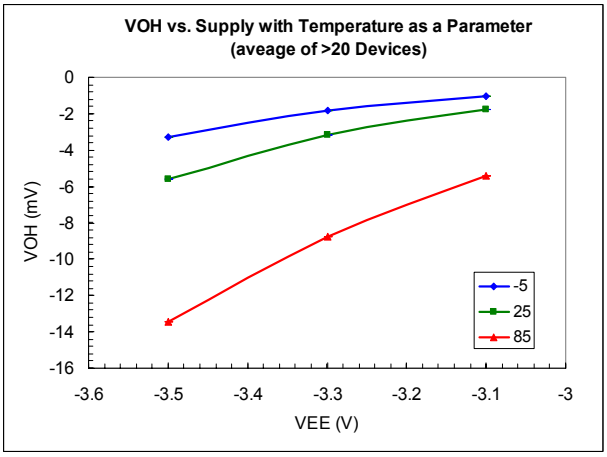



**Figure 3**. $V_{OH}$ vs. power supply with temperature as parameter

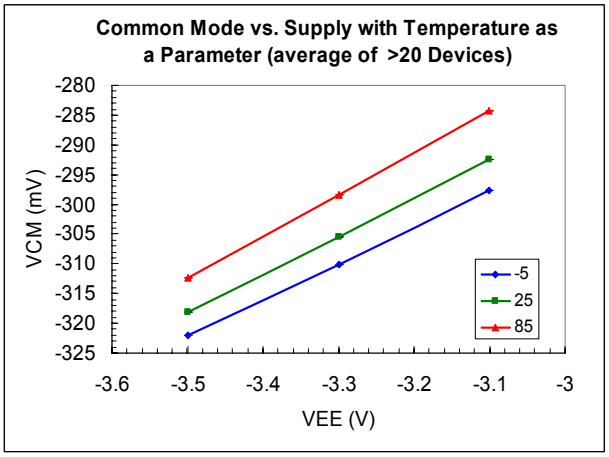



**Figure 4.** Output common mode vs. power supply with temperature as parameter

# Time Domain Operating Characteristics

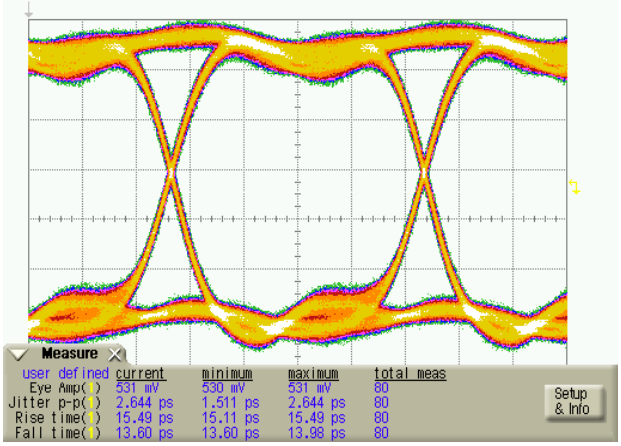



**Figure 5.** QFN Output eye diagram at 12.5 Gbps, T=25°C; $V_{EE}$=-3.3 V; 17 ps/div, 100 mV/div.

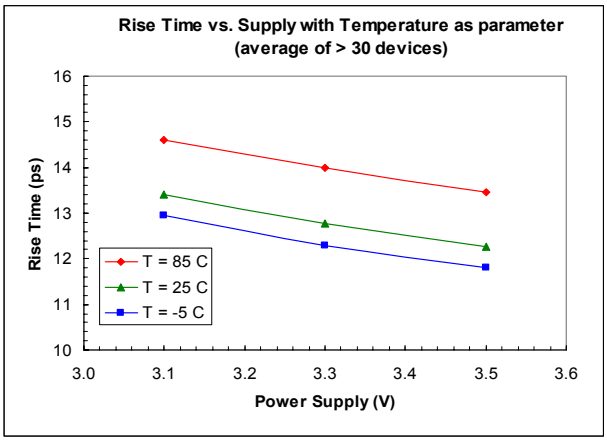



**Figure 6.** Rise time vs. power supply with temperature as parameter

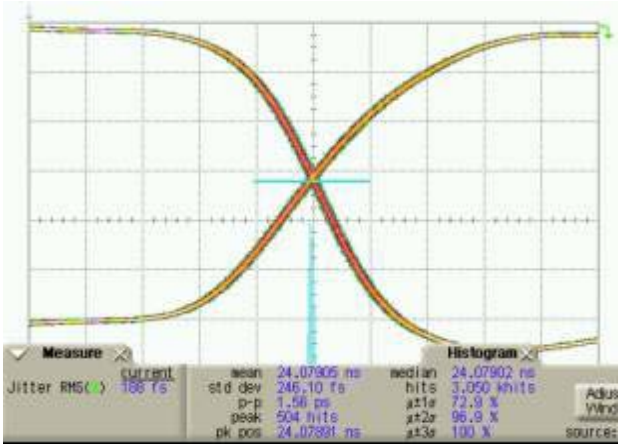



**Figure 7.** Histogram of output zero-crossing for 1010 output; T=25° C and $V_{EE}$ =-3.3 V

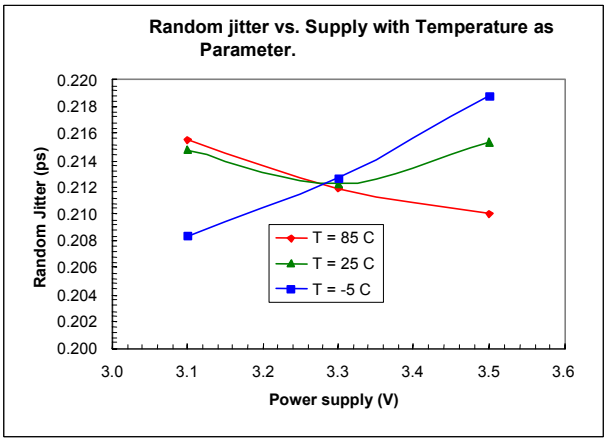



**Figure 8.** Random jitter vs. power supply with temperature as parameter

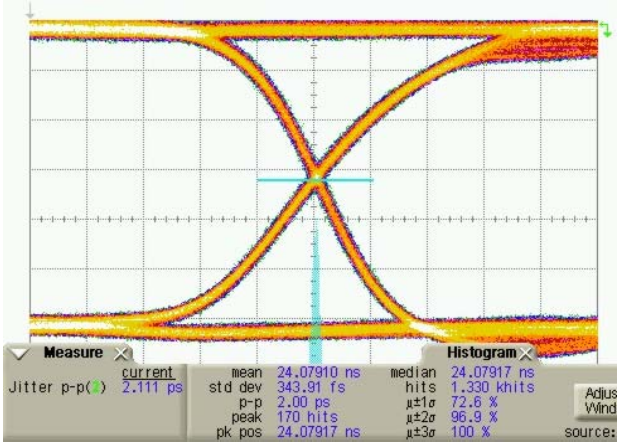



**Figure 9.** Die output crossing at 12.5 Gbps, T=25°C; $V_{EE}$=-3.3 V 5 ps/div.; Histogram used to measure peak-to-peak jitter.

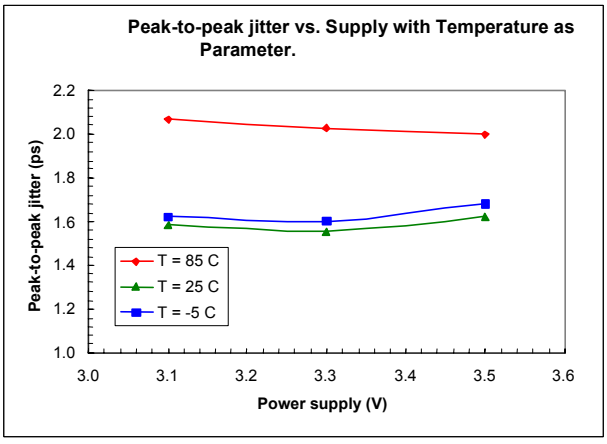



**Figure 10.** Peak-to-peak jitter vs. power supply with temperature as parameter

# Typical Return Losses

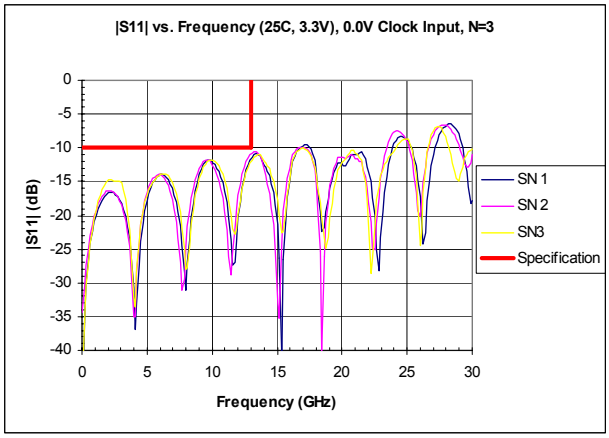



**Figure 11.** |S11| versus frequency of 3 QFN parts

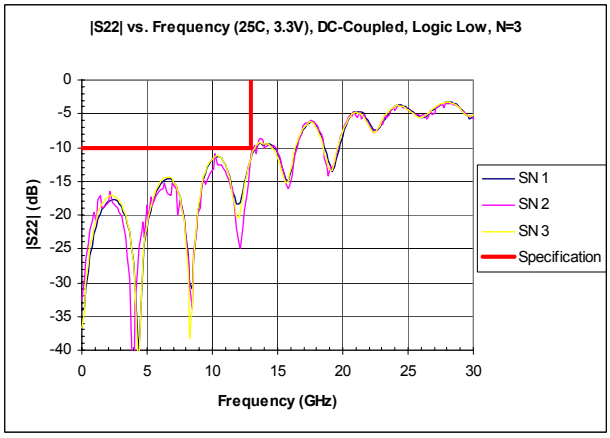



**Figure 12.** |S22| versus frequency with output in low state (worst case) of 33 parts; Die level data.

# Clock to Data Phase Margin

The clock to data phase margin is defined in degrees with 360° being a full period of the clock at 12.5 Gbps. It is measured by gradually adjusting the phase of the clock input relative to the data input and looking at the error rate of the differential encoder with a bit error rate tester. As indicated in figure 13, the 13650DE's phase margin is large: typically 290°.

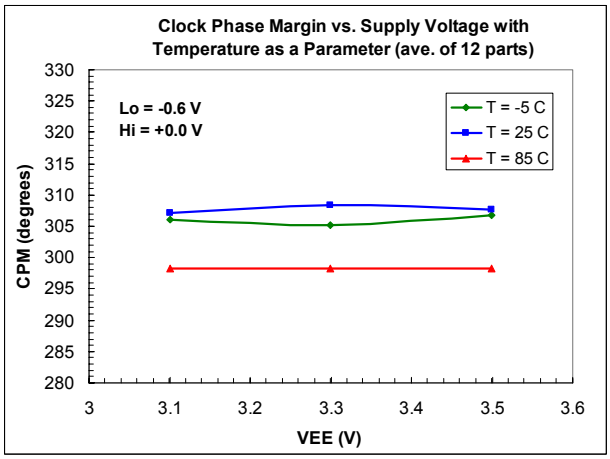
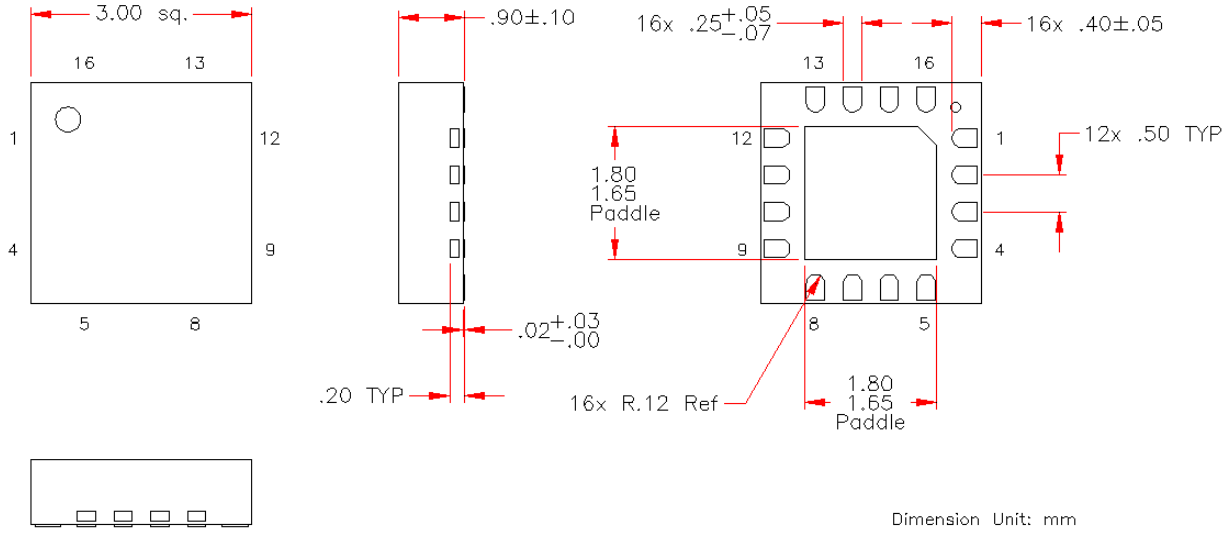



**Figure 13.** Clock phase margin vs. operating conditions at 12.5 Gbps

### Set-up and Hold Times

Direct measurement of the set-up and hold times is difficult because it involves accurately measuring the electrical delay of the clock and input from signal generators to the package pins and knowledge of the phase between the two signals at their respective generators. Since simulations indicate that the set-up and hold times are equal to within a picosecond, they can be determined from the phase margin. Since the phase margin is typically 290°, the typical set-up and hold times are one half of 70°/360° times 80 ps, or 8 ps.

# QFN Package Outline Drawing and Pin Assignment




| Name | Pin | Description | Function |
|---|---|---|---|
| DINp | 2 | Non-inverting Data Input | Input |
| DINn | 3 | Inverting Data Input | Input |
| CLKINp | 6 | Non-inverting Clock Input | Input |
| CLKINn | 7 | Inverting Clock Input | Input |
| DOUTp | 11 | Non-inverting Data Output | Output |
| DOUTn | 10 | Inverting Data Output | Output |
| GND | 1, 4, 5, 8, 9, 12, 14, Paddle | Ground | Supply |
| $V_{EE}$ | 13, 15, 16 | Power Supply: Connect to – 3.3 V | Supply |

Note:
The paddle must be electrically tied to ground.

# Order Information

| Part No. | Description |
|---|---|
| 13650DE-S02QFN | 13 Gbps Differential Encoder (–3.3 V Supply) in QFN Package |
| 13650DE-S02QFN-EVB | 13 Gbps Differential Encoder (–3.3 V Supply) in QFN Package on an Evaluation Board with SMA Connectors |

# Contact Information

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# Qualification Notification

The 13650DE-S02 is fully qualified. Please contact Inphi for the qualification report.

**Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.**

# Version Updates

**From Version 1.0 to 1.1 (dated 5/21/06):**

1. Added Thermal Resistance to Operating Conditions table (page 2).
2. Electrical Specifications table (page 3):
   a. Added notes 1 & 3.
   b. Changed note numbers on parameter descriptions.
3. Qualification Notification section:
   a. Added statement on radiation tolerance.

**From Version 1.1 to 1.2 (dated 2007-06-12):**

1. Removed radiation tolerance statement in Qualification Notification section (page 9).