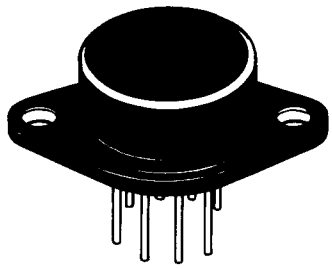
1464

High Speed Power MOSFET Driver Amplifier



The 1464 is a high speed, FET input, transconductance amplifier, designed to drive an external power MOSFET output stage. The use of an external output stage makes the 1464 extremely versatile, allowing the users to tailor the part to their requirements. It operates from ±10V to ±50V supplies.

Input bias current and offset voltage are guaranteed less than ±200pA and ±5mV, respectively. The 1464's high output impedance (30MΩ, typical) combined with its transconductance of 5,000 μmhos (typical), allows the user easily to construct power op-amps with open loop gains in excess of 100dB.

The 1464 is packaged in an 8-pin TO-3 package and the standard device is fully specified for -55°C to +125°C operation. The 1464-83 is specified over the -55°C to +125°C temperature range and meets the high reliability requirements of MIL-STD-883C, Class "B". This device may also be ordered screened to Class "S".

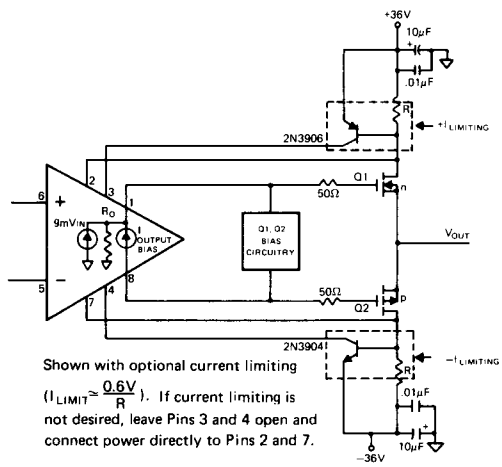


Figure 1. 1464 Standard Configuration

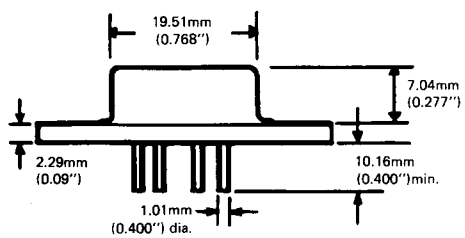
FEATURES

- FET Input
- Wide Supply Range: ±10V to ±50V
- User Selected VMOS Output Stage (No SOA Restrictions)
- Configure Class AB or Class B

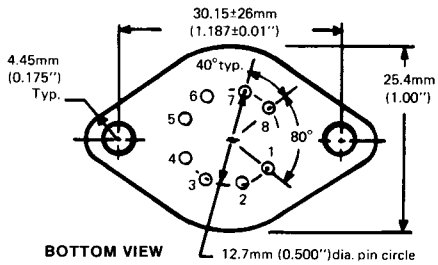
APPLICATIONS

- Deflection Yoke Drivers
- PWM Motor Drive Amplifiers
- Video Distribution Amplifiers
- ATE Pin Drivers
- High Performance Audio Amplifiers

PACKAGE DIMENSIONS



TO-3 METAL CAN



BOTTOM VIEW

PIN DESIGNATION
1. +IOUT OUTPUT SOURCE
2. +VCC
3. +ILIMIT
4. −ILIMIT
5. −IN
6. +IN
7. −VCC
8. −IOUT OUTPUT SINK

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±55V
Differential Input Voltage	±25V
Common Mode Input Voltage	$\pm V_{cc}$
Operating Temperature Range (Case)	−55°C to +125°C
Specified Temperature Range (Case)	
1464, 1464-83 (1)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

SPECIFICATIONS (+25°C, V_{cc} = ±36V, unless otherwise indicated.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS				
Offset Voltage: Initial	---	±2	±5	mV
Drift vs. Temperature	---	±20	---	µV/°C
Bias Current: Initial	---	±10	±200	pA
Drift vs. Temperature	---	Doubles every 10°C	---	
Common Mode Voltage Range for DC Linear Operation	---	±28	---	V
Common Mode Rejection Ratio	90	100	---	dB
TRANSFER CHARACTERISTICS				
Transconductance	---	5,000	---	µmhos
Open Loop Gain ($R_L = \infty$)	95	103	---	dB
OUTPUT CHARACTERISTICS				
Output Resistance	---	30	---	MΩ
Output Compliance Voltage ($R_L = \infty$)	±33	±35	---	V
Output Drive Current	---	±8	---	mA
Output Bias Current	5.5	6.5	7.5	mA
POWER REQUIREMENTS				
Supply Voltage Range	±10	±36	±50	V
Quiescent Current	---	±30	±36	mA

NOTES

1. Screened to the high reliability requirements of MIL-STD-883C, Class "B". May also be ordered screened to Class "S".

DESIGN CONSIDERATIONS

The 1464 is designed to drive a complementary power MOSFET output stage. The output stage can be run Class B (for low quiescent power dissipation) or Class AB (for low distortion, fast settling), as shown in Figure 2. The 1464 supplies a quiescent output bias current of ~6.5mA between pins 1 and 8 in order to drive the output FET bias circuitry (for Class B operation, short pins 1 and 8). The output bias current has a negative temperature coefficient of ~−12.5µA/°C (Figure 3); if the 1464 is mounted to the same heat sink as the output FETs, this will allow the use of a simple, single resistor bias scheme. If the output FETs are mounted on a separate heat sink, temperature compensation must be provided externally; one way of doing this is shown in Figure 4. This circuit, known as a V_{BE} multiplier, will provide a temperature coefficient of ~−3.2mV/°C per volt of bias voltage (transistor Q1 must be mounted on the same heat sink as the output FETs).

The 1464 is a differential input transconductance amplifier. To construct a high performance operational amplifier, it is only necessary to add a high input impedance output stage. The low-frequency voltage gain of the 1464 is determined by its transconductance and load resistance:

$A_{V/V} = g_m(R_L \| R_O)$ where:

g_m = transconductance of 1464 ≅ 5,000µmhos (typical)

R_L = load resistance (input resistance of external output stage)

R_O = output resistance of 1464 ≅ 30MΩ (typical)

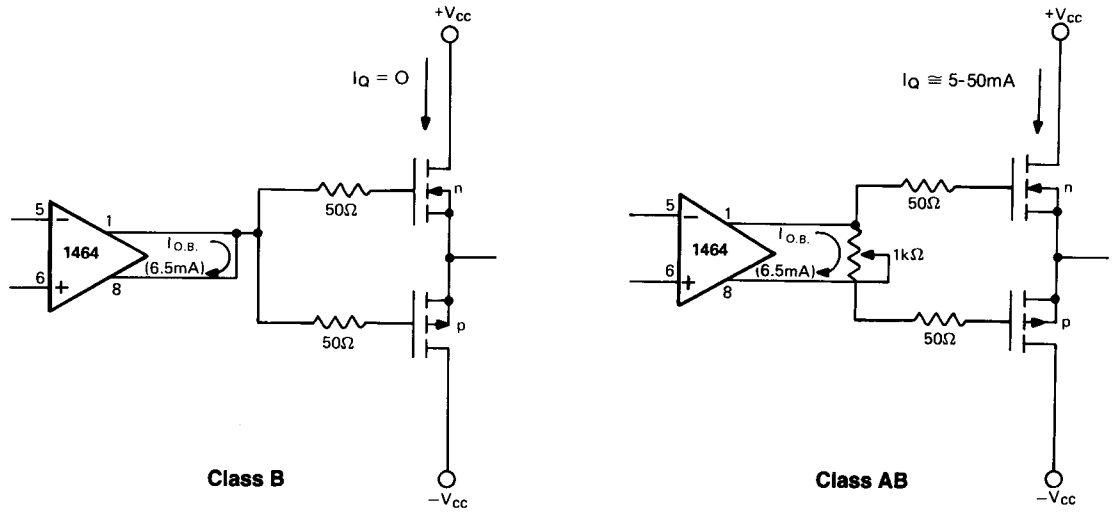


Figure 2. Ouput Stage Biasing

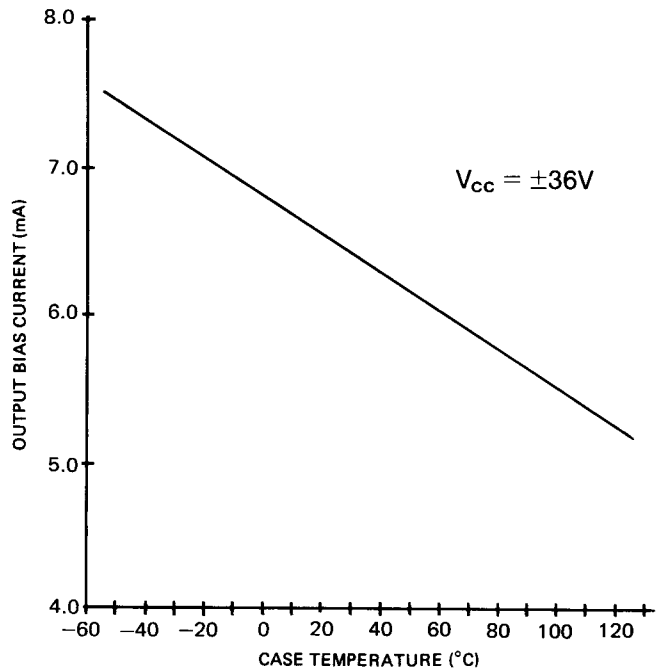


Figure 3. 1464 IOutput Bias vs. TCase

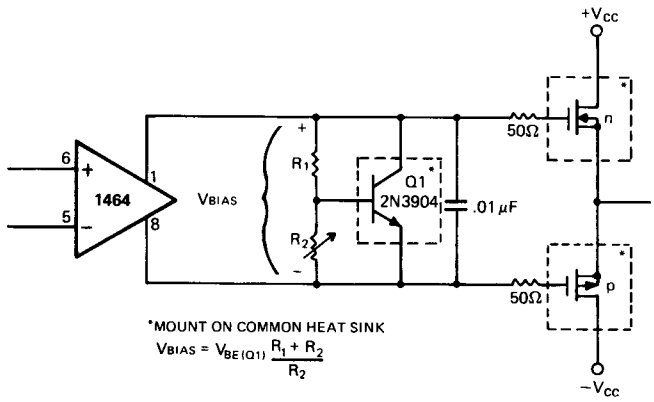


Figure 4. Biasing Output Stage Using a V_{BE} Multiplier.

By using a MOSFET output stage, the load resistance is maximized, and thus high gain is achieved. The maximum gain achievable is limited to ~103dB (typical) by the output resistance of the 1464 (30MΩ typical).

The input capacitance of the output stage creates a dominant pole in the amplifier transfer function. Thus, the 1464 is compensated by the input capacitance of the output stage. Increasing this capacitance will increase stability, but will reduce slew rate and frequency response. An alternative method of compensation is to lower the input resistance of the output stage; this does not affect slew rate as much, but does reduce open loop gain at all frequencies. Taking load capacitance into account, the gain of the amplifier will be:

$$A_{V/V} = \frac{g_m(R_L \| R_O)}{1+2\pi(R_L \| R_O)C_L f}$$

where C_L = load capacitance (input capacitance of output stage)

Several typical circuits are shown in Figures 6, 7, 8 and 9; their performance is compared in Figure 10. Ferranti/Supertex FETs were chosen as the output devices due to their comparatively low capacitance, which allows higher slew rates and wider bandwidths. Other FETs may be used if desired, or FETs may be paralleled for increased current output.

Current Limiting

The 1464 has provisions for current limiting via pins 3 ($+I_{LIMIT}$) and 4 ($-I_{LIMIT}$). The basic current limit configuration, shown in Figure 1, requires two transistors and two resistors. The current limit resistors are chosen such that:

$$R = \frac{0.6V}{I_{LIMIT}}$$

where I_{LIMIT} = desired limit current

R = current limit resistor

Different positive and negative current limits may be used, if desired.

Figure 5 shows a foldback current limiting scheme which limits short circuit current to a small fraction of the full load current. The value of the limiting resistors may be determined as follows:

$$R_A \cong \frac{0.6V}{I_{MAX}}$$

$$R_B \cong 300\ (\frac{V_{cc}}{0.6V - R_A I_{SC}} - 1)$$

where

$I_{MAX} = I_{OUT}$ at maximum V_{OUT}

I_{SC} = Short circuit current (I_{OUT} at V_{OUT} = OV)

If no current limiting is desired, pins 3 and 4 should be left open and power should be applied directly to pins 2 and 7.

Bypassing

For optimum performance and noise rejection, power supplies should be bypassed with 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors. These should be mounted as close to the 1464 as possible. Additional bypassing should be used at the output stage, with a minimum of 10μF per amp of output current. These capacitors should be tantalum also, and should be mounted close to the drains of the output FETs. Layout and bypassing are critical for short settling times; more bypassing may be required if this parameter is critical.

Thermal Considerations

In most applications the 1464 and its output stage will require a heat sink. If the 1464 is mounted on the same heat sink as the output stage, the user will have to consider its power dissipation (2.6W maximum at $V_{cc} = \pm 36V$) as well as the power dissipation of the output transistors. In circuits where the 1464 is not mounted on the same heat sink as the output stage, the 1464 will generally require a separate, small heat sink when operated at supply voltages greater than $V_{cc} = \pm 20V$. The thermal resistance of the 1464 (case to ambient) is approximately 30°C/W. Thus, operating at $V_{cc} = \pm 36V$ ($I_{cc} = \pm 36mA$ max., $P_D = 2.6W$ max.) without a heat sink would cause the case temperature to rise (2.6W) (30°C/W) = 78°C above ambient. A small, clip-on heat sink, such as the AAVID 4791B, would reduce this to approximately 38°C above ambient. A larger heat sink may be required at higher voltages, or at high ambient temperatures.

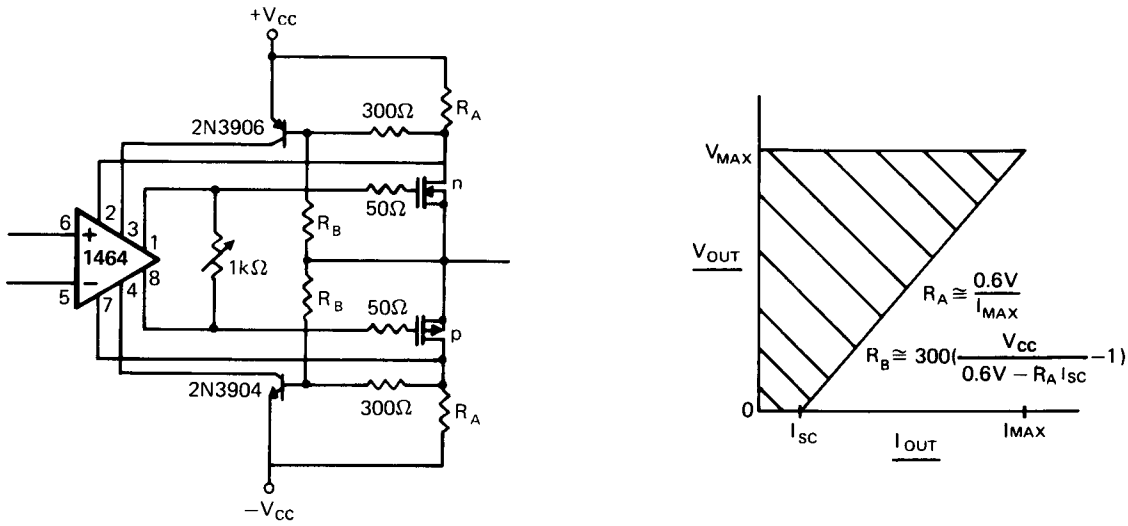
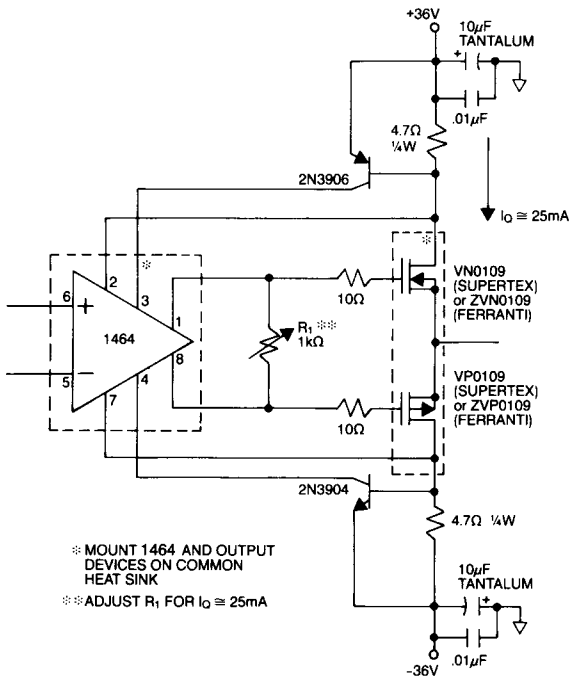


Figure 5. 1464 With Foldback Current Limiting

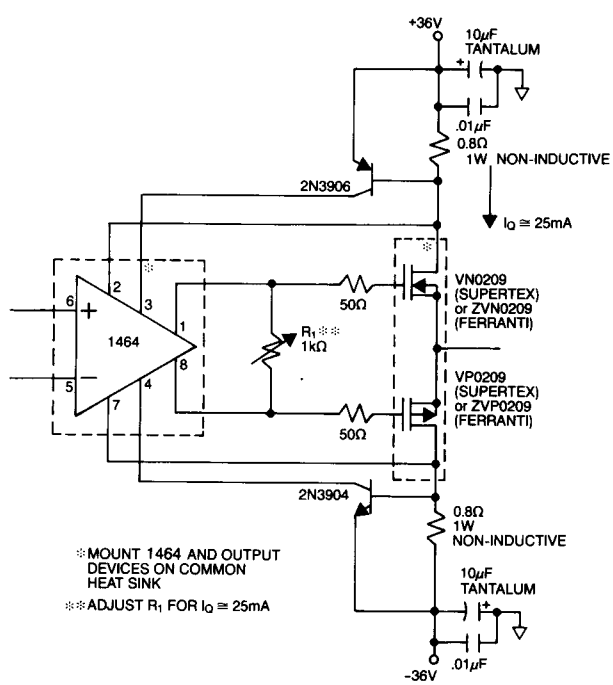


TYPICAL CHARACTERISTICS (V_{CC} = ±36V, T_C = 25°C, R_L = 300Ω)

Slew Rate	±500V/μs
Unity Gain Bandwidth	26MHz
Open Loop Gain (DC)	103dB
Output Voltage (I_{OUT} = 100mA)	±30V
Output Short Circuit Current	±125mA
Settling Time (A_{CL} = −5, ±10V Step, 0.1%)	110ns

STABLE FOR NOISE GAINS ≥ 3

Figure 6. ±30V, ±100mA Output High Speed Op Amp

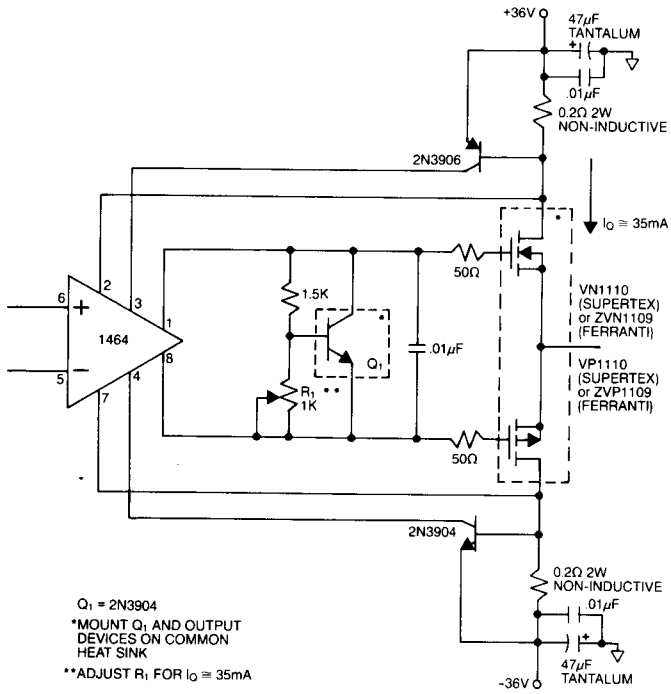


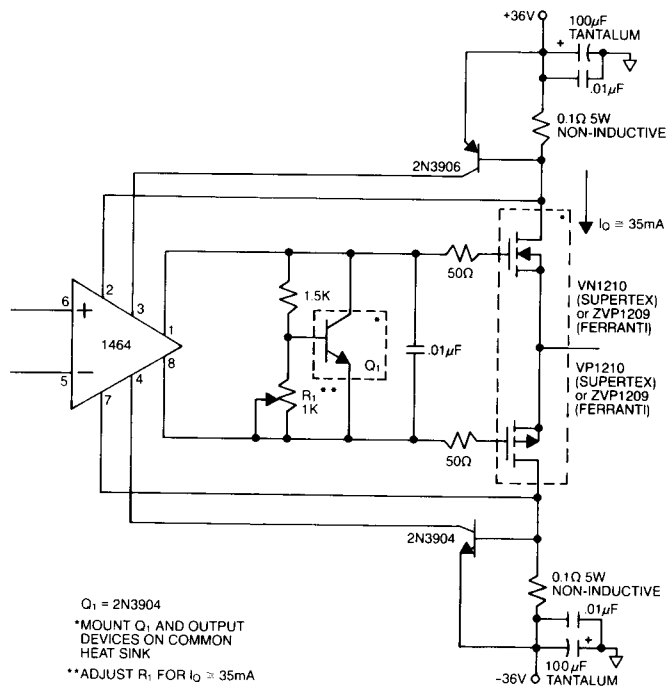
TYPICAL CHARACTERISTICS (V_{CC} = ±36V, T_C = 25°C, R_L = 50Ω)

Slew Rate	±175V/μs
Unity Gain Bandwidth	19MHz
Open Loop Gain (DC)	103dB
Output Voltage (I_{OUT} = 560mA)	±28V
Output Short Circuit Current	750mA
Settling Time (A_{CL} = −1, ±10V Step, 0.1%)	150ns

UNITY GAIN STABLE

Figure 7. ±28V, ±560mA Output High Speed Op Amp





TYPICAL CHARACTERISTICS (V_{CC} = ±36V, T_C = 25°C, R_L = 15Ω)

Slew Rate	±100V/μs
Unity Gain Bandwidth	9MHz
Open Loop Gain (DC)	100dB
Output Voltage (I_{OUT} = 2A)	±30V
Output Short Circuit Current	3A
Settling Time (A_{CL} = −1, ±10V Step, 0.1%)	230ns
UNITY GAIN STABLE	

Figure 8. ±30V, ±2A Output Op Amp

TYPICAL CHARACTERISTICS (V_{CC} = ±36V, T_C = 25°C, R_L = 5.6Ω)

Slew Rate	±50V/μs
Unity Gain Bandwidth	2MHz
Open Loop Gain (DC)	96dB
Output Voltage (I_{OUT} = 5A)	±28V
Output Short Circuit Current	6A
Settling Time (A_{CL} = −1, ±10V Step, 0.1%)	750ns
UNITY GAIN STABLE	

Figure 9. ±28V, ±5A Output Op Amp

TYPICAL PERFORMANCE

V_{CC} = ±36V, T_C = 25°C, R_L = Rated Load (See Notes)

P_{OUT}	±V_{OUT}	±I_{OUT}	Slew Rate	Settling Time (0.1%, ±10V Step)	Unity Gain Bandwidth	A_{OL}	Circuit/See Figure No.	Notes
3W	±30V	±100mA	±500V/μs	110ns (A_{CL} = −5)	26MHz	103dB	6	R_L = 300Ω; Stable for Noise Gains ≥ 3
15.7W	±28V	±560mA	±175V/μs	150ns (A_{CL} = −1)	19MHz	103dB	7	R_L = 50Ω; Unity Gain Stable
60W	±30V	±2A	±100V/μs	230ns (A_{CL} = −1)	9MHz	100dB	8	R_L = 15Ω; Unity Gain Stable
140W	±28V	±5A	±50V/μs	750ns (A_{CL} = −1)	2MHz	96dB	9	R_L = 5.6Ω; Unity Gain Stable

Figure 10. Comparison of Amplifier Performance