



15N10

Power MOSFET

14.7A, 100V (D-S) N-CHANNEL POWER MOSFET

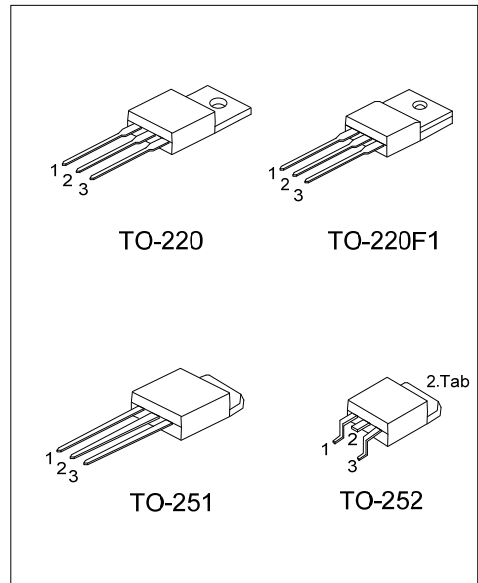
■ DESCRIPTION

The UTC **15N10** is an N-Channel enhancement MOSFET, it uses UTC's advanced technology to provide customers with a minimum on-state resistance, high switching speed and low gate charge.

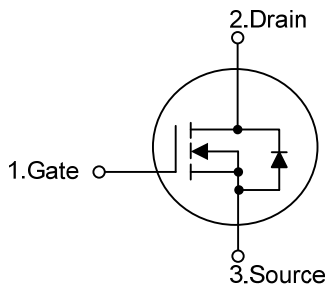
The UTC **15N10** is suitable for high efficiency switching DC/DC converter, LCD display inverter and load switch.

■ FEATURES

- * $R_{DS(ON)} \leq 100 \text{ m}\Omega @ V_{GS}=10V, I_D=8.0A$
- $R_{DS(ON)} \leq 110 \text{ m}\Omega @ V_{GS}=4.5V, I_D=8.0A$
- * High switching speed



■ SYMBOL



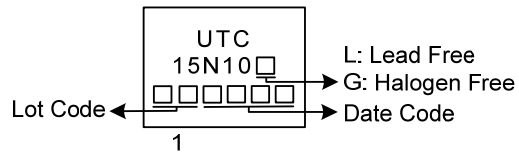
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
15N10L-TA3-T	15N10G-TA3-T	TO-220	G	D	S	Tube
15N10L-TF1-T	15N10G-TF1-T	TO-220F1	G	D	S	Tube
15N10L-TM3-T	15N10G-TM3-T	TO-251	G	D	S	Tube
15N10L-TN3-R	15N10G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>15N10G-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TA3: TO-220, TF1: TO-220F1, TM3: TO-251 TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

PARAMETER			SYMBOL	RATINGS	UNIT
Drain-Source Voltage			V_{DSS}	100	V
Gate-Source Voltage			V_{GSS}	± 20	V
Drain Current	Continuous	$T_C=25^{\circ}\text{C}$	I_D	14.7	A
		$T_C=70^{\circ}\text{C}$		13.6	A
	Pulsed		I_{DM}	30	A
Power Dissipation	$T_C=25^{\circ}\text{C}$	TO-220	P_D	60	W
		TO-220F1		31	W
		TO-251		34.7	W
		TO-252			
Operating Junction Temperature			T_J	-55 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-220F1	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
	TO-251/TO-252		110	$^{\circ}\text{C}/\text{W}$
Junction to Case (Note)	TO-220	θ_{JC}	2.5	$^{\circ}\text{C}/\text{W}$
	TO-220F1		4.03	$^{\circ}\text{C}/\text{W}$
	TO-251/TO-252		3.6 (Note)	$^{\circ}\text{C}/\text{W}$

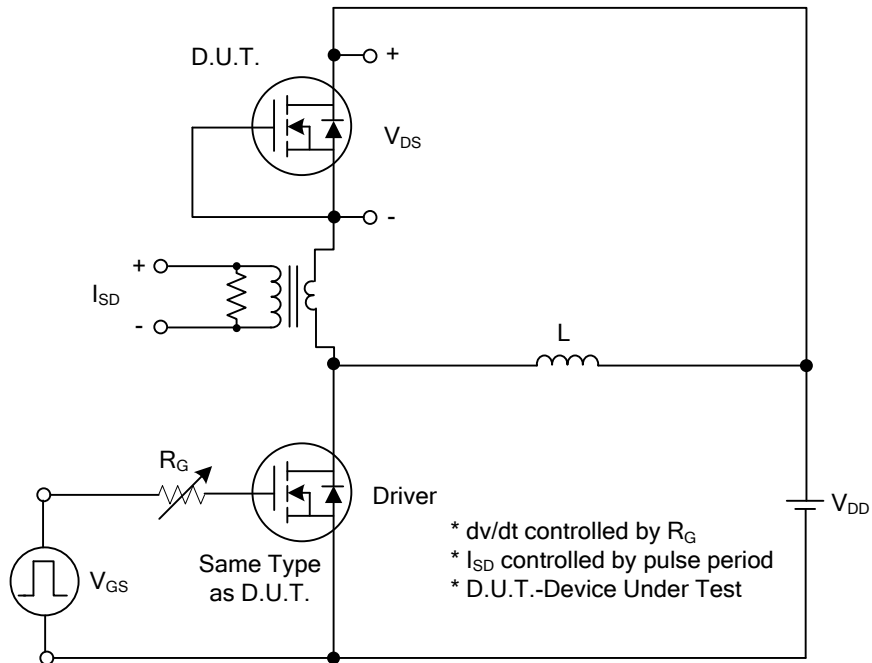
Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$, unless otherwise specified)

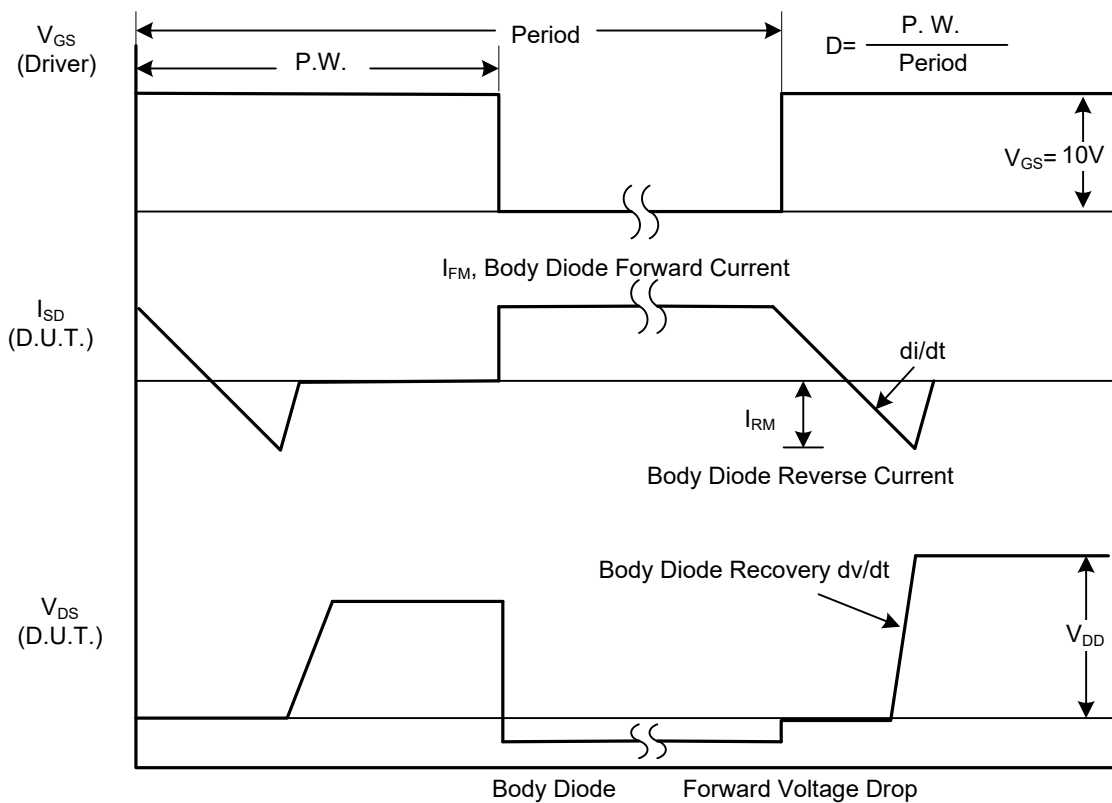
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	100			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=+20\text{V}$, $V_{DS}=0\text{V}$			+100	nA
		$V_{GS}=-20\text{V}$, $V_{DS}=0\text{V}$			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1.0		3.0	V
Drain-Source On-State Resistance (Note)	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=8.0\text{A}$			100	m Ω
		$V_{GS}=4.5\text{V}$, $I_D=8.0\text{A}$			110	m Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=15\text{V}$, $f=1\text{MHz}$		1411		pF
Output Capacitance	C_{OSS}		78		pF	
Reverse Transfer Capacitance	C_{RSS}		65		pF	
Gate-Resistance	R_G	$V_{DS}=0\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$		0.81		Ω
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{GS}=10\text{V}$, $V_{DS}=80\text{V}$, $I_D=15\text{A}$		34		nC
Total Gate Charge	Q_G	$V_{GS}=4.5\text{V}$, $V_{DS}=80\text{V}$, $I_D=15\text{A}$		18.4		nC
Gate to Source Charge	Q_{GS}		5.5		nC	
Gate to Drain Charge	Q_{GD}		8		nC	
Turn-ON Delay Time	$t_{D(ON)}$		13		ns	
Rise Time	t_R	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=15\text{A}$, $R_G=25\Omega$		22		ns
Turn-OFF Delay Time	$t_{D(OFF)}$		100		ns	
Fall-Time	t_F		43		ns	
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=8\text{A}$, $V_{GS}=0\text{V}$		0.9	1.2	V

Note: Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

■ TEST CIRCUITS AND WAVEFORMS

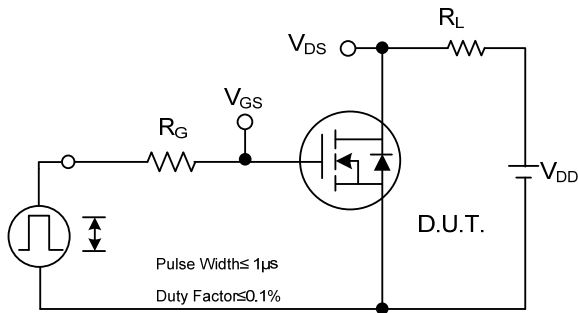


Peak Diode Recovery dv/dt Test Circuit

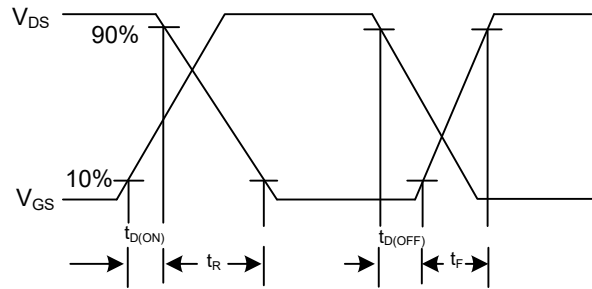


Peak Diode Recovery dv/dt Waveforms

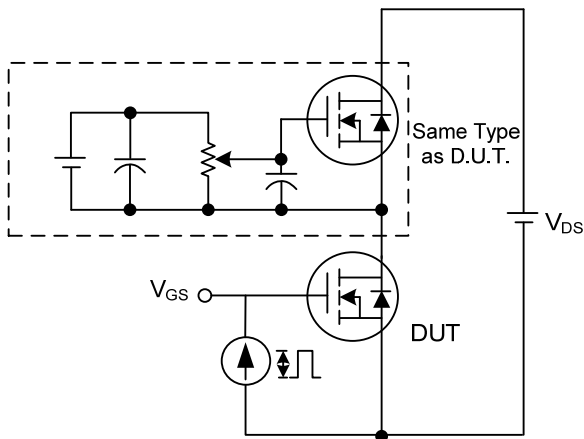
TEST CIRCUITS AND WAVEFORMS



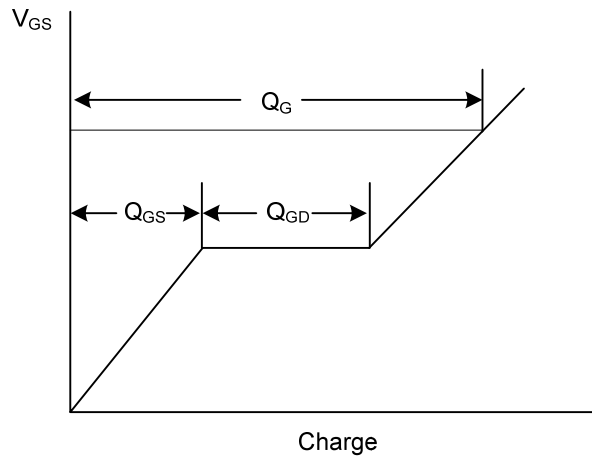
Switching Test Circuit



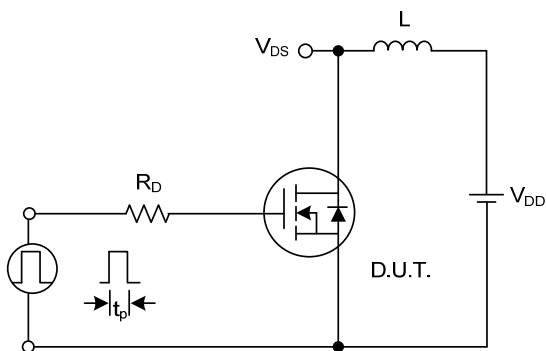
Switching Waveforms



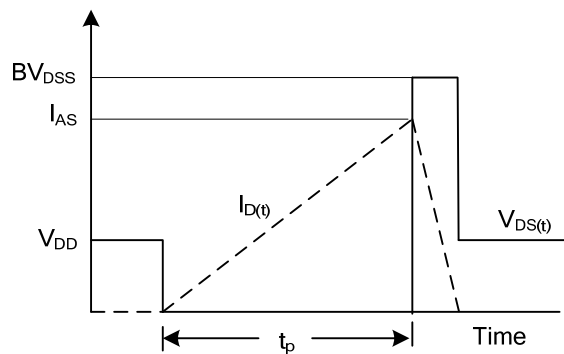
Gate Charge Test Circuit



Gate Charge Waveform

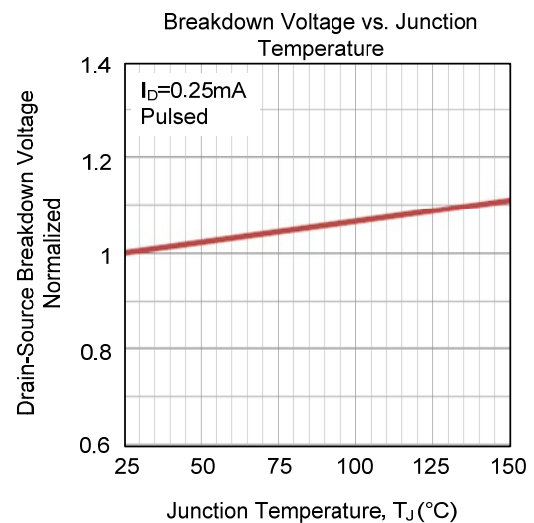
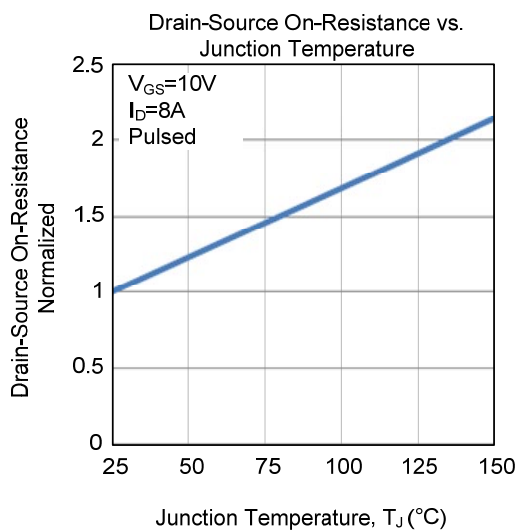
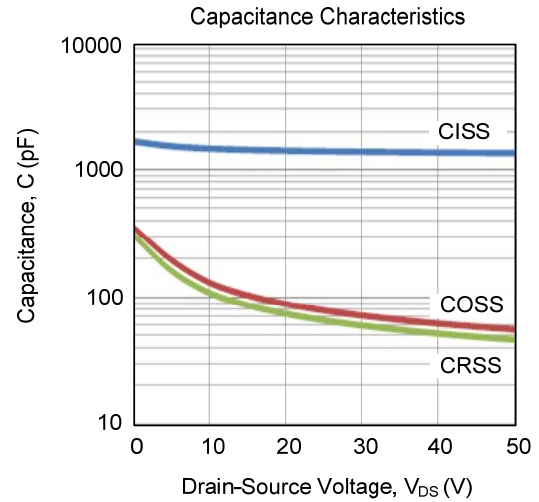
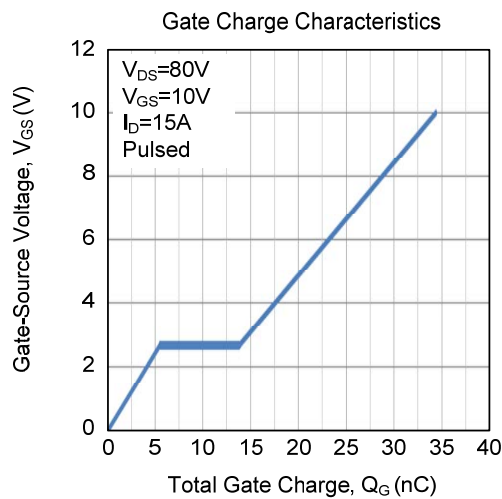
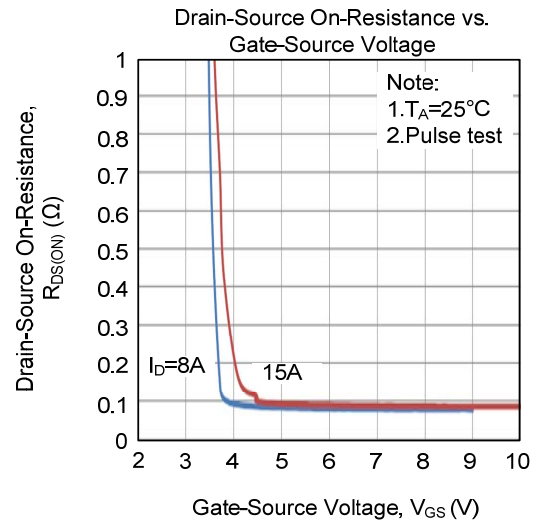
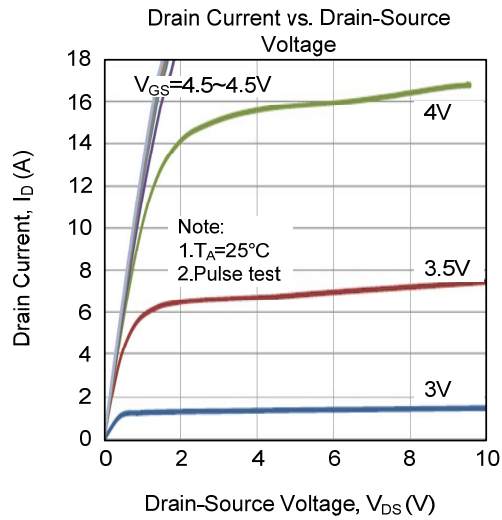


Unclamped Inductive Switching Test Circuit

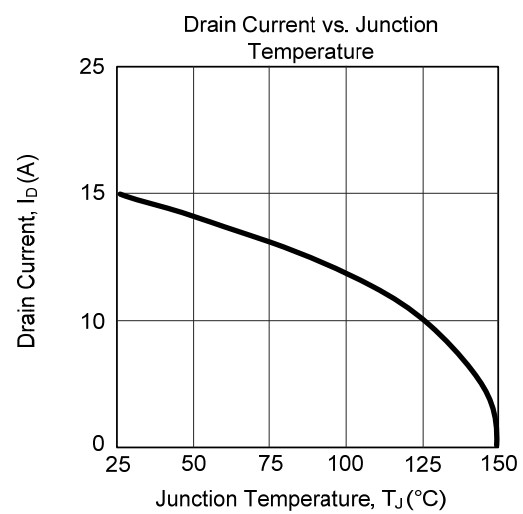
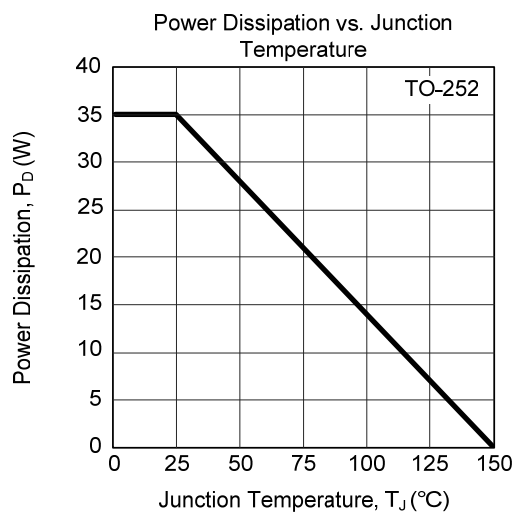
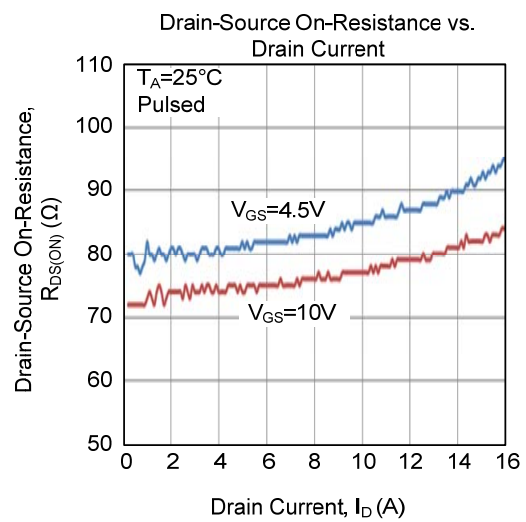
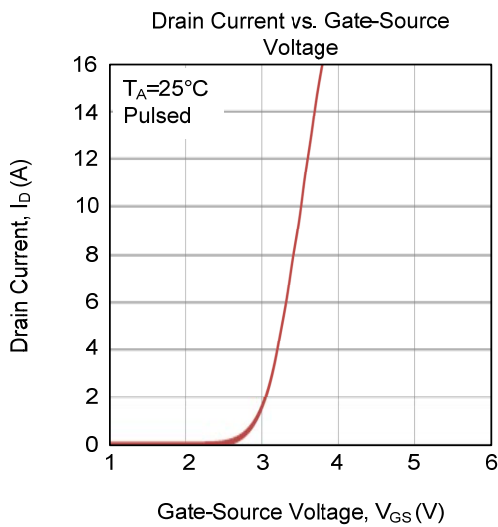
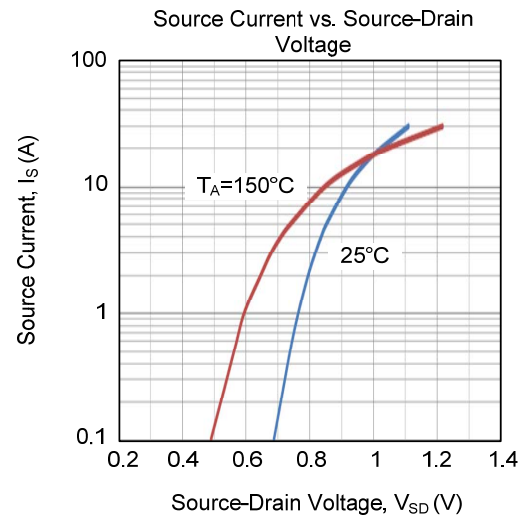
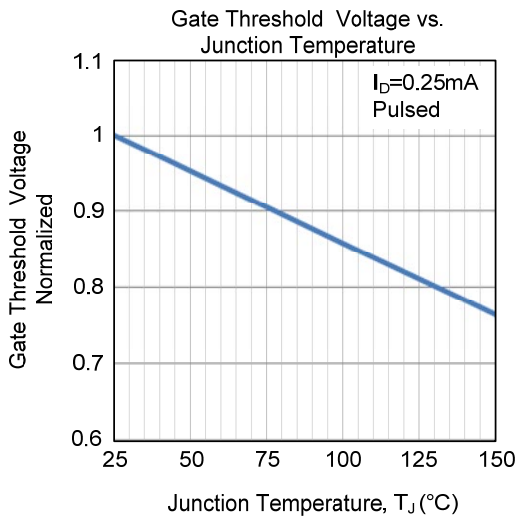


Unclamped Inductive Switching Waveforms

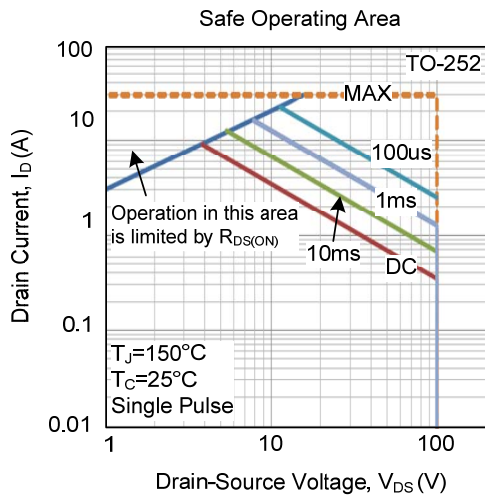
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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