



15N65K-MT

Power MOSFET

15A, 650V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **15N65K-MT** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

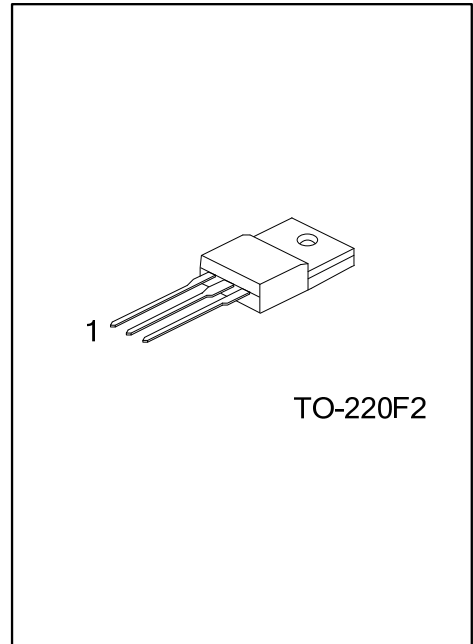
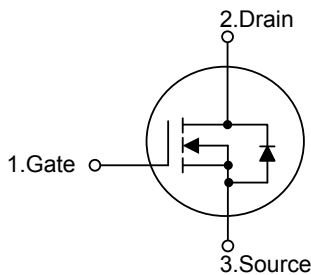
The UTC **15N65K-MT** is generally applied in high efficiency switch mode power supplies.

FEATURES

* $R_{DS(ON)} < 0.6\Omega$ @ $V_{GS} = 10V, I_D = 7.5A$

* High Switching Speed

SYMBOL



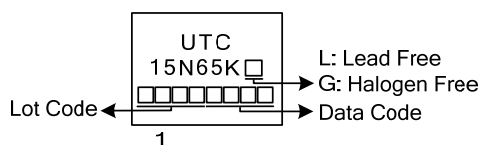
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
15N65KL-TF2-T	15N65KG-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>15N65KL-TF2-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube (2) TF2: TO-220F2 (3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified.) (Note 5)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous $T_C=25^\circ\text{C}$	I_D	15	A
	Pulsed (Note 2)	I_{DM}	60	A
Avalanche Current (Note 2)		I_{AR}	15	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	750	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	15	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)		P_D	52	W
Derate above 25°C			0.416	W/ $^\circ\text{C}$
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating; Pulse width limited by maximum junction temperature
3. $L=6.7\text{mH}$, $I_{AS}=15\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
4. $I_{SD}\leq 15\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
5. Drain current limited by maximum junction temperature

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.4	$^\circ\text{C}/\text{W}$

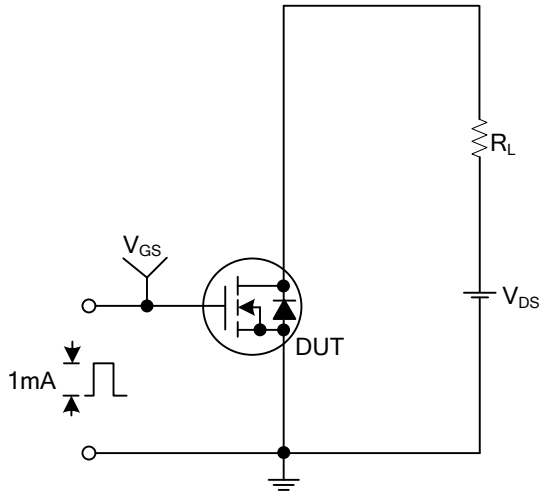
■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$, $T_J=25^\circ\text{C}$	650			V	
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C , $I_D=250\mu\text{A}$		0.5		$\text{V}/^\circ\text{C}$	
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$,			1	μA	
Gate- Source Leakage Current	Forward	I_{GSS} $V_{GS}=+30\text{V}$, $V_{DS}=0\text{V}$			+100	nA	
	Reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$			-100	nA	
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	2.0		4.0	V	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=7.5\text{A}$			0.60	Ω	
DYNAMIC PARAMETERS							
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$		2000		pF	
Output Capacitance	C_{OSS}				210		pF
Reverse Transfer Capacitance	C_{RSS}				11		pF
SWITCHING PARAMETERS							
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DS}=30\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		110		ns	
Rise Time	t_R				128		ns
Turn-OFF Delay Time	$t_{D(OFF)}$				244		ns
Fall-Time	t_F			116		ns	
Total Gate Charge	Q_G	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $I_D=1.3\text{A}$ (Note 1, 2)		47.3		nC	
Gate to Source Charge	Q_{GS}				13		nC
Gate to Drain ("Miller") Charge	Q_{GD}				13.2		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current	I_S				15	A	
Maximum Body-Diode Pulsed Current	I_{SM}				60	A	
Drain-Source Diode Forward Voltage	V_{SD}	$I_{SD}=15\text{A}$, $V_{GS}=0\text{V}$			1.4	V	

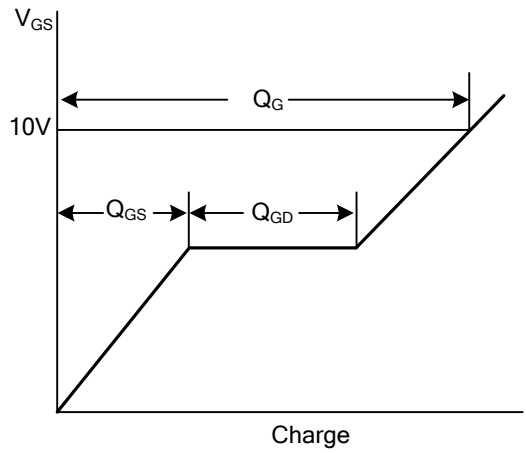
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$; Duty Cycle $\leq 2\%$

2. Essentially Independent of Operating Temperature Typical Characteristics

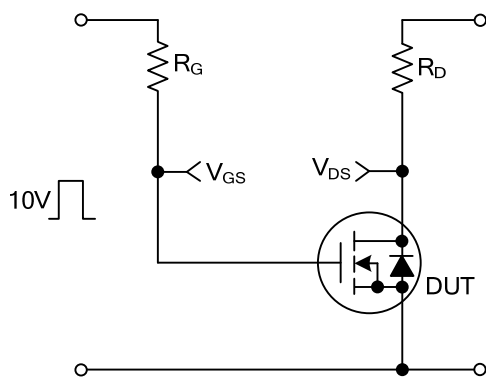
TEST CIRCUITS AND WAVEFORMS



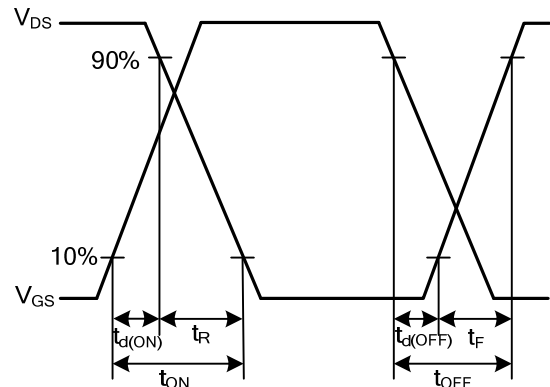
Gate Charge Test Circuit



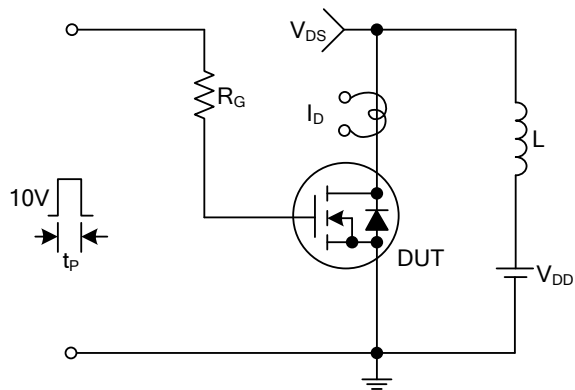
Gate Charge Waveforms



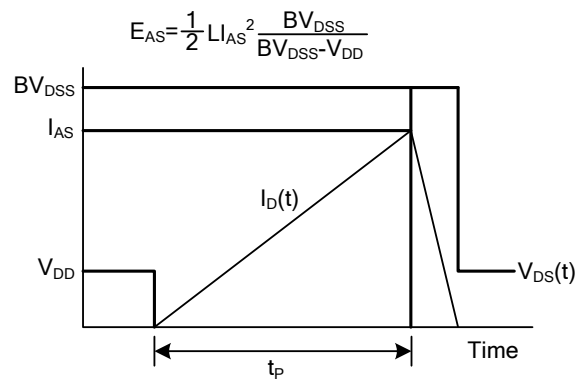
Resistive Switching Test Circuit



Resistive Switching Waveforms



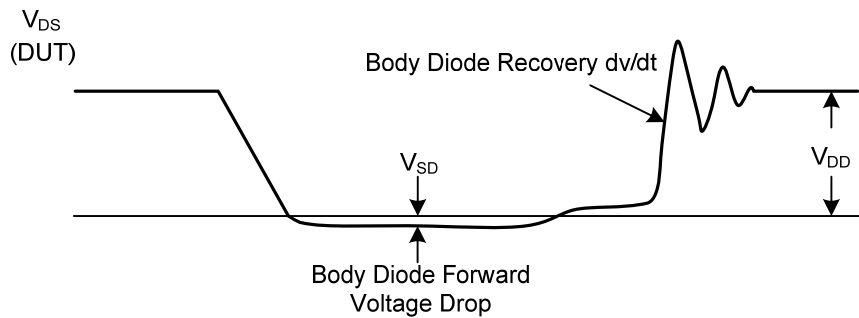
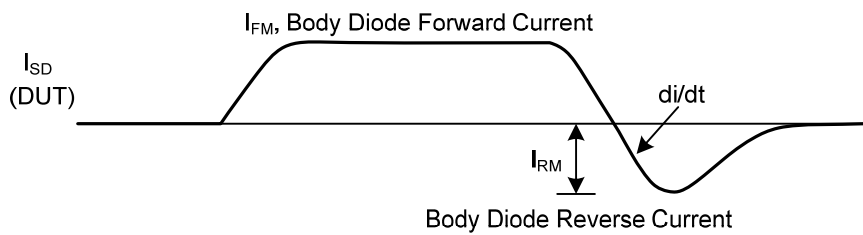
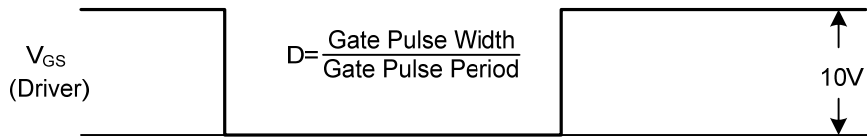
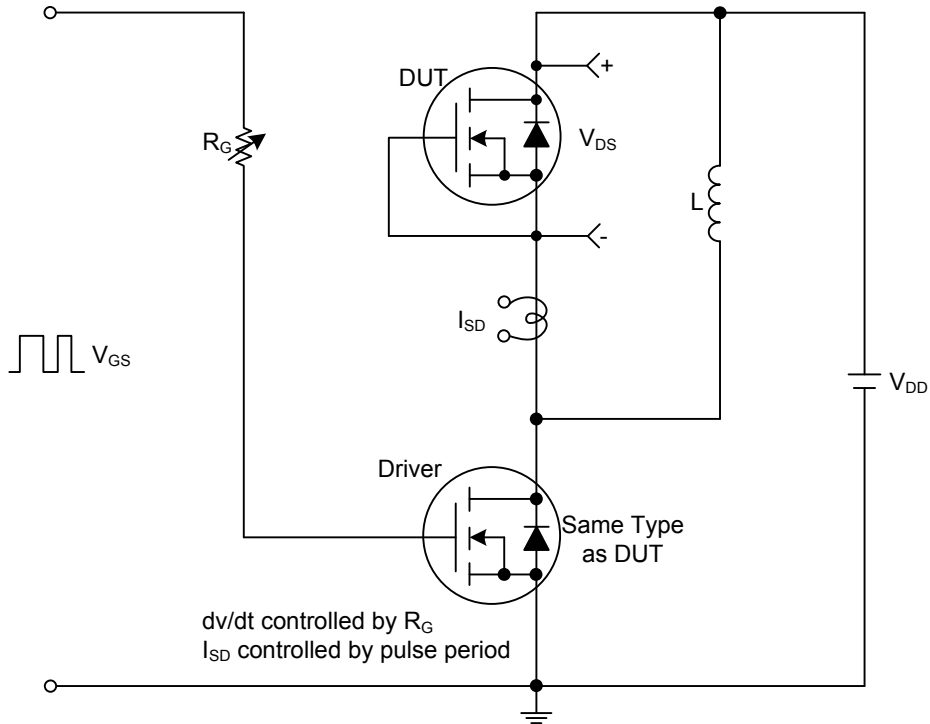
Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)

Peak Diode Recovery dv/dt Test Circuit & Waveforms



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