



15NM50

Preliminary

Power MOSFET

**15A, 500V N-CHANNEL
SUPER-JUNCTION MOSFET**

■ DESCRIPTION

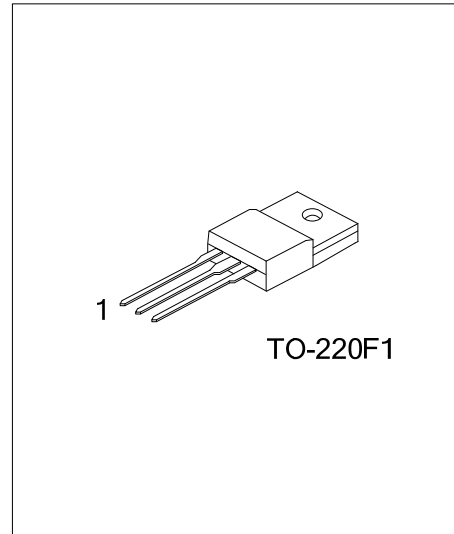
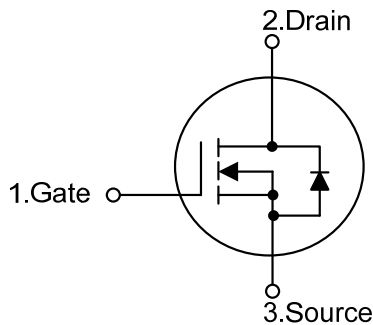
The UTC 15NM50 is an Super Junction MOSFET Structure . It uses UTC advanced planar stripe, DMOS technology to provide customers perfect switching performance, minimal on-state resistance.

The UTC 15NM50 is universally applied in electronic lamp ballasts based on half bridge topology, high efficiency switched mode power supplies, active power factor correction, etc.

■ FEATURES

- * $R_{DS(ON)} < 0.35\Omega @ V_{GS}=10V, I_D=7.5A$
- * By using Super Junction Structure
- * Fast Switching
- * With 100% Avalanche Tested

■ SYMBOL



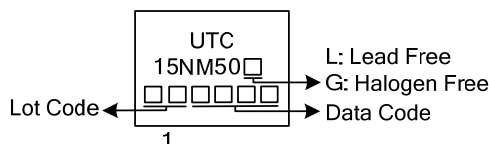
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
15NM50L-TF1-T	15NM50G-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>15NM50L-TF1-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) T: Tube (2) TF1:TO-220F1 (3) L: Lead Free, G: Halogen Free and Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	500	V
Gate to Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	15 (Note 2)
		$T_C=100^\circ\text{C}$	7 (Note 2)
Pulsed Drain Current (Note 3)	I_{DM}	44 (Note 2)	A
Single Pulsed Avalanche Energy(Note 4)	E_{AS}	225	mJ
Peak Diode Recovery dv/dt (Note 5)	dv/dt	4.5	V/ns
Power Dissipation	P_D	$T_C=25^\circ\text{C}$	52
		Derate above 25°C	0.416
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Drain current limited by maximum junction temperature
3. Repetitive Rating : Pulse width limited by maximum junction temperature
4. $L=2\text{mH}$, $I_{AS}=15\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
5. $I_{SD}\leq 11\text{A}$, $di/dt\leq 200\text{A}/\mu\text{s}$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.4	$^\circ\text{C}/\text{W}$

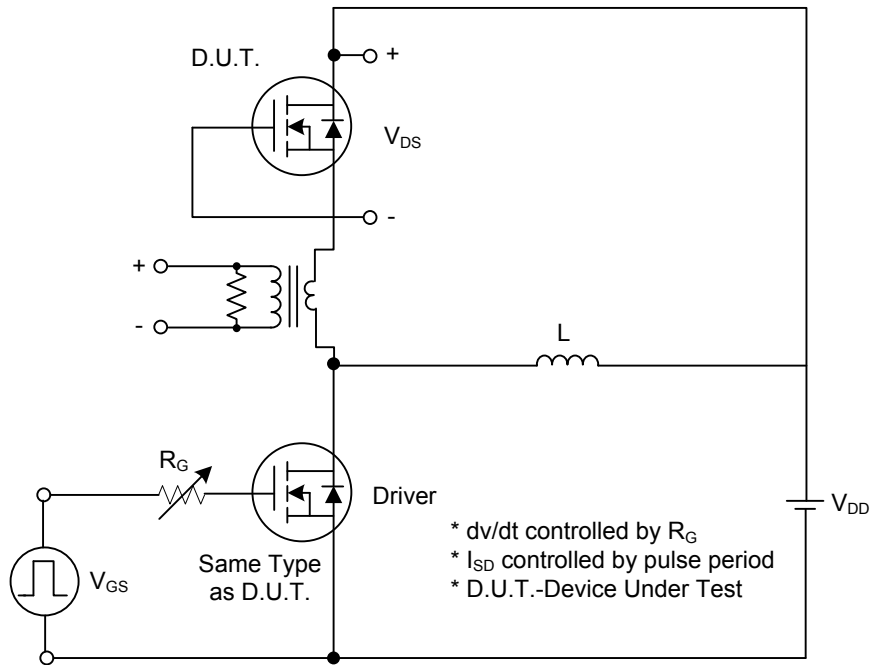
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	500			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D=250\mu\text{A}$, Referenced to 25°C		0.5		$\text{V}/^\circ\text{C}$
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
		$V_{DS}=500\text{V}$, $T_J=125^\circ\text{C}$			100	μA
Gate-Source Leakage Current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=7.5\text{A}$			0.35	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$		625		pF
Output Capacitance	C_{OSS}			330		pF
Reverse Transfer Capacitance	C_{RSS}			15		pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ $V_{GS}=10\text{V}$ (Note 1, 2)		55		ns
Turn-ON Rise Time	t_R			95		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			295		ns
Turn-OFF Fall Time	t_F			125		ns
Total Gate Charge	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=1.3\text{A}$, $I_G=100\mu\text{A}$ (Note 1, 2)		41		nC
Gate-Source Charge	Q_{GS}			6		nC
Gate-Drain Charge	Q_{GD}			12		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				11	A
Maximum Body-Diode Pulsed Current	I_{SM}				44	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=15\text{A}$, $V_{GS}=0\text{V}$			1.4	V

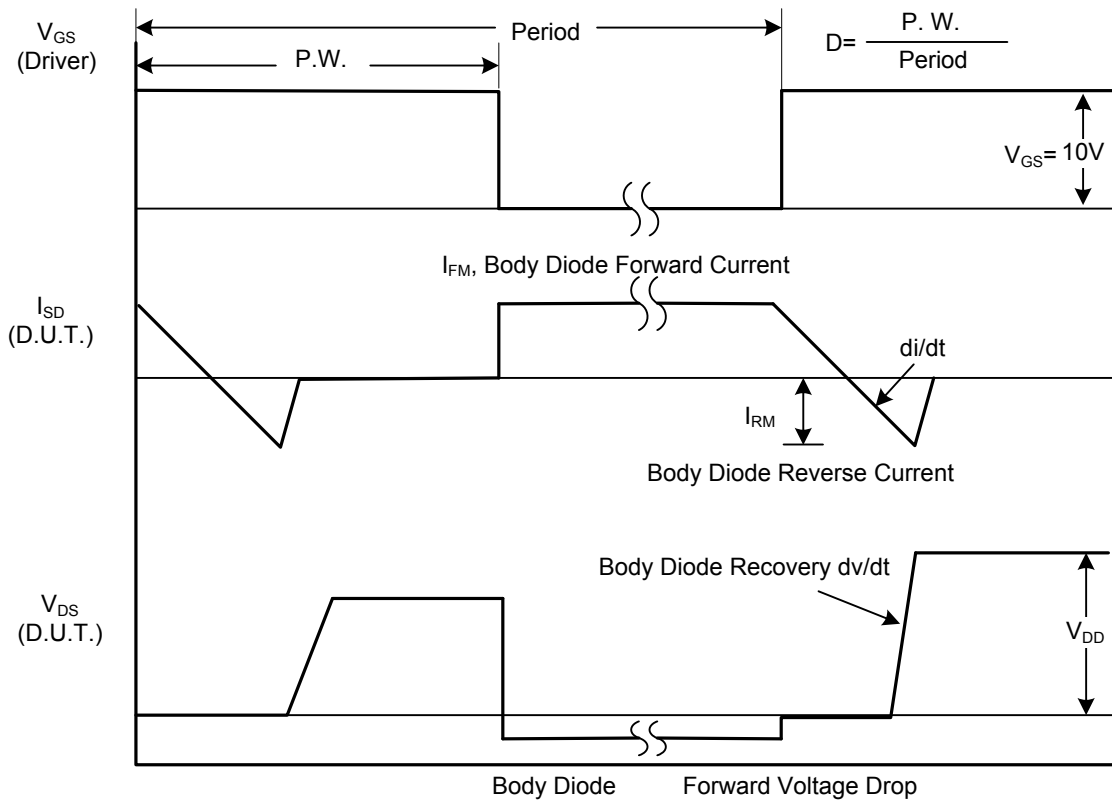
Note: 1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

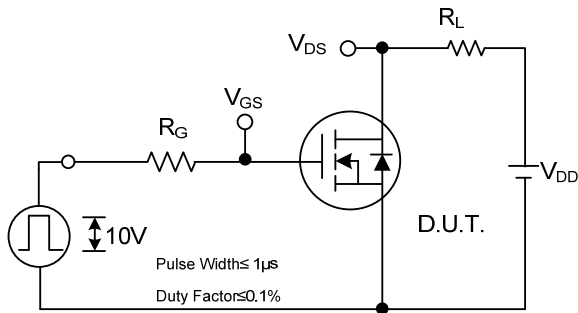


Peak Diode Recovery dv/dt Test Circuit

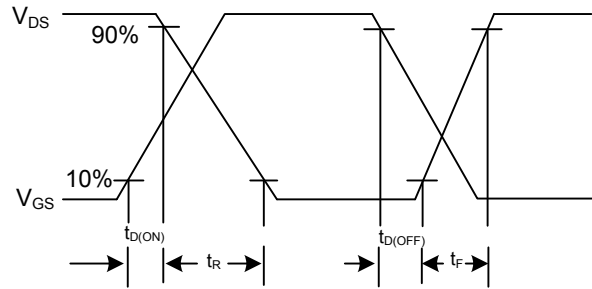


Peak Diode Recovery dv/dt Waveforms

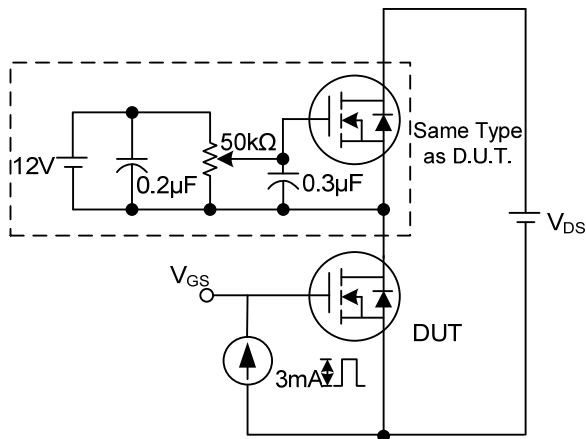
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



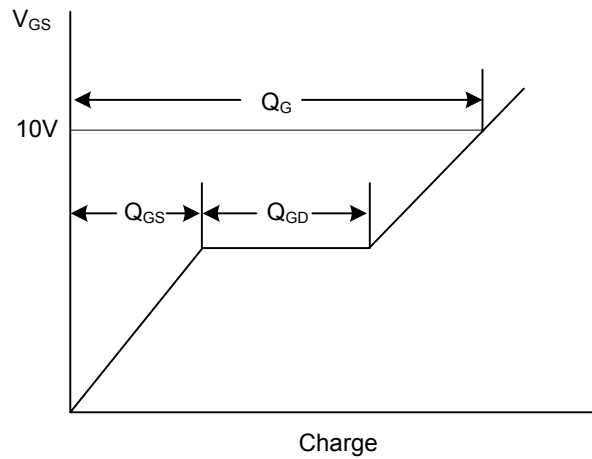
Switching Test Circuit



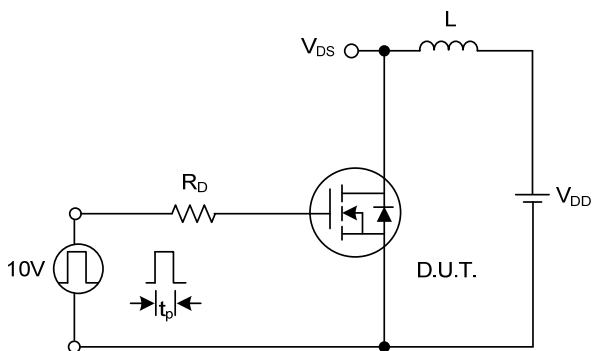
Switching Waveforms



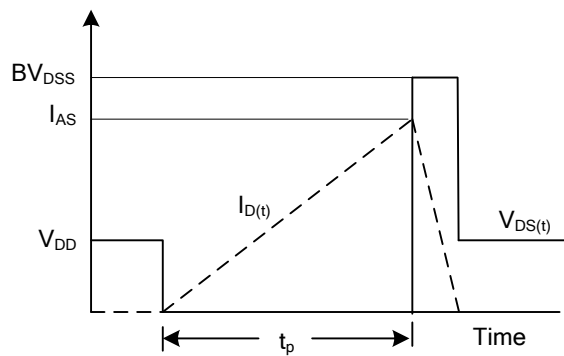
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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