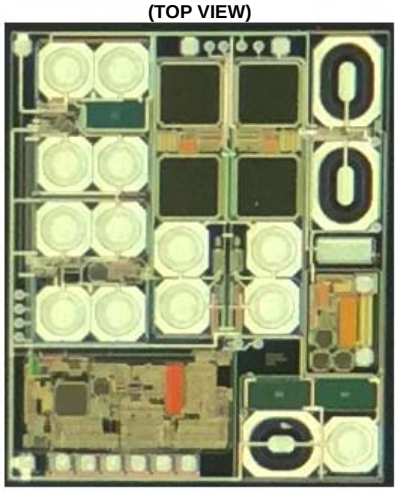
16SCT001D
1200V DIRECT-COUPLED MOSFET / IGBT GATE DRIVER

- Maximum Blocking Voltage. . . 1200 V
- Zero External Components
- Direct Drive From Low-Voltage Control Signals
- MOSFET / IGBT Gate-Emitter Overdrive Circuitry
- Fast IGBT Turn-On & Turn-Off Times
- Low HV Current
- Ultra-Low Idle Current

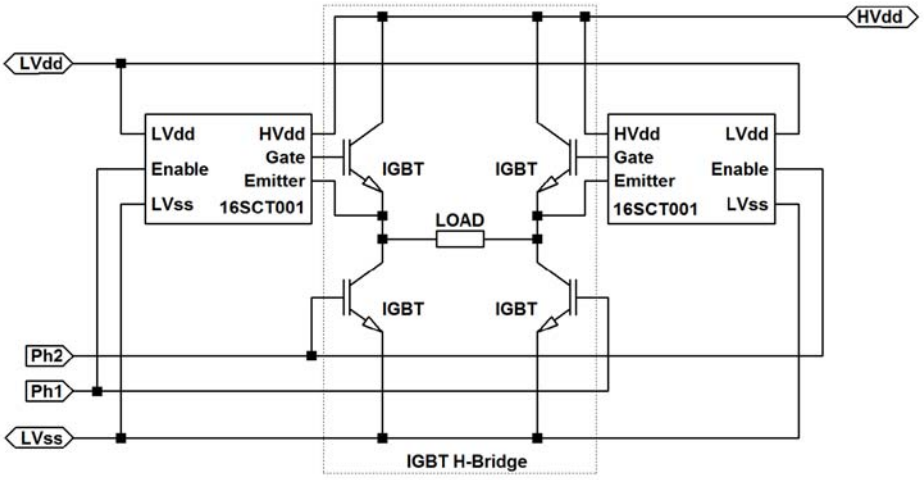
DIE
(TOP VIEW)



Description

The 16SCT001E is a high-voltage (1200V max) direct coupled MOSFET / IGBT gate driver typically used in systems requiring the ability to control the conduction state of a high-voltage (HV) MOSFET / IGBT switch. The chip has built-in circuitry to drive the MOSFET / IGBT gate above the HV supply to ensure that the transistor is adequately saturated.

Typical application



Absolute maximum ratings

High Voltage Power Supply (HV_{dd} - LV_{ss})	1200 V
Low Voltage Power Supply (LV_{dd} - LV_{ss})	18 V
Operating temperature	-40 C to 100 C
Storage temperature	-65 C to 125 C

Maximum operating conditions

PARAMETER	MIN	MAX	UNIT
Operating voltage (HVdd - LVss)	40	1000	V
Operating voltage (LVdd - LVss)	6	18	V

Pin definitions

SYMBOL	DESCRIPTION
HVdd	High Voltage Supply; 40 - 1200V
LVdd	Low Voltage Supply; 6.0 - 18V
LVSS	Low Voltage Supply; 0V
IntClkE	Internal Clock Enable; asserted high (LVdd) enables internal oscillator
ClkSel	Selects Internal or External clock source; asserted high (LVdd) selects internal clock
Clk	External clock source; 0 - LVdd, 500kHz - 1.2MHz
ClkBar	External clock source (complement to Clk, non-overlapping); ; LVdd - 0, 600kHz - 1.2MHz
Gate	Gate terminal of the high-side IGBT, drives above HV_{dd} to ensure IGBT saturation
Emitter	Emitter terminal of the high-side IGBT

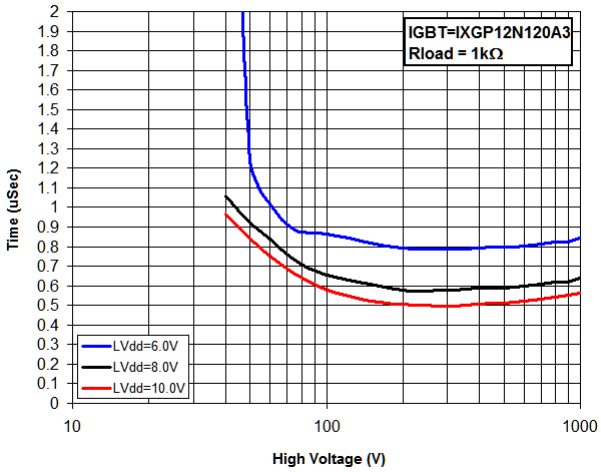
Static electrical characteristics ($25^oC \pm 5^oC$ unless specified)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{HVdd}	HV_{dd} off state current	HV_{dd} = 750V LVdd = 8.0V			85	µA
I_{LVdd}	LV_{dd} off state current	LV_{dd} = 8V	-10		10	nA
R_{CLKin}	Clk, ClkBar input resistance to LVss	V_{in} = 8V	4.5	10	16	kOhm

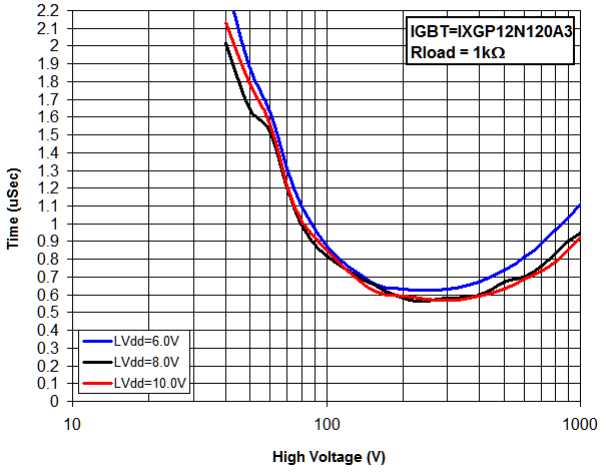
Dynamic electrical characteristics (IGBT: IXGP12N120A3, R_{load}: 1kΩ, 25°C ± 5°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ge}	IGBT Gate - Emitter Voltage	LV_{dd} = 8V, HVdd=100V	14.5	15.5	16.5	V
t_{rdVge}	V_{ge} Rise Time Delay to Vge=2.0V	LV_{dd} = 8V, HVdd=100V	0.55	0.86	1.25	µS
t_{rVge}	V_{ge} Rise Time (to 90% Vge)	LV_{dd} = 8V, HVdd=100V	15.0	24.0	35.0	µS
t_{fdVge}	V_{ge} Fall Time Delay (to 90% Vge)	LV_{dd} = 8V, HVdd=100V	0.70	1.44	2.00	µS
t_{fVge}	V_{ge} Fall Time (to 10% Vge)	LV_{dd} = 8V, HVdd=100V	0.01	0.20	0.50	µS
$t_{rdILoad}$	Load Current Rise Time Delay to 10%	HV_{dd} = 500V, LV_{dd} = 8V	0.25	0.60	1.00	µS
t_{rILoad}	Load Current Rise Time 10%-90%	HV_{dd} = 500V, LV_{dd} = 8V	0.20	0.50	1.00	µS
$t_{fdILoad}$	Load Current Fall Time Delay to 90%	HV_{dd} = 500V, LV_{dd} = 8V	1.00	1.55	2.20	µS
t_{fILoad}	Load Current Fall Time 90%-10%	HV_{dd} = 500V, LV_{dd} = 8V	0.10	0.25	0.50	µS
I_{HVdd}	HV_{dd} pulse-on current (t>100uSec)	LV_{dd} = 8V			6.0	mA
I_{LVdd}	LV_{dd} pulse-on current (t>100uSec)	LV_{dd} = 8V			1.0	mA
tsc	Turn-off time	LV_{dd} = 8V, HV_{dd} = 100V R_{load} = 3.9Ω			2.2	µS
tc	Internal Clock Period	LV_{dd} = 8V, HV_{dd} = 0V IntClkE = ClkSel = LV_{dd}	1.10	1.45	2.0	µS
tc	Internal Clock Duty Cycle	LV_{dd} = 8V, HV_{dd} = 0V IntClkE = ClkSel = LV_{dd}	45.0	50.0	55.0	%

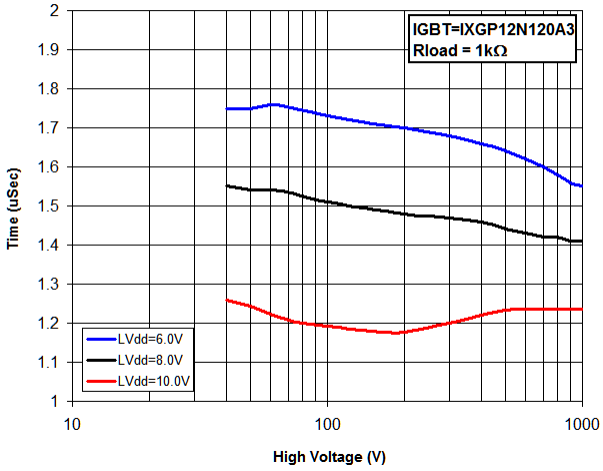
Load Current Rise Time Delay to 10%



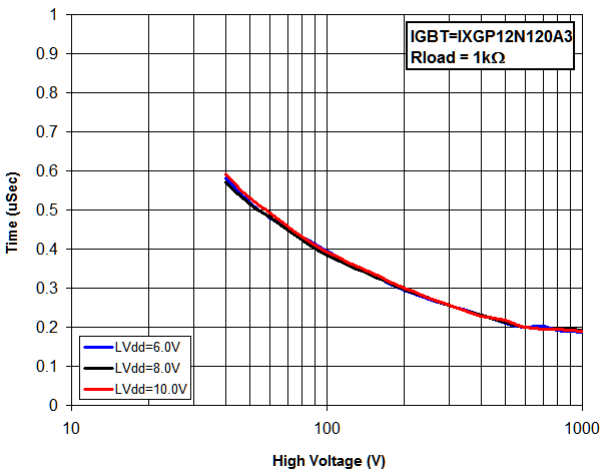
Load Current 10%-90% Rise Time



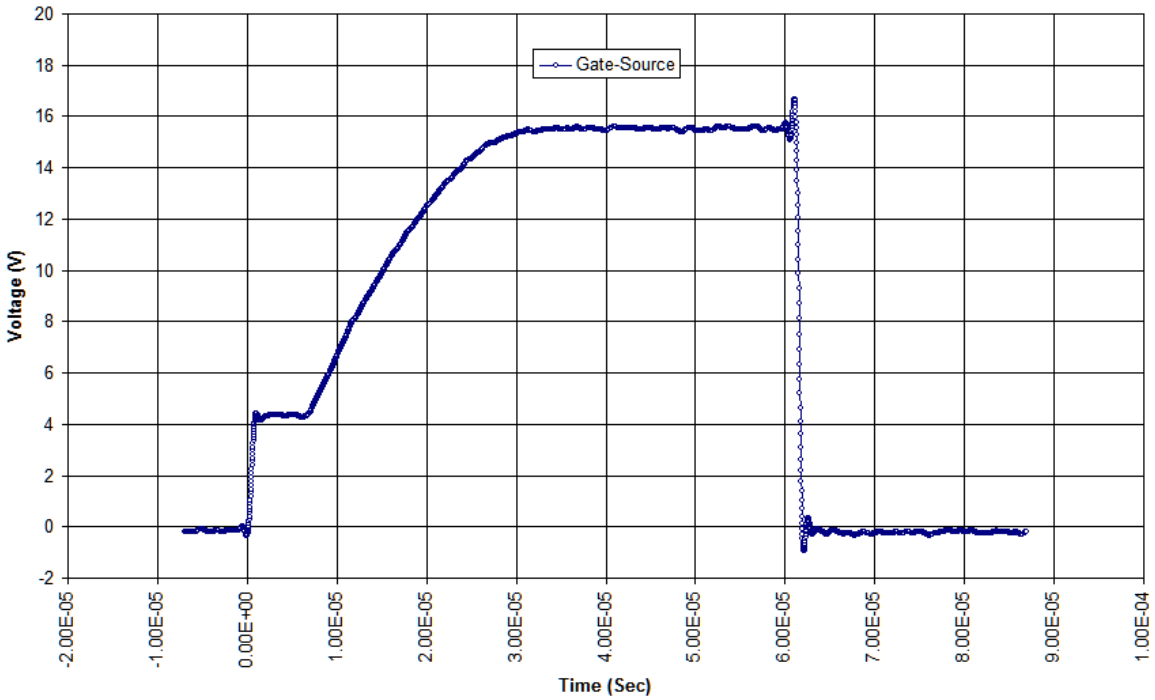
Load Current Fall Time Delay to 90%



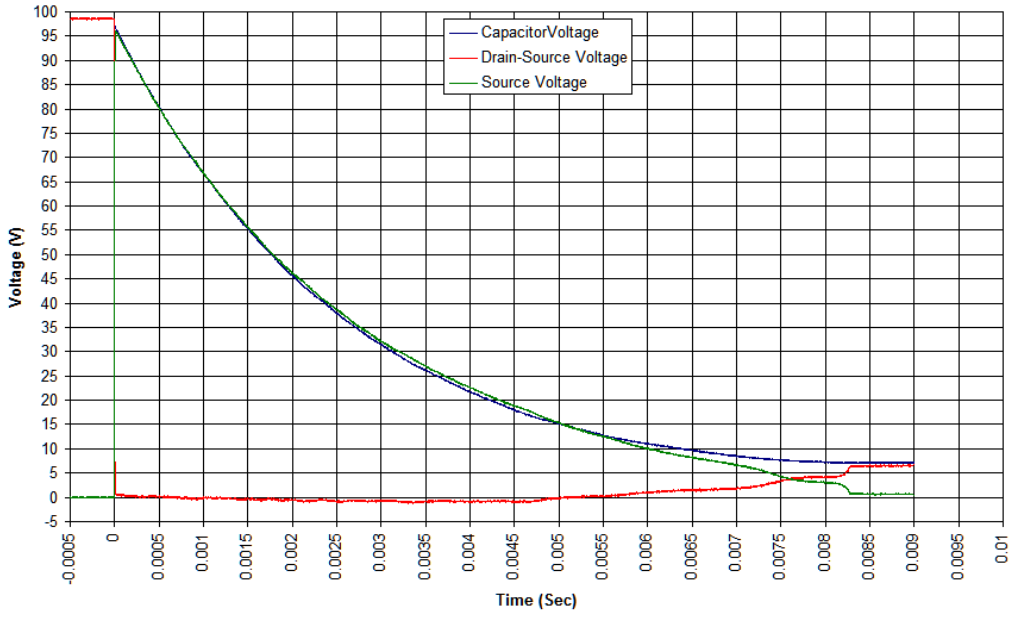
Load Current 90%-10% Fall Time

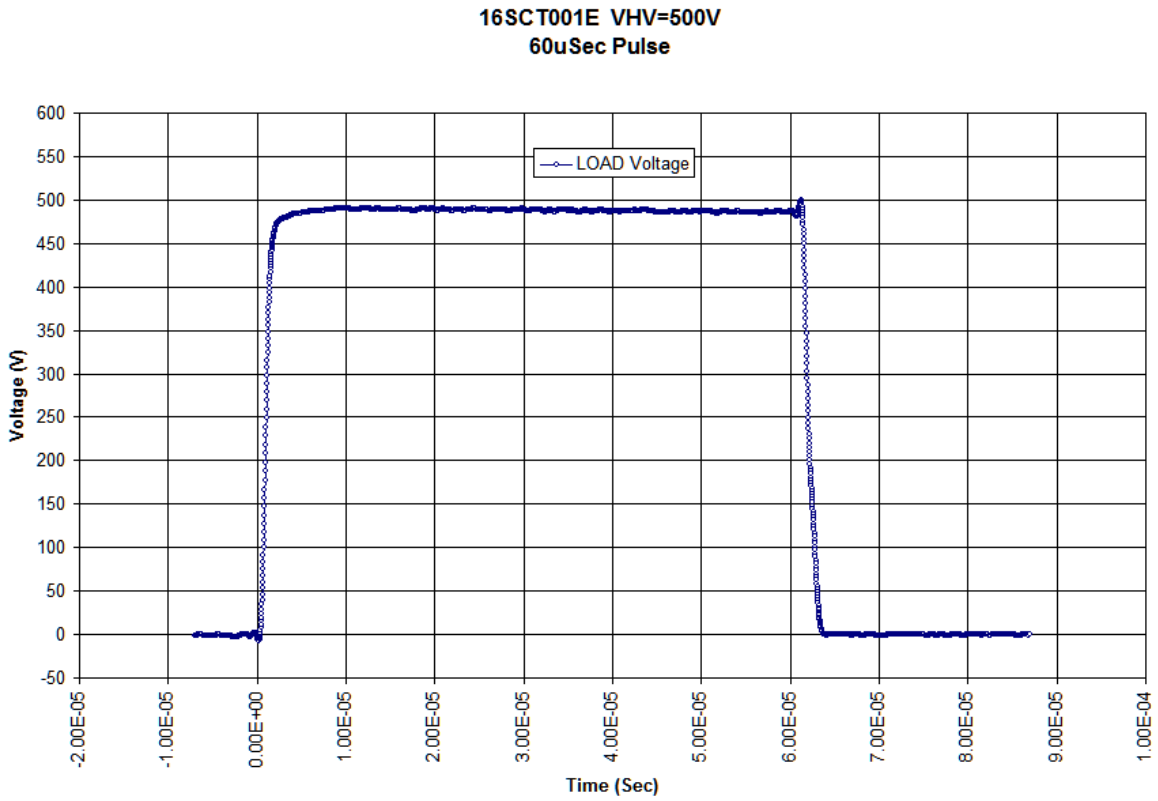


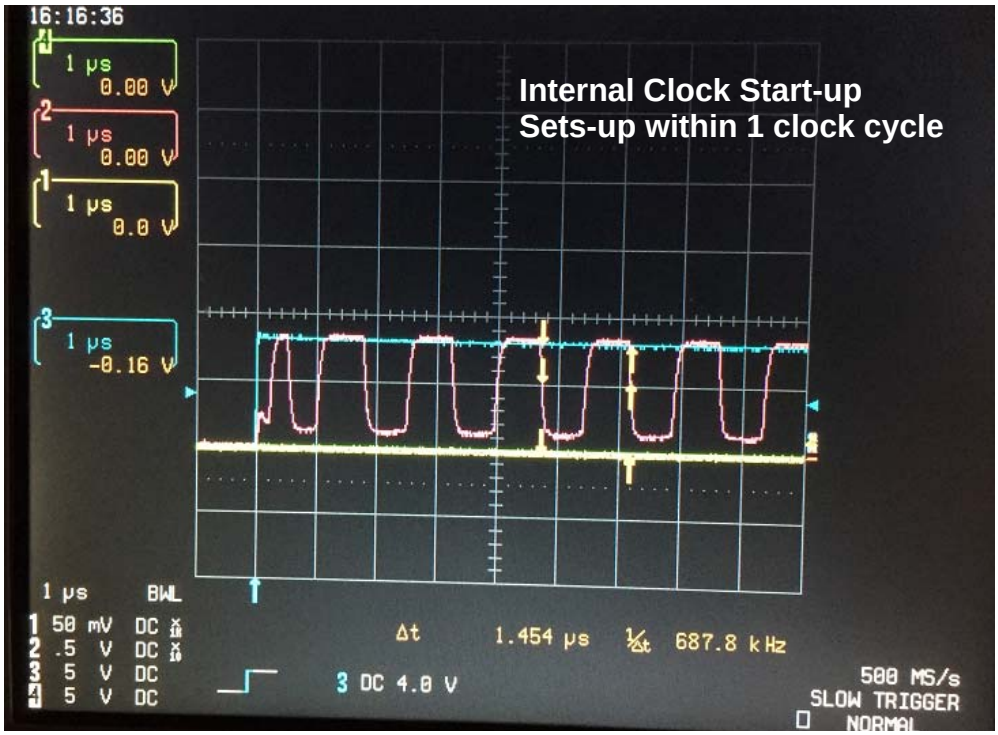
16SCT001E VHV=100V
60uSec Pulse, LOAD=1kOhm



16SCT001E VHV=100V [Complete Capacitor Discharge]
20mSec Pulse, LOAD=512 Ohm Cap=5uF RC=2.6mSec







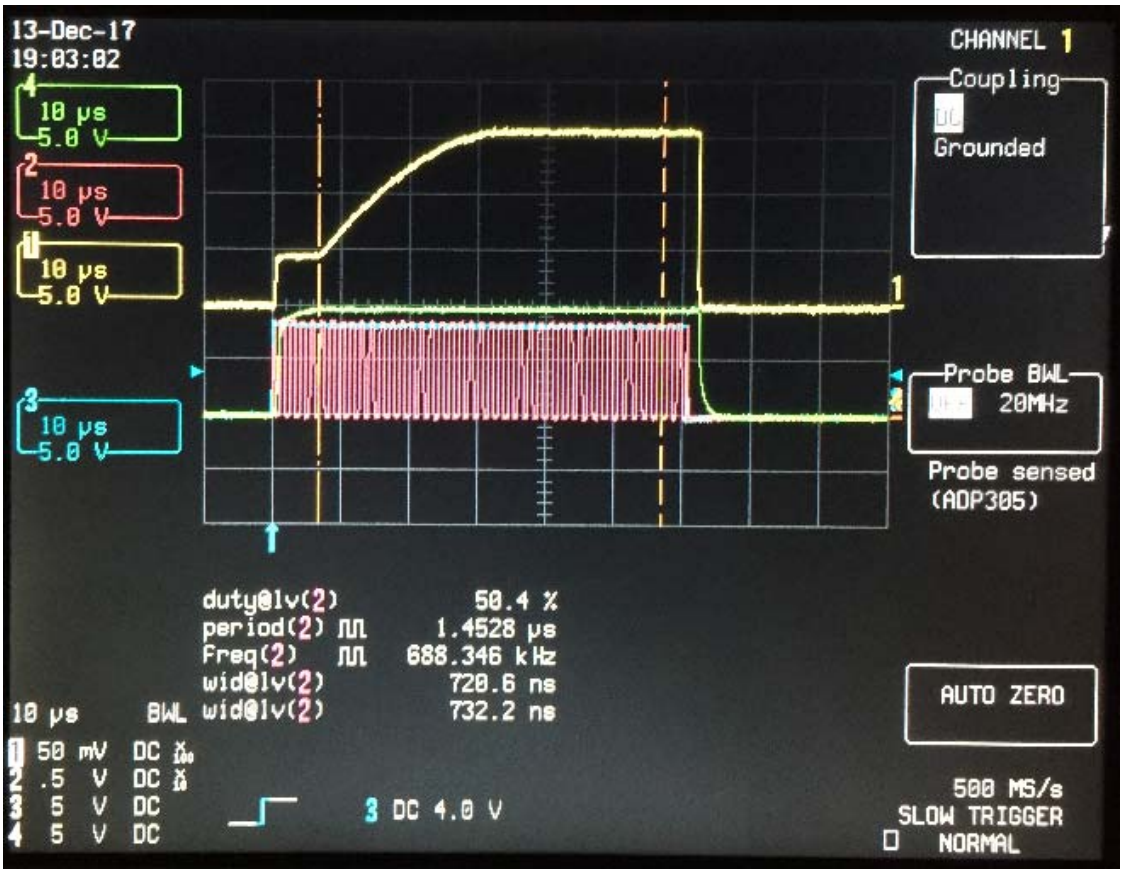


Fig 5: HV=100V, Rload=1kOhm, IGBT=IXGP12N120A3:
Yellow trace (Ch1) is Gate-Emitter voltage
Green Trace (Ch4) is Emitter Voltage/10
Blue Trace (Ch3) is Internal Clock Enable
Red Trace (Ch2) is Internal Clock

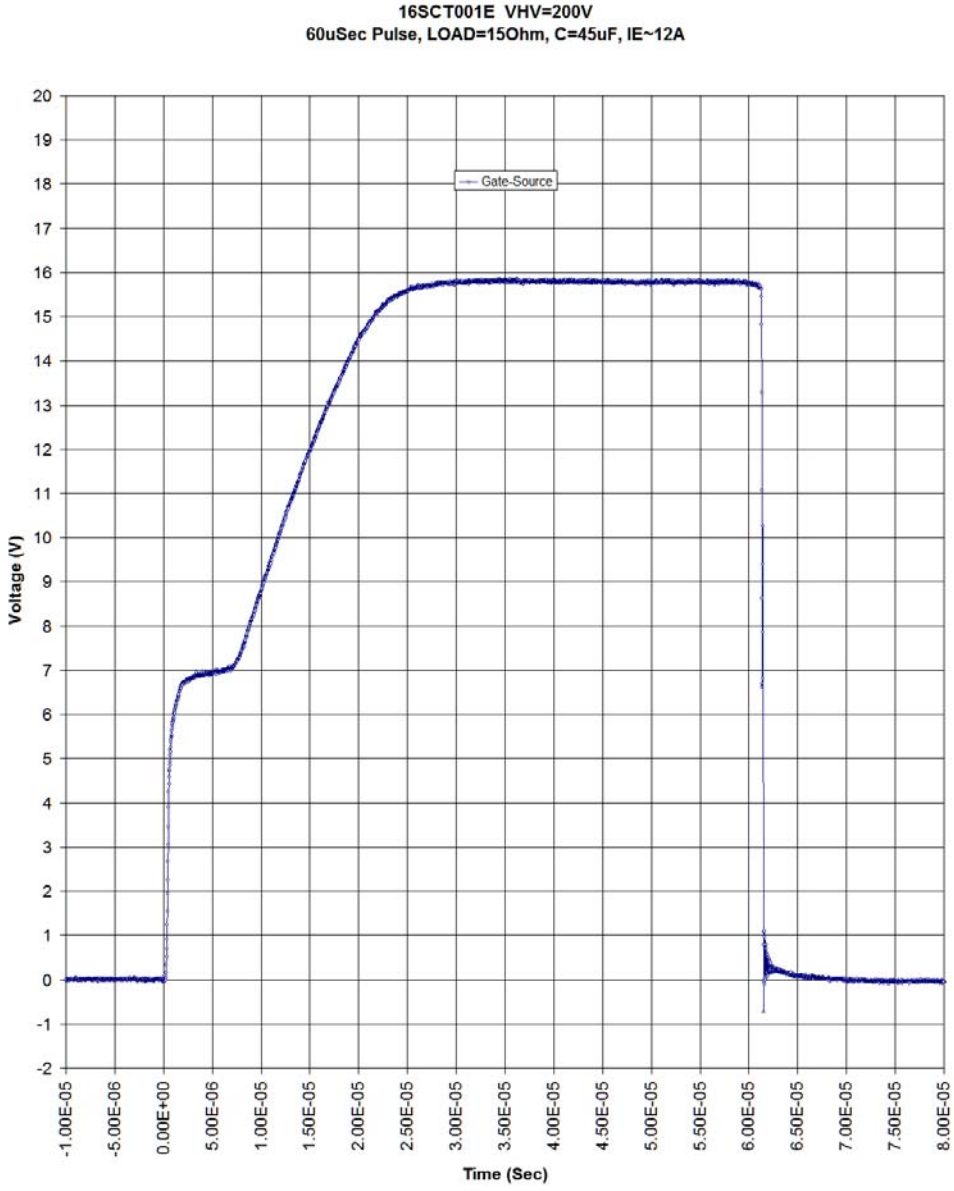


Fig 6: HV=200V, Rload=15.0 Ohm, IGBT=IXGP12N120A3:
Gate Emitter voltage showing faster rise to maximum Vge when a low resistance load is used. In this case 90% of Vge (14.2V/15.8V) is reached in ~19.6uSec. This condition corresponds to a IGBT current of about 12A.

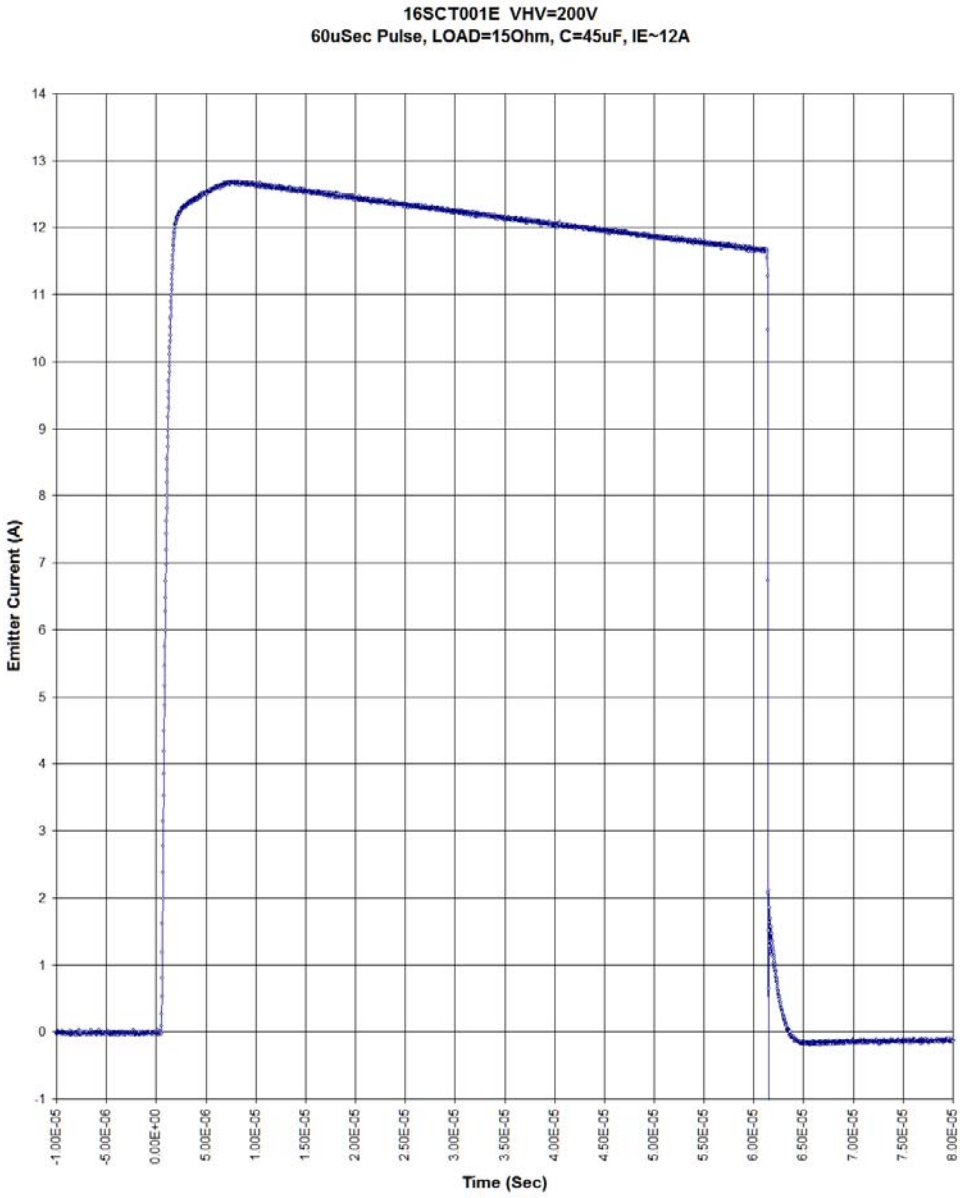
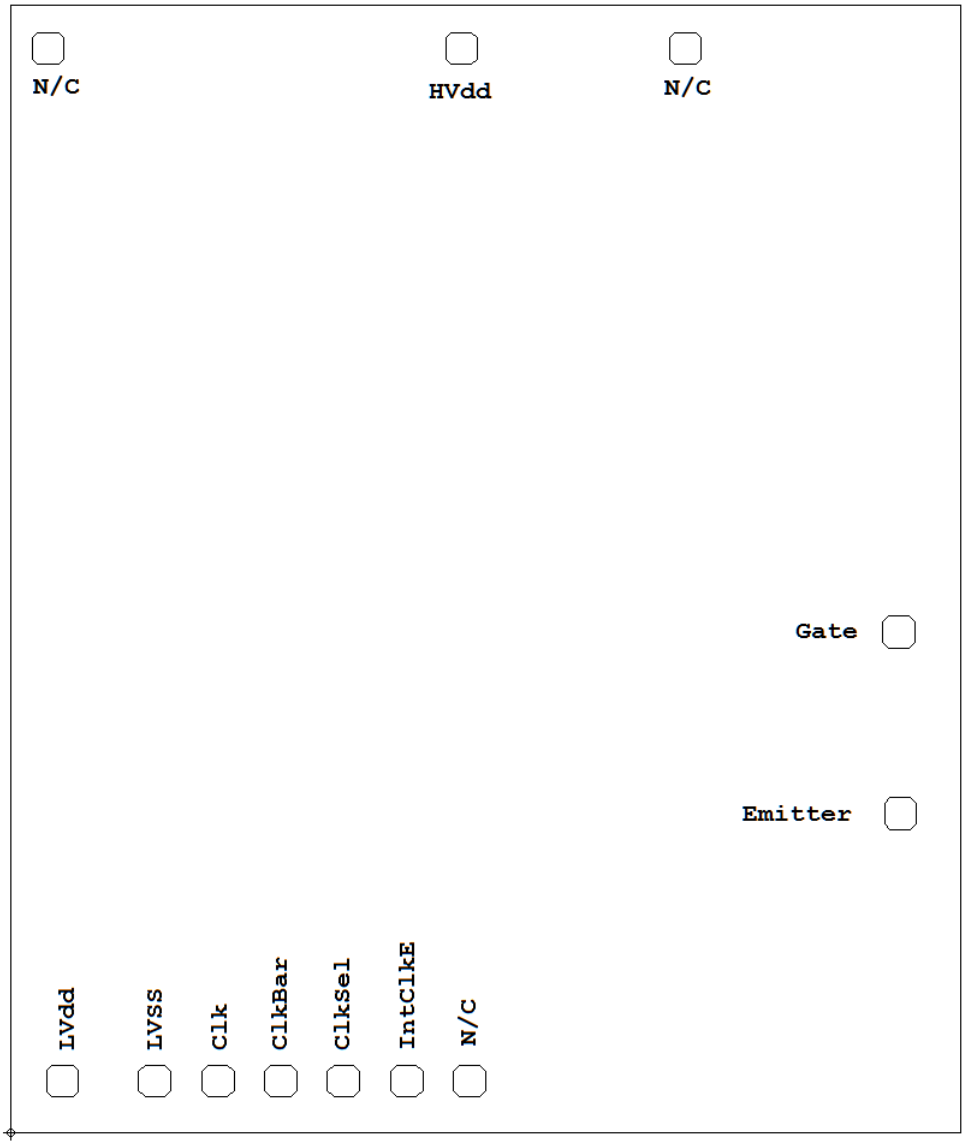


Fig 7: HV=200V, Rload=15.0 Ohm, IGBT=IXGP12N120A3:
Emitter current showing faster rise to maximum Ie when a low resistance load is used. In this case 100% of Ie (12.6A) is reached in ~7.7uSec. This condition corresponds to a peak IGBT current of about 12.6A.

Die Dimensions

PARAMETER		MIN	TYP	MAX	UNIT
Y_{SIZE}	Long Side Dimensions	3160	3260	3360	µm
X_{SIZE}	Short Side Dimensions	2650	2750	2850	µm
Z_{SIZE}	Die Thickness	260	285	310	µm



Visual inspection

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
100% Visual Inspection per MIL STD 883H Method 2010 Condition B.	ALL	100%	n/a	n/a

Product qualification tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 504hrs @ V_{HV}=1000V; MIL STD 883 method 1015	3	22	0	n/a
Physical dimensions	3	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	3	20	1	n/a

Lot acceptance tests

PARAMETER	Lot Sampled	Sample Size	Fails Allowed	UNIT
Static burn-in 168hrs @ V_{HV}=1000V; MIL STD 883 method 1015	each	22	0	n/a
Physical dimensions	each	11	0	n/a
Wire Bond Evaluation (Gold Ball Bond) per MIL STD 883 method 2011	each	20	1	n/a

Product qualification tests are performed on 3 lots while a Lot Acceptance Test (LAT) is performed on each “diffusion lot”. LAT is considered complete if the lot was used for product qualification.

All samples used for qualification and LAT burn-in test are assembled in a open cavity ceramic DIL package with a dielectric silicone gel filling the cavity. Tthe chip is mounted to provide isolation between the wirebonds and the substrate and to eliminate surface conduction and polarization as possible means of unwanted failure.

Application notes

To make best use of the 16SCT001, the chip should be molded before high voltage is applied to it. This can either be done with a standard mold compound or with silicone gel. Care should be taken when selecting a encapsulant to ensure proper dielectric strength and resistance. We recommend that the dielectric strength of the dielectric used be greater than 10kV/mm at a thickness of 50um.

Care should also be taken to properly isolate the chips substrate which is biased at about half V_{HV}. In no circumstance should the chip be mounted over layers providing less than 1kV of dielectric isolation. It is also strongly recommended to use non-conducting epoxy for attaching the chip.

Ball bonding should be used for attaching conductors to the chip's pad. Wedge bonding is not recommended because of the shorter distance between the wirebond and the chip's edge, increasing the risk of arcing. When using ball bonding the wire should extend vertically for at least 100um before going horizontal toward the substrate or package pad.