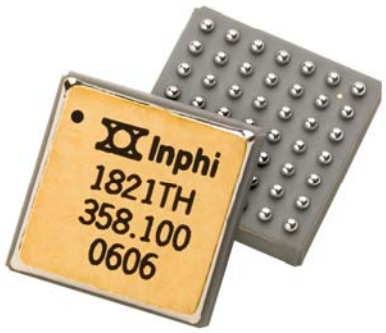
1821TH
18 GHz Bandwidth 2 GS/s THA
Datasheet



Applications

- Test instrumentation equipment, ATE
- RF demodulation systems
- Radar
- Software radio
- Digital receiver systems
- High-speed DAC deglitching
- THA for differential ADCs
- Digital sampling oscilloscopes

Features

- Supports 2 GS/s sampling rate
- 18 GHz input bandwidth (small-signal)
- 15 GHz input bandwidth (0.5 Vpp)
- 12 GHz input bandwidth (1 Vpp)
- THD < -60 dB (1 GHz 1 Vpp input)
- THD < -35 dB (10 GHz 0.5 Vpp input)
- Fast rise time: < 25 ps (10 – 90%)
- Ultra low aperture jitter: < 50 fs
- 0 dB Gain with up to 1 Vpp out
- Differential master-slave architecture
- Multiple clock modes
- Adjustable input termination voltage
- Single -5.2 V power supply
- Low power consumption: 1300 mW
- Small die size: 1.58 mm x 1.28 mm
- Available in a BGA package and in die form
- Evaluation kit available

Description

The 1821TH track-and-hold amplifier is designed for high-precision sampling of wideband signals with multi-GHz frequency content. The master-slave architecture integrates two track-and-hold circuits, a 50-ohm differential output buffer, and clock mode selection logic.

Sample rates up to 2 GS/s are supported. Clock modes include out-of-phase master-slave (M/S) clocking based on a single clock signal and independent M/S clocking based on two clock signals. The output is settled for nearly a complete clock cycle of the slave T/H.

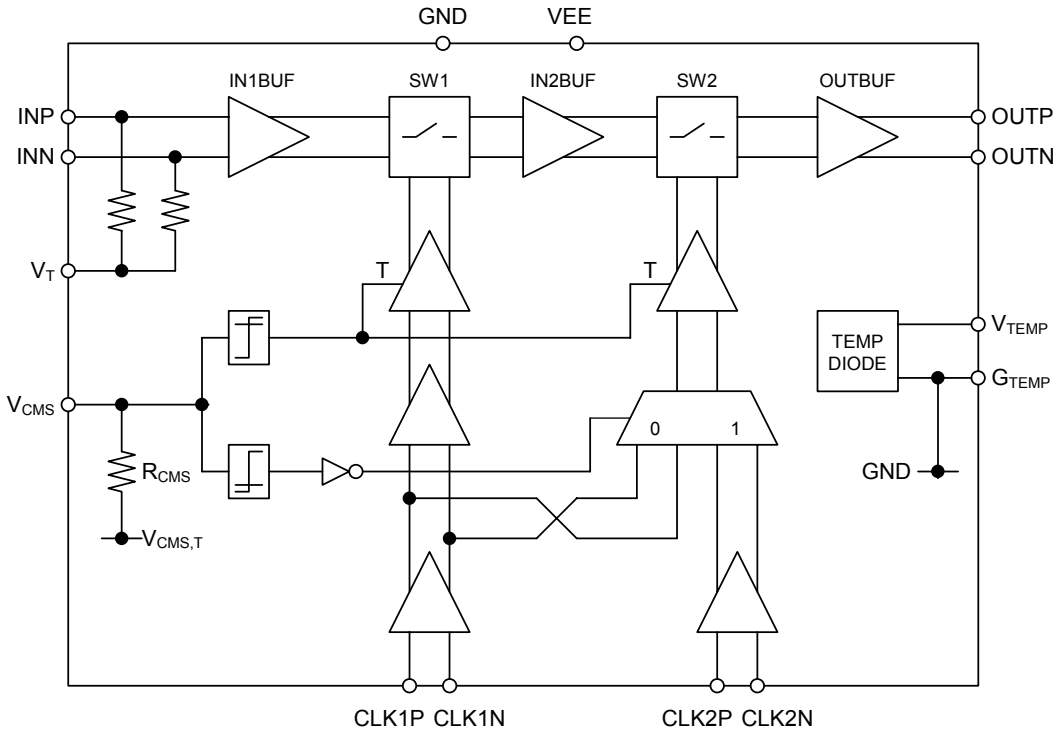
Analog inputs are direct coupled and terminated on-chip with 50 ohms to a user-adjustable voltage.

The 1821TH can be driven single-ended or differentially and provides differential outputs. An output buffer provides 0 dB overall THA gain and up to 1 Vpp differential output swing into a 50-ohm load. Clock inputs are direct coupled and are terminated with 50 ohms to ground.

Because of it's low power dissipation and low thermal resistance, the 1821TH does not normally require a heat sink when operated at a case temperature up to the maximum case temperature of 85 °C.

The 1821TH operates from a single -5.2 V power supply. It is available in a 6 mm square, hermetic, BGA package and in die form. It is also available on an evaluation board with SMA connectors

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply Voltage	V_{EE}		-6	0.5	V
RF Input Signals[1]		Terminated to V_T on-Chip	max(-2, -2.5+V_T)	min(1, 2.5+V_T)	V
RF Output Signals			-2	1	V
Input Termination Voltage[2]	V_T		max(-4 – 2$V_{IN,MIN}$, -5 +2$V_{IN,MAX}$)	min(2 –2$V_{IN,MAX}$, 5 +2$V_{IN,MIN}$)	V
Clock Mode Select Voltage	V_{CMS}		V_{EE} - 0.3	0.3	V
Temperature Diode Voltage	V_{TEMP}		TBD	TBD	V
Junction Temperature - Die	T_J		-47	+175	°C
Case Temperature - Package	T_C		-65	+125	°C
Shipping/Storage Temperature	T_{STORE}		-65	+125	°C
Humidity	R_H		0	100	%
ESD Protection (HBM)		All, Except Analog Inputs	500	---	V
		Analog Inputs	100	---	V

Notes:

[1] RF input signals, INp and INn, are terminated on-chip with 50 Ω to V_T. The stated min and max values insure that INp and INn lie between -2 & +1 V and limit the pin currents to 50 mA.

[2] The V_T min and max values depend on RF input signal levels and are assumed to be driven by 50 Ω sources. $V_{IN,MIN}$ ($V_{IN,MAX}$) is the minimum (maximum) expected INp or INn voltage, assuming a 50 Ω to GND termination. The stated V_T voltage min and max values insure that INp and INn lie between -2 & +1 V and limit the pin currents to 50 mA.

Test Levels

Test Level (TL)	Test Procedure
1	100% Production tested at V_{EE} = -5.2 V, T_C = 25 C. Characterization sample tested over V_{EE}, T_C operating conditions
2	Characterization sample tested over V_{EE}, T_C operating conditions
3	Guaranteed by design and/or characterization testing
4	Typical value only.

Operating Conditions

Parameter	Symbol	Conditions	TL	Min	Typ	Max	Unit
Power Supply Voltage	V_{EE}	± 5% Tolerance	---	-5.45	-5.2	-4.95	V
Supply Current	I_{EE}		1	---	250	---	mA
On-Chip Power Dissipation	P_D		1	---	1.3	---	W
Operating Temperature (Junction) - Die	T_J		---	-22	---	+125	°C
Operating Temperature (Case) – Packaged[1]	T_C		---	-40	---	+85	°C
Thermal Resistance	R_{JC} (θ_{JC})		---	---	13.8	---	°C/W

Notes:
[1] The set of data at –40C BGA package operating temperature has been verified on a limited number of parts from one wafer only. Therefore, this data set should be regarded as typical values.

Electrical Specifications: RF I/O

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Full Scale Range	FSR	Single-Ended	4	---	500	---	mVpp
		Differential	4	---	1000	---	mVpp
Input High Level[1]	V_{IH}		2	0.5	---	---	V
Input Low Level[1]	V_{IL}		2	---	---	-0.5	V
Input Resistance		Each Lead to V_T	1	45	50	55	Ω
Input Return Loss	RL_{IN}	Up to 15 GHz	2	10	---	---	dB
Clock Amplitude		Single-Ended	2	300	---	600	mVpp
		Differential	2	300	---	1200	mVpp
Clock Input High Level	V_{CH}		2	0.5	---	---	V
Clock Input Low Level	V_{CL}		2	---	---	-1	V
Clock Input Resistance		Each Lead to GND	1	54	60	66	Ω
Clock Input Return Loss	RL_{CLK}	Up to 5 GHz	2	15	---	---	dB
Output Termination Voltage	$V_{OUT,T}$		2	0	0	1	V
Output Common Mode Voltage[2]	$V_{OUT,CM}$	Into 50 Ω to $V_{OUT,T}$	3	---	-0.55 + 0.58$V_{OUT,T}$	---	V
Output Return Loss	RL_{OUT}	Up to 5 GHz	2	15	---	---	dB
Gain (50-Ω I/O Environment)	A_V	-5 to +85 °C Temp. range	1	0.95	1	1.05	
		-40 to +85°C Temp range	1	0.85	1	1.05	
Gain Drift	$\partial A_V/\partial T$	-5 to +85 °C Temp. range	2	---	-100	---	ppm/°C
		-40 to -5°C Temp range	2	---	430	---	
Offset	V_O	Differential, Input Referred	2	---	---	±10	mV
Offset Drift	$\partial V_O/\partial T$	Differential, Input Referred	2	-50	10	+60	uV/°C

Notes:

[1] Input voltages are defined as input pad (or ball) voltages with respect to GND. For inputs that are not closely GND-centered, set V_T so that input voltages are within the V_{IL} to V_{IH} range. The V_T input must be connected to GND or a DC supply that is bypassed well to GND. For GND-centered inputs, connect V_T to GND.

[2] Outputs are resistively terminated, on chip, to GND. The $V_{OUT,T}$ range allows adjustment of $V_{OUT,CM}$ from -550 mV to about +30 mV. $V_{OUT,T}$ is the termination voltage at the destination end of the receiving device

Electrical Specifications: DC I/O

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Clock Mode Select Voltage[1]	V_{CMS}	**Full Track Mode**: TH1 and TH2 in Track Mode; CLK1 and CLK2 Ignored	3	-0.5	---	0	V
		CLK1 Mode: CLK1 clocks TH1 and TH2, out-of-phase; CLK2 Ignored	3	V_{EE} + 2	---	-2	V
		CLK1&2 Mode: CLK1 clocks TH1, CLK2 clocks TH2	3	V_{EE}	---	V_{EE} + 0.5	V
Clock Select Termination Voltage[2]	$V_{CMS,T}$		3	---	$0.5V_{EE}$	---	V
Clock Select Input Resistance	R_{CMS}	To $V_{CMS,T}$. V_{EE}-0.5 < V_{CMS} < 0.5 V	3	---	3	---	kΩ

Notes:

[1] V_{CMS} selects one of three clock modes. Full track mode is useful for test purposes. CLK1 mode is the easiest to use since only one clock signal is required. CLK1&2 mode allows sub-sampling by N of the TH1 output by choosing $f_{CLK2} = f_{CLK1} / N$. A high CLK1 frequency may be optimal for lowest clock jitter while a low CLK2 frequency may allow reduced speed requirements on subsequent circuitry, such as an ADC.

[2] Internally generated voltage. For V_{EE} = -5.2V, $V_{CMS,T}$ = -2.6V. If the CMS pin is open, V_{CMS} defaults to $V_{CMS,T}$. This results in the CLK1 mode being selected.

Electrical Specifications: Dynamic

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Bandwidth, Small-Signal	bw	-3dB Gain, 0.1 Vpp Input	2	---	18	---	GHz
Bandwidth, Half-Scale Signal		-3dB Gain 0.5 Vpp Input	2	---	15	---	GHz
Bandwidth, Large-Signal	BW	-3dB Gain 1 Vpp Input	2	11	12	---	GHz
Gain Flatness Deviation		Up to 10 GHz	2	---	±0.5	±0.8	dB
Integrated Noise[1]		Over the first Nyquist band	4	---	0.64	---	mV
		Over second Nyquist band	4	---	0.32	---	mV
Noise Power Floor		Input Referred	4	---	22.3	---	nV/√Hz
Master T/H Hold Feedthrough[2]	$A_{TH1,HOLD}$	1 GHz 1 Vpp Input	2	---	-65	---	dB
Total Harmonic Distortion[3,4]	THD	1 GHz 1 Vpp Input	1	---	-60	-55	dB
		2 GHz 1 Vpp Input	2	---	-55	-51	dB
		3 GHz 1 Vpp Input	2	---	-53	-48	dB
		5 GHz 1 Vpp Input	2	---	-40	-35	dB
		10 GHz 1 Vpp Input	2	---	-27	-24	dB
		14 GHz 1 Vpp Input	2	---	-25	---	dB
		1 GHz 0.5 Vpp Input	2	---	-70	-55	dB
		2 GHz 0.5 Vpp Input	1	---	-60	-52	dB
		3 GHz 0.5 Vpp Input	2	---	-60	-52	dB
		5 GHz 0.5 Vpp Input	2	---	-50	-40	dB
		10 GHz 0.5 Vpp Input	2	---	-35	-30	dB
		14 GHz 0.5 Vpp Input	2	---	-32	---	dB
		17 GHz 0.5 Vpp Input	2	---	-33	---	dB
		5 GHz 0.25 Vpp Input	2	---	-55	-50	dB
		10 GHz 0.25 Vpp Input	1	---	-45	-40	dB
		14 GHz 0.25 Vpp Input	2	---	-39	---	dB
		17 GHz 0.25 Vpp Input	2	---	-40	---	dB
		5 GHz 0.1 Vpp Input	2	---	-55	-50	dB
		10 GHz 0.1 Vpp Input	1	---	-50	-45	dB
		14 GHz 0.1 Vpp Input	2	---	-45	---	dB
		17 GHz 0.1 Vpp Input	2	---	-44	---	dB

Notes:

[1] Input Referred, 1 GHz clock. Integrated Noise and Noise Power Floor depend on sample rate. Noise Power Floor decreases 3dB when the sample rate doubles.

[2] In dB: $A_{TH1,HOLD}$ = -(TH1 isolation). Since the TH1 track mode gain is close to unity, $A_{TH1,HOLD}$ can be measured and is the ratio of the TH gain with TH1 in hold mode to the TH gain with TH1 in track mode (TH2 is kept in track mode).

[3] THD is measured using a differential output with a differential input. Both outputs are terminated with 50 Ω to $V_{OUT,T}$.

[4] THD data measured at 14 & 17 GHz were taken on three devices at 25C, -15C, & -40C BGA package temperatures.

Electrical Specifications: TH1 Switching

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Aperture Delay[1]	t_A	After V_{CLK1P}-V_{CLK1N} Goes Positive	4	---	55	---	ps
Aperture Delay Drift	$\partial t_A/\partial T$		2	---	+25	---	fs/°C
Aperture Jitter	Δt	Jitter Free 2 GHz 0.5 Vpp CLK1 Signal	3	---	50	---	fs
Settling Time[1,2]	t_S	After V_{CLK1P}-V_{CLK1N} Goes Positive. To 1 mV at Hold Capacitors, $t_{TRACK1,MIN}$, Observed	4	---	50	---	ps
Differential Pedestal/ V_{IN}			4	---	±0.25	---	%
Differential Droop Rate/ V_{IN}[3]		Hold Mode	2	---	-0.2	---	%/ns
Differential Drift Rate[3]		Hold Mode	2	---	±0. 5	---	mV/ns
Hold Noise/ √(Hold Time)			4	---	TBD	---	mV/√ns
Maximum Hold Time[4,5]	$t_{HOLD1,MAX}$		3	25	---	---	ns
Minimum CLK1 Frequency[4]	$f_{CLK1,MAX}$	50% Duty Cycle Clock	2	---	---	20	MHz
Maximum CLK1 Frequency[6]	$f_{CLK1,MAX}$	50% Duty Cycle Clock	2	2000	---	---	MHz
Acquisition Time[1]	t_{ACQ}	After V_{CLK1P}-V_{CLK1N} Goes Negative. To 1 mV at Hold Capacitors, FSR Input Step	4	---	100	---	ps
Maximum Acquisition Slew Rate	$(\partial V/\partial t)_{MAX}$	At Hold Capacitors, FSR Input Step	4	---	25	---	V/ns
Rise Time[7]	t_R	10 – 90%, 0 to FSR/2 Input Step	3	---	15	25	ps
Minimum Track Time	$t_{TRACK1,MIN}$		4	---	200	---	ps

Notes:

[1] The V_{CLK1P}-V_{CLK1N} positive edge is the TH1 hold command. It causes a transition from the track mode to the hold mode. The V_{CLK1P}-V_{CLK1N} negative edge is the TH1 track command. It causes a transition from the hold mode to the track mode.

[2] For a 0.5Vpp input step with a 25ps (10-90%) rise time. Measured from the time at which the mid-level slope line of the hold capacitor voltage crosses the final value to the time at which the hold capacitor voltage is within 1mV of its final value.

[3] The time variation of the differential output voltage, V_{OUT}, with TH1 in hold mode and TH2 in track mode, is:

dV_{OUT}/dt = TH1 Drift Rate + V_{OUT} x TH1 Droop Rate.

[4] The slew rate of the track-to-hold clock transition should be 1 V/ns or higher for best performance.

[5] The hold time is limited by differential droop, causing exponential decay of the differential signal. No recovery time is required after any hold duration. The maximum hold time is defined here as the time at which the differential signal loss is 5% of its initial held value.

[6] This device was characterized with a clock frequency of up to 2 GHz. However, a limited number of parts passed tests with a 3 GHz clock (room temperature only).

[7] Measured as $\sqrt{(t_{rise,cap}^2 - t_{rise,input}^2)}$, where $t_{rise,input}$ is the 10-90% rise time of the input signal and $t_{rise,cap}$ is the 10-90% rise time of the hold capacitor signal. The rise time $t_{rise,cap}$ is equal to that of the time-reconstructed output signal of a sampled repetitive step signal with rise time $t_{rise,input}$.

Electrical Specifications: TH2 Switching

WARNING – To prevent damage to the part:
- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions							
Parameter	**Symbol**	**Conditions**	**TL**	**Min**	**Typ**	**Max**	**Unit**
Aperture Delay	t_{A2}	After V_{CLK2P}-V_{CLK2N} Goes Positive in CLK1&2 Mode. After V_{CLK1P}-V_{CLK1N} Goes Negative in CLK1 Mode	4	---	45	---	ps
Aperture Delay Drift	$\partial t_{A2}/\partial T$		4	---	+25	---	fs/°C
Settling Time[1]	t_{S2}	After V_{CLK2P}-V_{CLK2N} Goes Positive in CLK1&2 Mode. After V_{CLK1P}-V_{CLK1N} Goes Negative in CLK1 Mode. To 1 mV at Hold Capacitors, $t_{TRACK2,MIN}$, Observed	4	---	60	---	ps
Differential Pedestal / V_{IN}			4	---	±0.25	---	%
Differential Droop Rate / V_{IN}[2]			2	---	-0.1	---	%/ns
Differential Drift Rate[2]		Hold Mode	2	---	±0. 5	---	mV/ns
Hold Noise / √(Hold Time)			4	---	TBD	---	mV/√ns
Maximum Hold Time[3]	$t_{HOLD2,MAX}$		3	50	---	---	ns
Minimum CLK2 Frequency	$f_{CLK2,MAX}$	50% Duty Cycle Clock	2	---	---	10	MHz
Maximum CLK2 Frequency	$f_{CLK2,MAX}$	50% Duty Cycle Clock	2	2000	---	---	MHz
Minimum Track Time	$t_{TRACK2,MIN}$	After TH1 in Hold Mode	4	---	200	---	ps

Notes:

[1] For a 0.5Vpp step between subsequent TH1 output levels. Measured from the time at which the mid-level slope line of hold capacitor voltage crosses the final value to the time at which the hold capacitor voltage is within 1mV of its final value.

[2] The time variation of the differential output voltage, V_{OUT}, with TH1 in any mode and TH2 in hold mode, is:

dV_{OUT}/dt = TH2 Drift Rate + V_{OUT} x TH2 Droop Rate.

[3] The hold time is limited by differential droop, causing exponential decay of the differential signal. No recovery time is required after any hold duration. The maximum hold time is defined here as the time at which the differential signal loss is 5% relative to its initial held value.

Typical DC Operating Characteristics

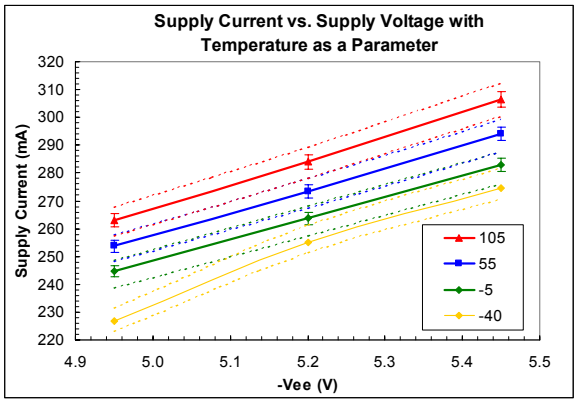


Figure 1. Measured power supply current vs. power supply voltage for 23 devices. The data at –40C were taken on 3 devices in the 49-ball, 6X6 mm BGA package.

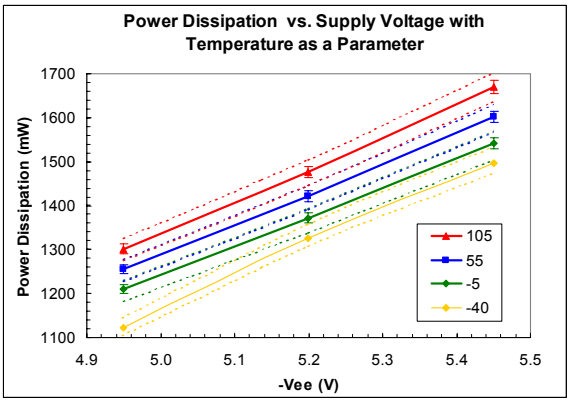


Figure 2. Measured power dissipation vs. power supply voltage for 23 devices. The data at –40C were taken on 3 devices in the 49-ball, 6X6 mm BGA package.

Typical Return Losses

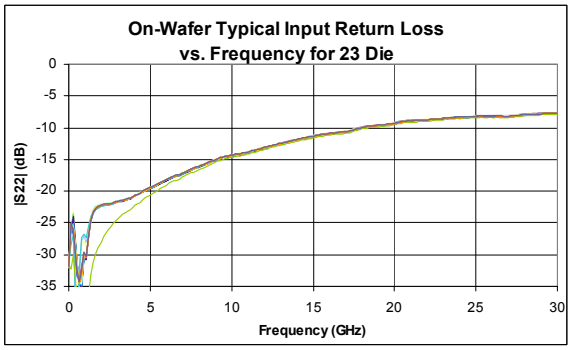


Figure 3. Measured input return loss for typical conditions (-5.2 V supply, 55 C back-side temperature, 0 V input common-mode and output termination voltage) for 23 devices.

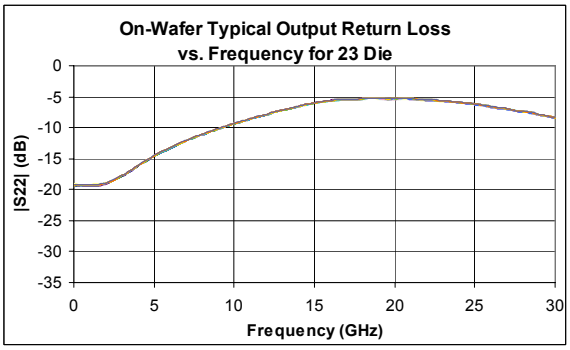


Figure 4. Measured output return loss for typical conditions (-5.2 V supply, 55 C back-side temperature, 0 V input common-mode and output termination voltage) for 23 devices.

Typical Sampling Characteristics

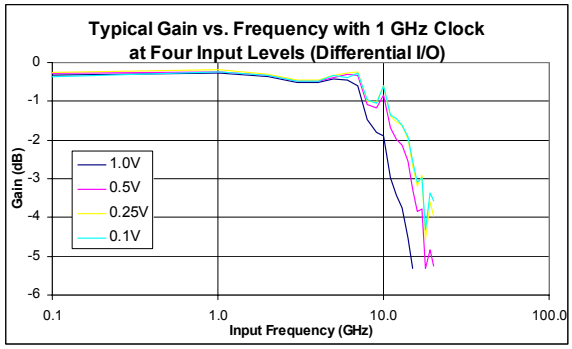


Figure 5. Measured gain of a single die for typical conditions (5.2 V supply, 55 C back-side temperature, 0 V input common-mode and output termination voltage) with differential inputs and outputs. A 1 Vpp differential clock at 1 GHz was applied. Output fundamental frequency was fixed at 20 MHz.

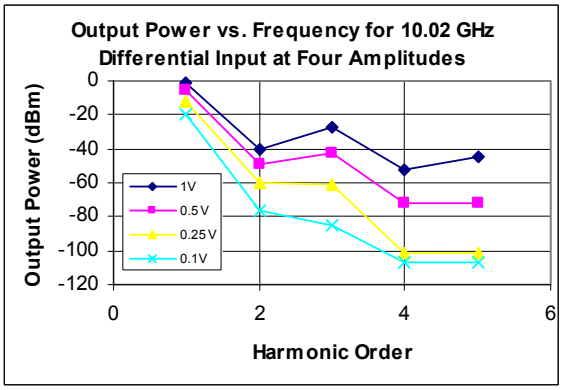


Figure 7. Measured output harmonic power of a single die for typical conditions (5.2 V supply, 55 C back-side temperature, 0 V input common-mode and output termination voltage) with differential inputs and outputs. A 1 Vpp differential clock at 1 GHz was applied.

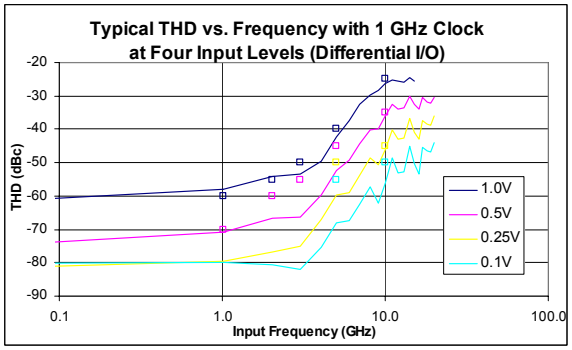


Figure 6. Measured THD of a single die for typical conditions (5.2 V supply, 55 C back-side temperature, 0 V input common-mode and output termination voltage) with differential inputs and outputs. A 1 Vpp differential clock at 1 GHz was applied. Output fundamental frequency was fixed at 20 MHz. Specification values are shown as squares on the plot.

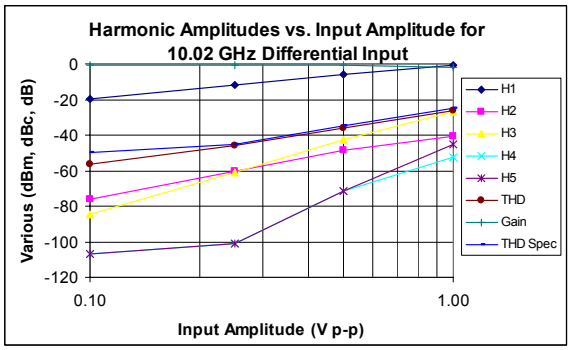


Figure 8. Measured output harmonic power of a single die for typical conditions (5.2 V supply, 55 C back-side temperature, 0 V input common-mode and output termination voltage) with differential inputs and outputs. A 1 Vpp differential clock at 1 GHz was applied.

Typical Sampling Characteristics at –40 C

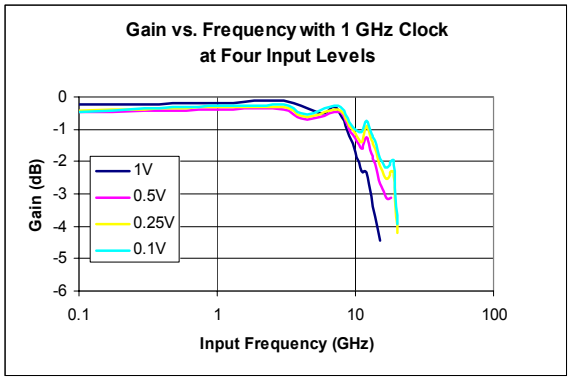


Figure 5. Measured gain of three BGA package parts on EVBs. Input conditions: -5.2 V supply, -40 C ball temperature, 0 V input common-mode and output termination voltage with differential inputs and outputs. A 1 Vpp differential clock at 1 GHz was applied. Output fundamental frequency was fixed at 20 MHz.

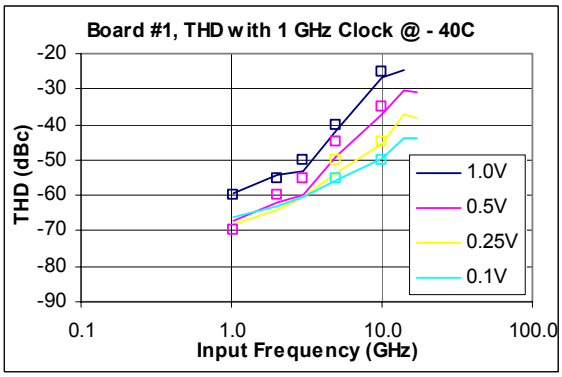


Figure 6. Measured THD of a single BGA package on EVB for typical conditions (-5.2 V supply, -40 C ball temperature, 0 V input common-mode and output termination voltage) with differential inputs and outputs. A 1 Vpp differential clock at 1 GHz was applied. Output fundamental frequency was fixed at 20 MHz. Specification values are shown as squares on the plot.

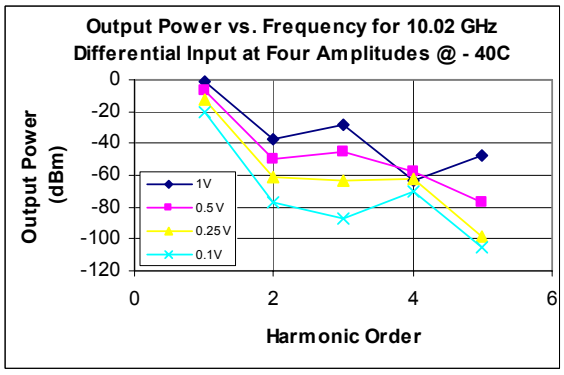


Figure 7. Measured output harmonic power of a single BGA package on EVB for typical conditions (-5.2 V supply, -40 C ball temperature, 0 V input common-mode and output termination voltage) with differential inputs and outputs.
A 1 Vpp differential clock at 1 GHz was applied.

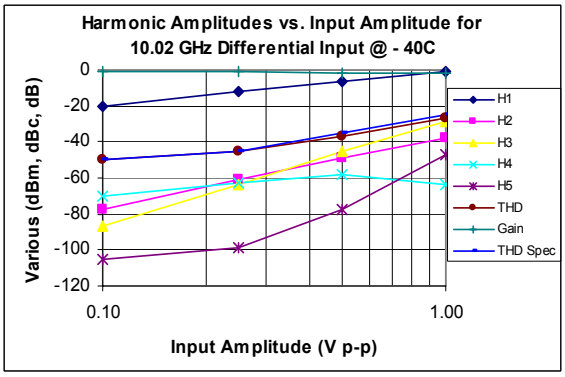


Figure 8. Measured output harmonic power of a single BGA package on EVB for typical conditions (-5.2 V supply, -40 C ball temperature, 0 V input common-mode and output termination voltage) with differential inputs and outputs.
A 1 Vpp differential clock at 1 GHz was applied.

V_T Pin Description

The voltage V_T sets the analog input termination voltage. This increases the range of signals that can be accurately sampled by adjusting their common-mode (V_{COM}) level at the THA inputs. Consider a differential input signal, with 50 Ω source impedance, that has a V_{COM} level when terminated into 50 Ω to ground. By setting V_T to -2 x V_{COM}, the common-mode level at the THA input pins is made zero. This feature can be used to adjust the input signal range to be within the specified input signal range for the THA. This can also be used for single-ended signal inputs, as illustrated by the following examples.

Consider first a differential, negative CML input pair with signal levels of -400 mV to 0 V on each side when terminated to 0 V (V_T=GND). The V_{COM} level of this differential signal is -200 mV. Setting V_T to +400 mV yields a 0 V V_{COM} level at the THA, analog input pins. Although the -200 mV original V_{COM} level would also be acceptable for the THA, this example shows the principle that can be applied to signals with larger V_{COM} voltages, either positive or negative.

Consider a single-ended, negative CML input to INp with a common-mode of -200 mV when terminated to GND. For optimal differential operation, the INn input should also be forced to -200 mV DC. If we set V_T to +400 mV, the INp common-mode becomes 0 V. In this case, since INn is terminated to V_T through 50 Ω, the INn common-mode voltage will be at +400 mV (V_T) if left disconnected. INn should be forced to 0 V either by connecting it through 50 Ω to -400 mV or by shorting it to GND.

The V_T pad (or ball) is well by-passed to GND on the die and in the package. Therefore, the analog inputs are AC terminated to GND. For proper DC termination V_T must be connected to either a DC supply or to GND. V_T may be forced to any value between -1 and 1 V, see the Maximum Ratings section.

V_{CMS} Pin Description

V_{CMS} is the clock mode select voltage. V_{CMS} digitally selects one of three clock modes for the two internal track-and-holds, TH1 and TH2. If left open, V_{CMS} by default assumes a level $V_{CMS,M}$ and CLK1 clocks both TH1 and TH2, out-of-phase. If forced low (V_{EE}), CLK1 clocks TH1 and CLK2 clocks TH2. If forced high (GND), both TH1 and TH2 are put into track mode and both CLK1 and CLK2 are ignored. For the voltage level ranges corresponding to the three states, see the I/O Electrical Specifications.

V_{TEMP} and G_{TEMP} Pin Description

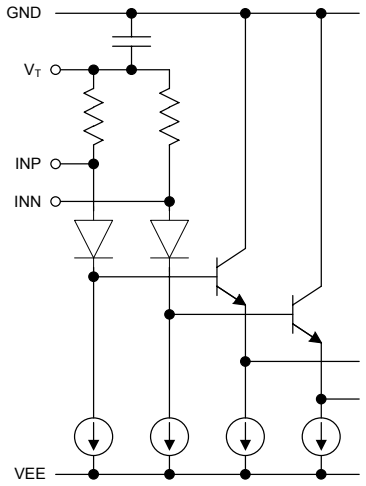
The V_{TEMP} and G_{TEMP} pins can be used to measure the chip temperature. The G_{TEMP} pin connects on-chip to GND and may serve as an extra GND connection when not used for temperature measurement. The V_{TEMP} pin connects to the G_{TEMP} through a parallel combination of two circuits: Circuit 1 is a series combination of two diodes, connected in the forward direction. Circuit 2 is a series combination of two similar diodes, connected in the reverse direction. V_{TEMP} does not connect in any other way to the rest of the IC. Although the GTEMP pin connects on-chip to GND, the connecting metal from G_{TEMP} to the diode combinations is routed so that it conducts only the diode currents, and no current of the rest of the IC. Therefore, the G_{TEMP} voltage accurately reflects the voltage at the diode terminals that connect to G_{TEMP}. Since V_{TEMP} only connects to the diode circuits, the voltage drop along the V_{TEMP} on-chip routing is also very small. These techniques are the same as the ones used in Kelvin probing.

The diodes are sized to provide their own ESD protection for stress on the V_{TEMP} terminal, see Absolute Maximum Ratings.

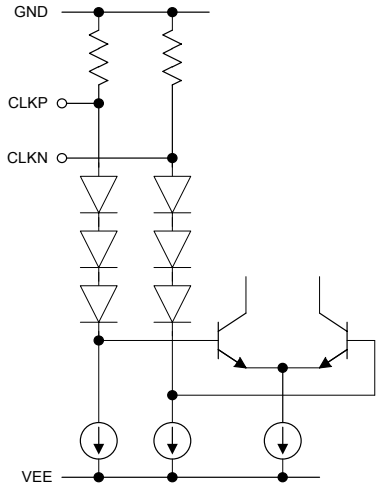
When forcing a positive current of, say 0.5 mA, from GTEMP to VTEMP, the voltage difference VTEMP – GTEMP will be about 1.2V at room temperature and will depend on the temperature of the two forward series diodes that conduct the current (the reverse biased series diodes conduct negligible current). The diodes (both forward and reverse combinations) are located near output buffer active circuitry. The reverse diodes allow the same type of temperature measurement to be done by forcing a negative current from GTEMP to VTEMP. For a current of -0.5mA for instance, the voltage VTEMP – GTEMP will now be -1.2V. The user thus has the option of measuring a positive or a negative voltage relative to GND level.

A calibration voltage vs. temperature curve for a fixed current may be obtained by measuring the mentioned voltage while changing the IC temperature in a controlled manner, e.g. mounted on a temperature chuck, with the IC powered off.

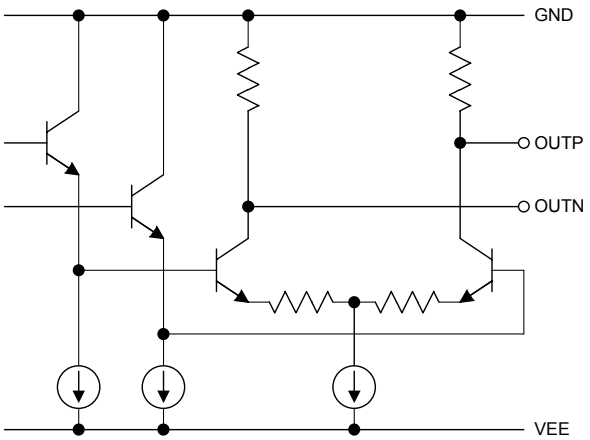
I/O Equivalent Circuits



Simplified analog input structure.

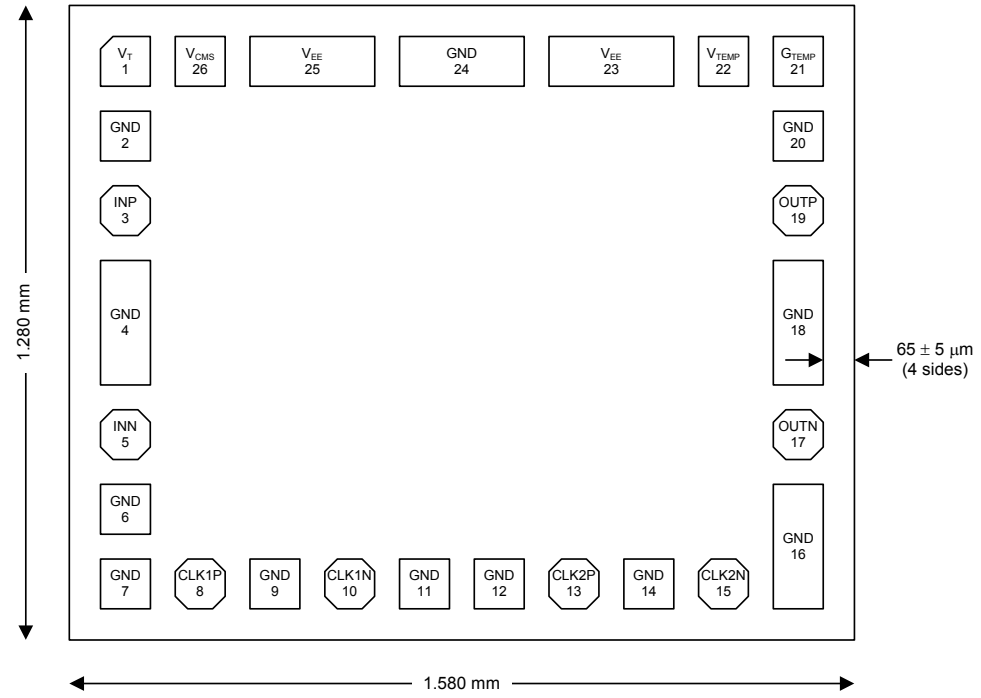


Simplified Clock1 and Clock2 input structure.



Simplified analog output structure.

Die Pad Layout



Notes:

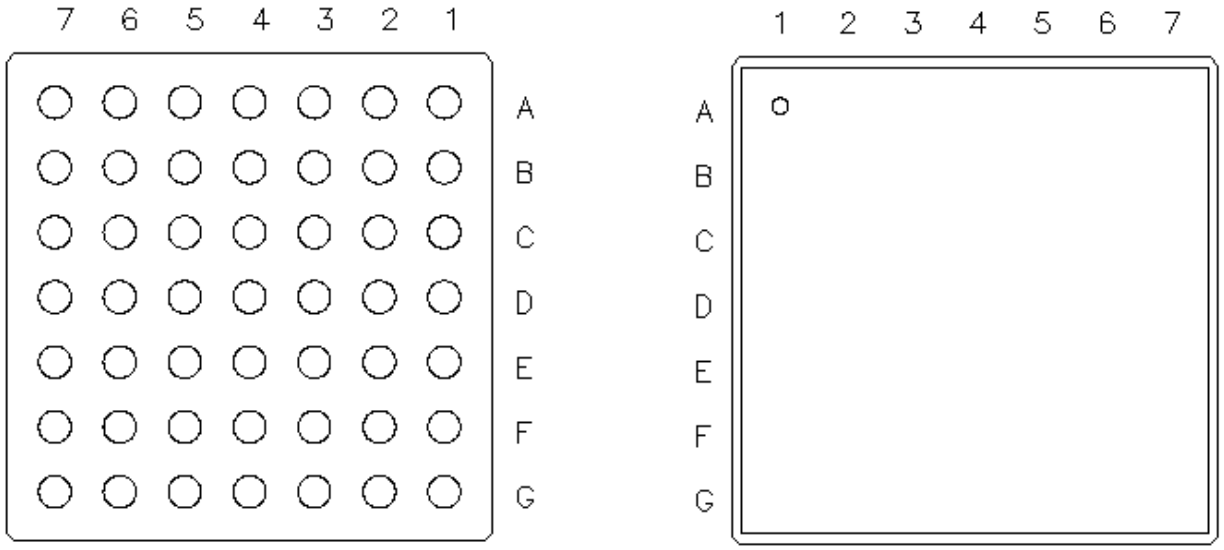
[1] Bond pads 4, 16, 18 are 100 **x** 250 µm², pads 23, 24, 25 are 250 **x** 100 µm², other pads are 100 **x** 100 µm².

[2] Gaps between bond pads are 50 µm.

[3] Die thickness: 150 ± 10 µm

Name	Pad	Description	Function
INp, INn	3, 5	Analog Inputs	Input
CLK1p, CLK1n	8, 10	Clock 1 Inputs	Input
CLK2p, CLK2n	13, 15	Clock 2 Inputs	Input
OUTp, OUTn	19, 17	Analog Outputs	Output
V_T	1	Termination Voltage for Analog Inputs	Input
V_{CMS}	26	Clock Mode Select	Digital Input
V_{TEMP}	22	Temperature Diode Voltage	Input
G_{TEMP}	21	Ground Sense Voltage for Temperature Diode	Output
V_{EE}	23, 25	Power Supply: Connect to -5.2 V	Supply
GND	2, 4, 6, 7, 9, 11, 12, 14, 16, 18, 20, 24	Ground	Supply

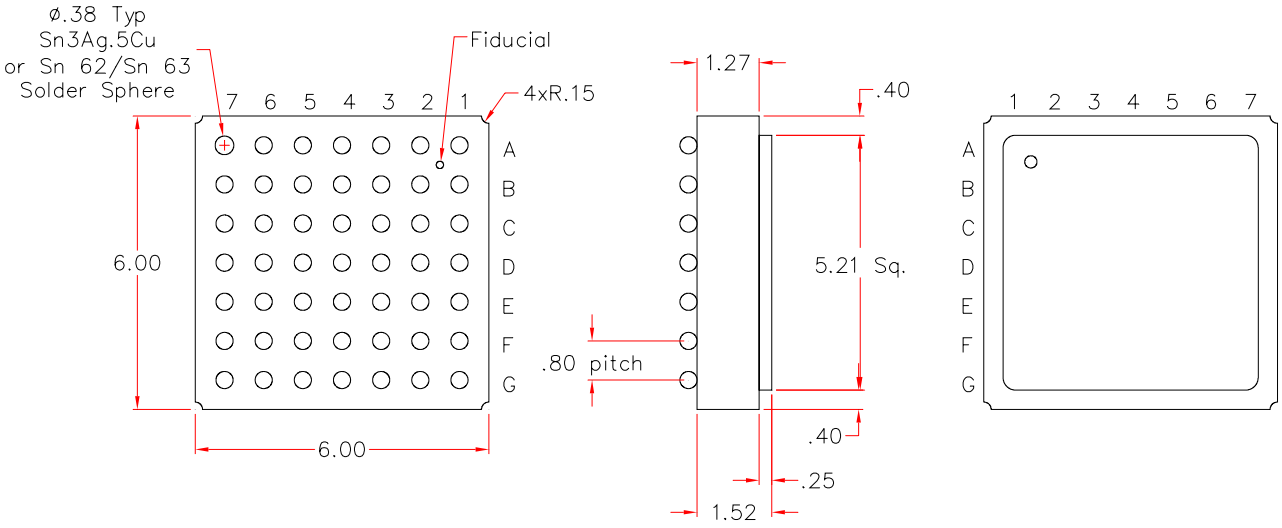
6 mm BGA Ball Out Information



Bottom View **Top View**

Name	Ball	Description	Function
INp, INn	C1, E1	Analog Inputs	Input
OUTp, OUTn	C7, E7	Analog Outputs	Output
CLK1p, CLK1n	G2, G3	Clock 1 Inputs	Input
CLK2p, CLK2n	G5, G6	Clock 2 Inputs	Input
V_T	A1	Termination Voltage for Analog Inputs	Input
V_{CMS}	A2	Clock Mode Select	Digital Input
V_{TEMP}	A6	Temperature Diode Voltage	Input
G_{TEMP}	A7	Ground Sense Voltage for Temperature Diode	Output
V_{EE}	A3-A5, B3, B5	Power Supply: Connect to -5.2 V	Supply
GND	B1, B2, B4, B6, B7, C2-C6, D1-D7, E2-E6, F1-F7, G4	Ground	Supply
N.C.	G1, G7	No Internal Connection	NC

6 mm BGA Package Outline Drawing



6 mm Fine Pitch Ceramic BGA with 0.8 mm pitch. Package is hermetic and thermal path is down through solder balls.

Order Information

Part No.	Description
1821TH-S01D	2 GS/s Track and Hold Amplifier in die form
1821TH-S01BPB	2 GS/s Track and Hold Amplifier in 49 pin BGA package with Lead balls
1821TH -S01BLF	2 GS/s Track and Hold Amplifier in 49 pin BGA package with Lead-free balls
1821TH-S01BPBEVB	2 GS/s Track and Hold Amplifier in 49 pin BGA package with Lead balls on an Evaluation Board with SMA Connectors

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Limited Qualification Notification

NOTE: The 1821TH has not undergone qualification testing (i.e. it has not been subjected to high temperature operation life test), a number of other products fabricated in the same semiconductor process have completed full qualification testing and have been demonstrated to be reliable. Contact Inphi Corporation for more details. As of the date of this datasheet release, the Absolute Maximum Ratings have not been fully tested.

Version History

Version 1.0 Introduction - (dated 3/21/06).
First Version.

From Version 1.0 to Version 1.1 (dated 4/17/06):

1. Added thermal comments to Descriptions section and thermal resistance to Operating Conditions table.
2. Corrected BGA Package Outline Drawing.
3. Added "Pb" (Lead balls) and "Lf" (Lead-free balls) designations to BGA part numbers.

From Version 1.1 to Version 1.2 (dated 4/21/06):

1. Reworded several table footnotes and pin descriptions on various pages.
2. Corrected signal names in 6 mm BGA Ball Out Information table on page 15.
3. Added "Sn63" to solder ball description in 6 mm BGA Package Outline Drawing on page 16.
4. Changed part numbers in Order Information section on page 17.

From Version 1.2 to Version 1.3 (dated 2006-12-19):

1. Changes to the Absolute Maximum Ratings section (page 3):
    a. Changed Minimum Shipping/Storage Temperature from -40°C to -65°C.
2. Changes to the Operating Conditions section (page 4):
    a. Changed the Operating Case Temperature from -5°C to -40°C.
3. Changes to the Electrical Specifications: RF I/O section (page 5):
    a. The RF Input Resistance and Clock Input Resistance Test Levels changed from 2 to 1.
    b. A temperature range test condition of –5°C to +85°C was added to the Gain specification.
    c. A second line was added to the Gain specification and a minimum value of 0.85 was used for the temperature range of –40°C to +85°C.
    d. A temperature range test condition of –5°C to +85°C was added to the Gain Drift specification and the typical value changed from 230 ppm/°C to –100 ppm/°C.
    e. A second line was added to the Gain Drift specification with a typical value of 430 ppm/°C for the temperature range of –40°C to –5°C.
    f. The minimum Offset Drift specification was defined to be –50 uV/°C.
    g. The maximum Offset Drift specification was defined to be +60 uV/°C.
4. Changes to the Electrical Specifications: Dynamic section (page 7):
    a. The Gain Flatness Deviation typical specification was defined to be ±0.5 dB.
    b. The Gain Flatness Deviation maximum specification was changed from ±0.5 dB to ±0.8 dB.
    c. One line was added to the Integrated Noise specification and the following changes made:
        i. Existing test conditions were moved to a new note (#1).
        ii. The conditions on the first line were defined as "Over the first Nyquist band" and the typical value set to 0.64 mV.
        iii. The conditions on the second line were defined as "Over second Nyquist band" and the typical value set to 0.32 mV.
    d. Noise Floor typical value changed from TBD to 22.3 nV/√Hz
    e. Several typical values and all maximum values were changed for the Total Harmonic Distortion specification.
5. Changes to the Typical DC Operating Characteristics section (page 10):
    a. The Supply Current over power and temperature graph was updated with –40°C data.
    b. The Power Dissipation over power and temperature graph was updated with –40°C data.
6. The Typical Sampling Characteristics at –40°C section was added. This section has all of the same graphs as the Typical Sampling Characteristics section, except that the data is all from operation at –40°C.
7. The footer date and document filename version were updated.

From Version 1.3 to Version 1.4 (dated 2007-01-17):

1. Changes to the Absolute Maximum Ratings section (page 3):
    a. Changed Minimum Junction Temperature (die) from -15°C to -47°C.
    b. Changed Minimum Case Temperature (package) from -40°C to -65°C.
2. Changes to the Operating Conditions section (page 4):
    a. Changed the Operating Junction Temperature from 15°C to -22°C.
    b. Added footnote #1.
3. Changes to the Electrical Specifications: Dynamic section (page 7):
    a. Added 14 & 17 GHz typical values to the THD specification.
    b. Added footnote #4.
4. Changes to the Electrical Specifications: TH1 Switching section (page 8):
    a. Added footnote #6.
5. Changes to the Typical DC Operating Characteristics section (page 10):
    a. Added a reference to the device form being the BGA package for –40C data to Fig. 1 & 2.
6. Changes to the Typical Sampling Characteristics at –40°C section (page 12).
    a. Added a reference to the device form being the BGA package.
7. Deleted the reference to validation testing in the Limited Qualification Notification section.