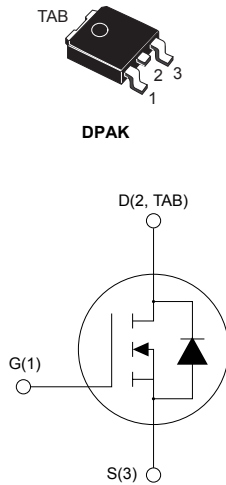


N-channel 550 V, 150 mΩ typ., 16 A MDmesh M5 Power MOSFET in a DPAK package



AM01475v1_noZen



Features

| Order code | V_{DS} at T_J max. | $R_{DS(on)}$ max. | I_D |
|------------|------------------------|-------------------|-------|
| STD18N55M5 | 600 V | 192 mΩ | 16 A |

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link

[STD18N55M5](#)

Product summary

| | |
|-------------------|---------------|
| Order code | STD18N55M5 |
| Marking | 18N55M5 |
| Package | DPAK |
| Packing | Tape and reel |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|------------------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 16 | A |
| | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 10 | |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 64 | A |
| P_{TOT} | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 110 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating junction temperature range | | $^\circ\text{C}$ |

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 16\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 340\text{ V}$.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|------------------|---|-------|---------------------------|
| R_{thJC} | Thermal resistance, junction-to-case | 1.14 | $^\circ\text{C}/\text{W}$ |
| $R_{thJA}^{(1)}$ | Thermal resistance, junction-to-ambient | 50 | $^\circ\text{C}/\text{W}$ |

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.) | 4 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 210 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ | 550 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 550\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 550\text{ V}$, $T_C = 125\text{ °C}^{(1)}$ | | | 100 | |
| I_{GSS} | Gate body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$ | | 150 | 192 | m Ω |

1. Specified by design, not tested in production.

Table 5. Dynamic

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|---|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 1260 | - | pF |
| C_{oss} | Output capacitance | | - | 42 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 3.6 | - | pF |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related | $V_{DS} = 0\text{ to }440\text{ V}$, $V_{GS} = 0\text{ V}$ | - | 103 | - | pF |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related | | - | 35 | - | pF |
| R_g | Gate input resistance | $f = 1\text{ MHz}$ open drain | - | 2.8 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 440\text{ V}$, $I_D = 8\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ | - | 31 | - | nC |
| Q_{gs} | Gate-source charge | (see Figure 15. Test circuit for gate charge behavior) | - | 8.3 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 14.2 | - | nC |

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|--------------|--------------------|--|------|------|------|------|
| $t_{d(v)}$ | Voltage delay time | $V_{DD} = 400\text{ V}$, $I_D = 10.5\text{ A}$, | - | 37 | - | ns |
| $t_{r(v)}$ | Voltage rise time | $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ | - | 7 | - | ns |
| $t_{c(off)}$ | Crossing time | (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform) | - | 10.3 | - | ns |
| $t_{f(i)}$ | Current fall time | | - | 8.3 | - | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 16 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 64 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 16\text{ A}$, $V_{GS} = 0\text{ V}$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, | - | 244 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 100\text{ V}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 2.8 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 23 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | - | 295 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 3.7 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 25 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

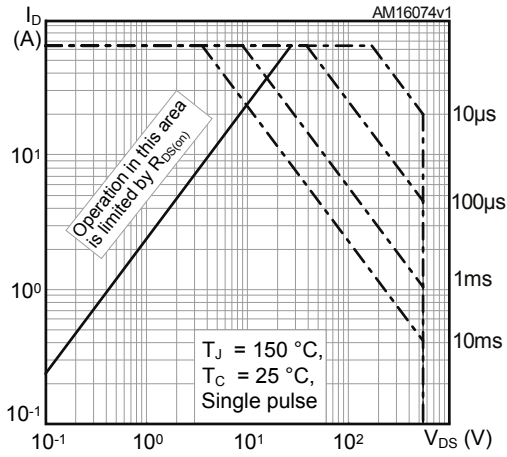


Figure 2. Thermal impedance

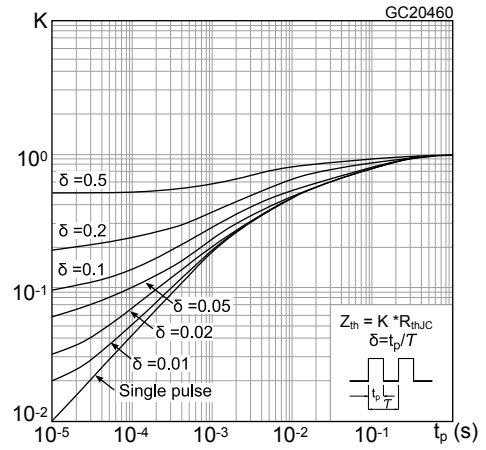


Figure 3. Output characteristics

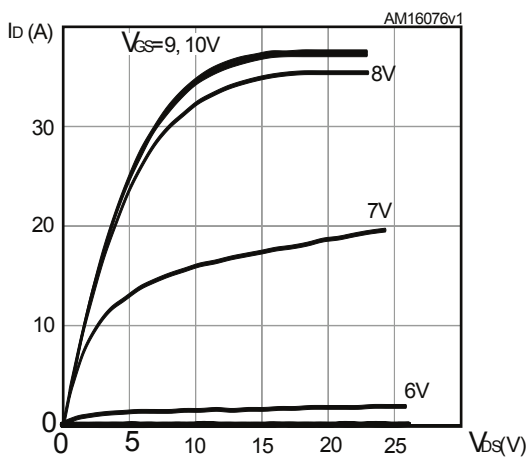


Figure 4. Transfer characteristics

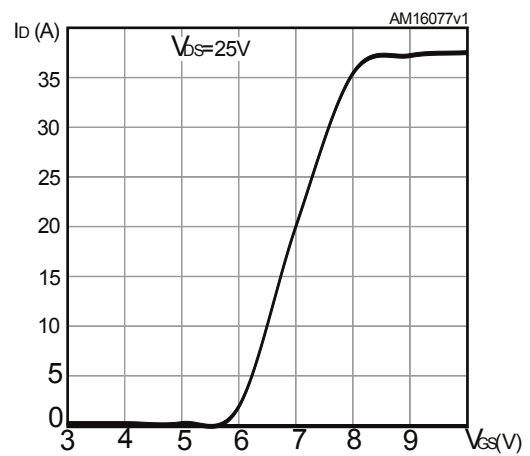


Figure 5. Gate charge vs gate-source voltage

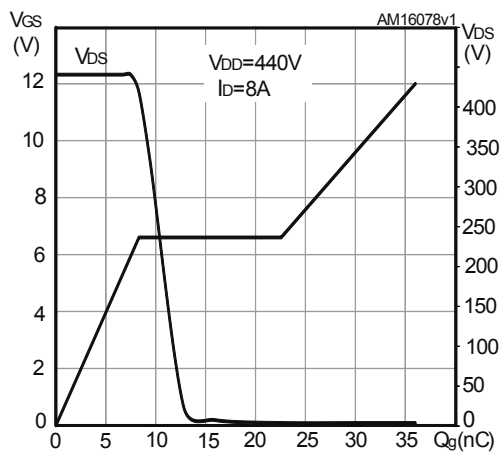


Figure 6. Static drain-source on resistance

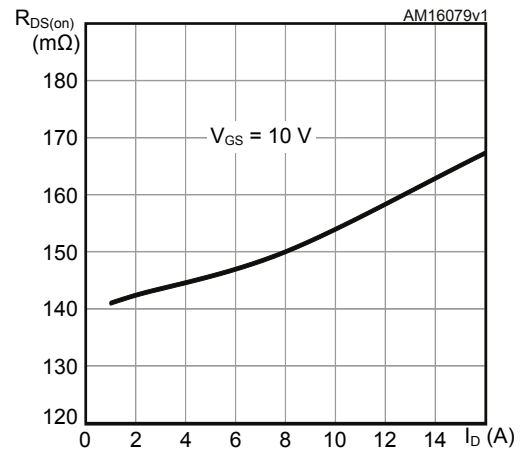


Figure 7. Capacitance variations

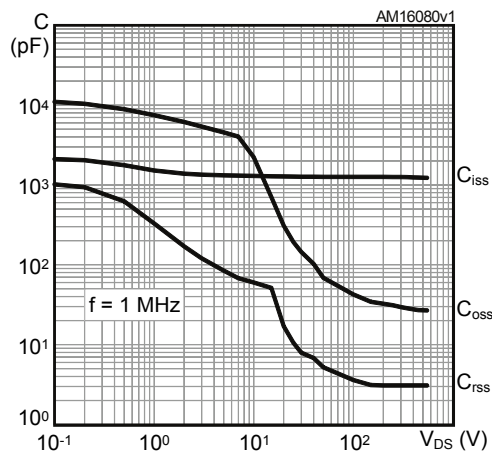


Figure 8. Output capacitance stored energy

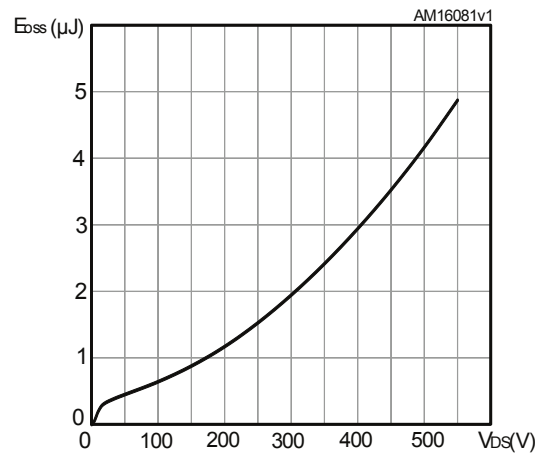


Figure 9. Normalized gate threshold voltage vs temperature

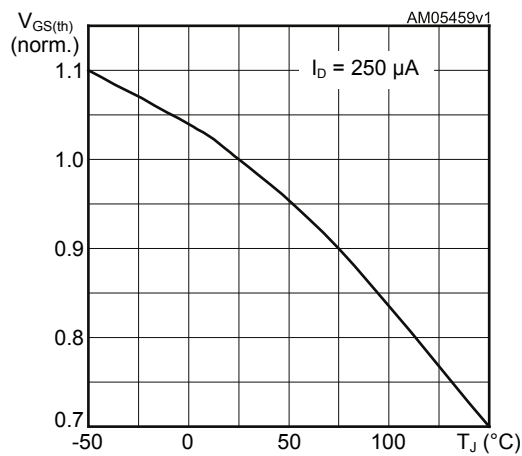


Figure 10. Normalized on-resistance vs temperature

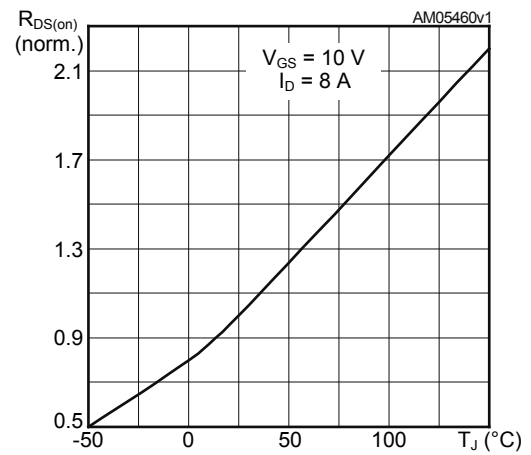


Figure 11. Drain-source diode forward characteristics

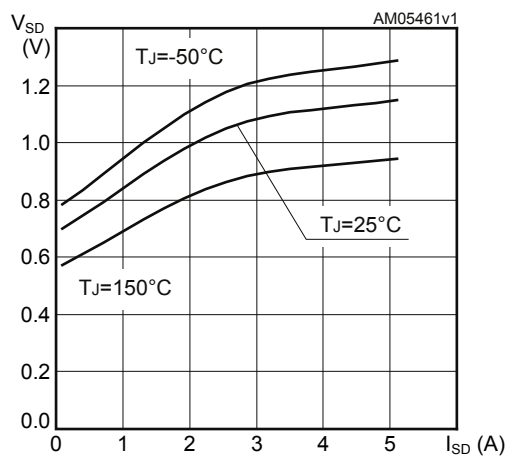


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature

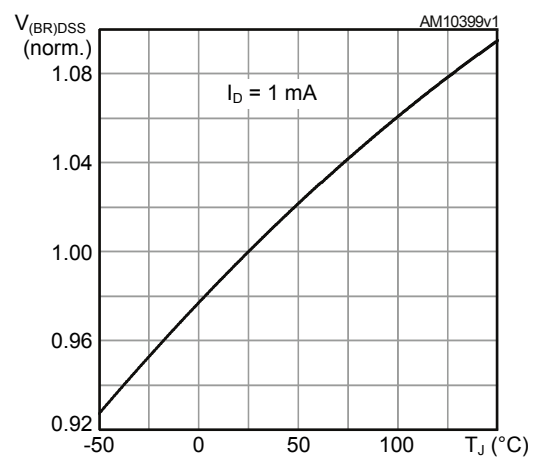
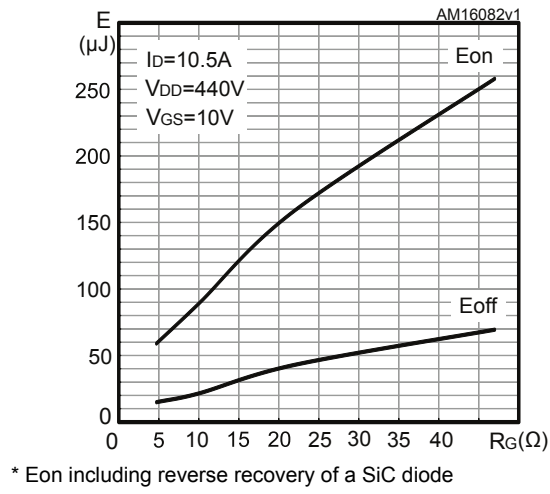
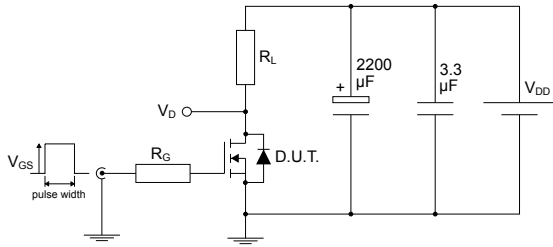


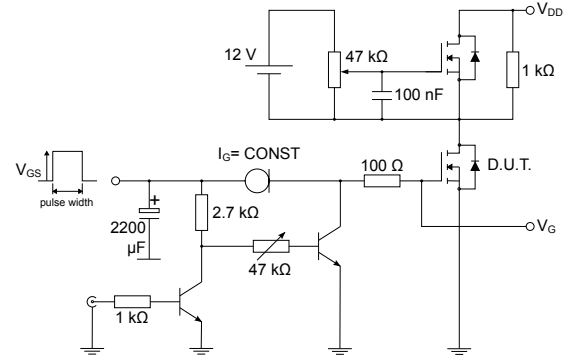
Figure 13. Switching energy vs gate resistance



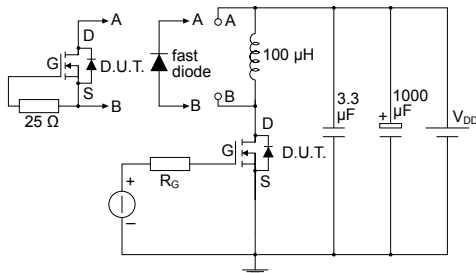
3 Test circuits

Figure 14. Test circuit for resistive load switching times


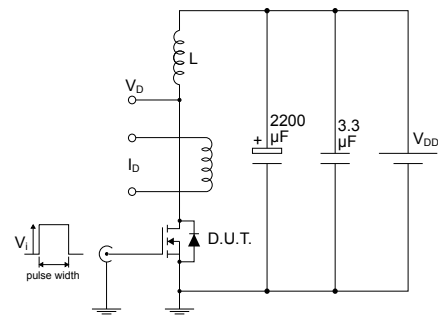
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Figure 15. Test circuit for gate charge behavior


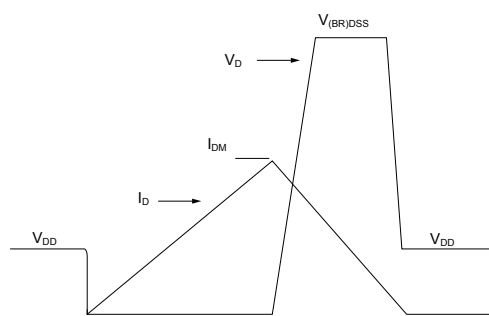
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Figure 16. Test circuit for inductive load switching and diode recovery times


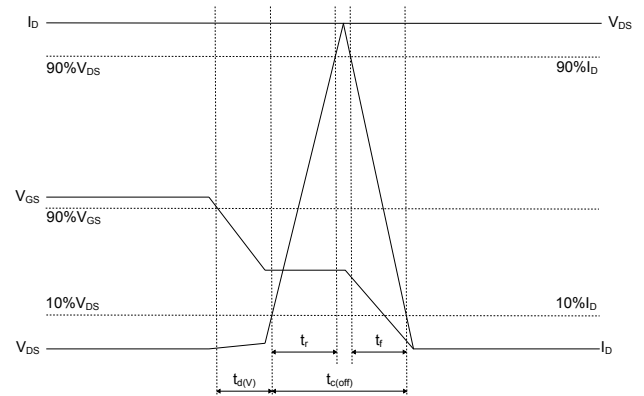
AM01470v1

Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


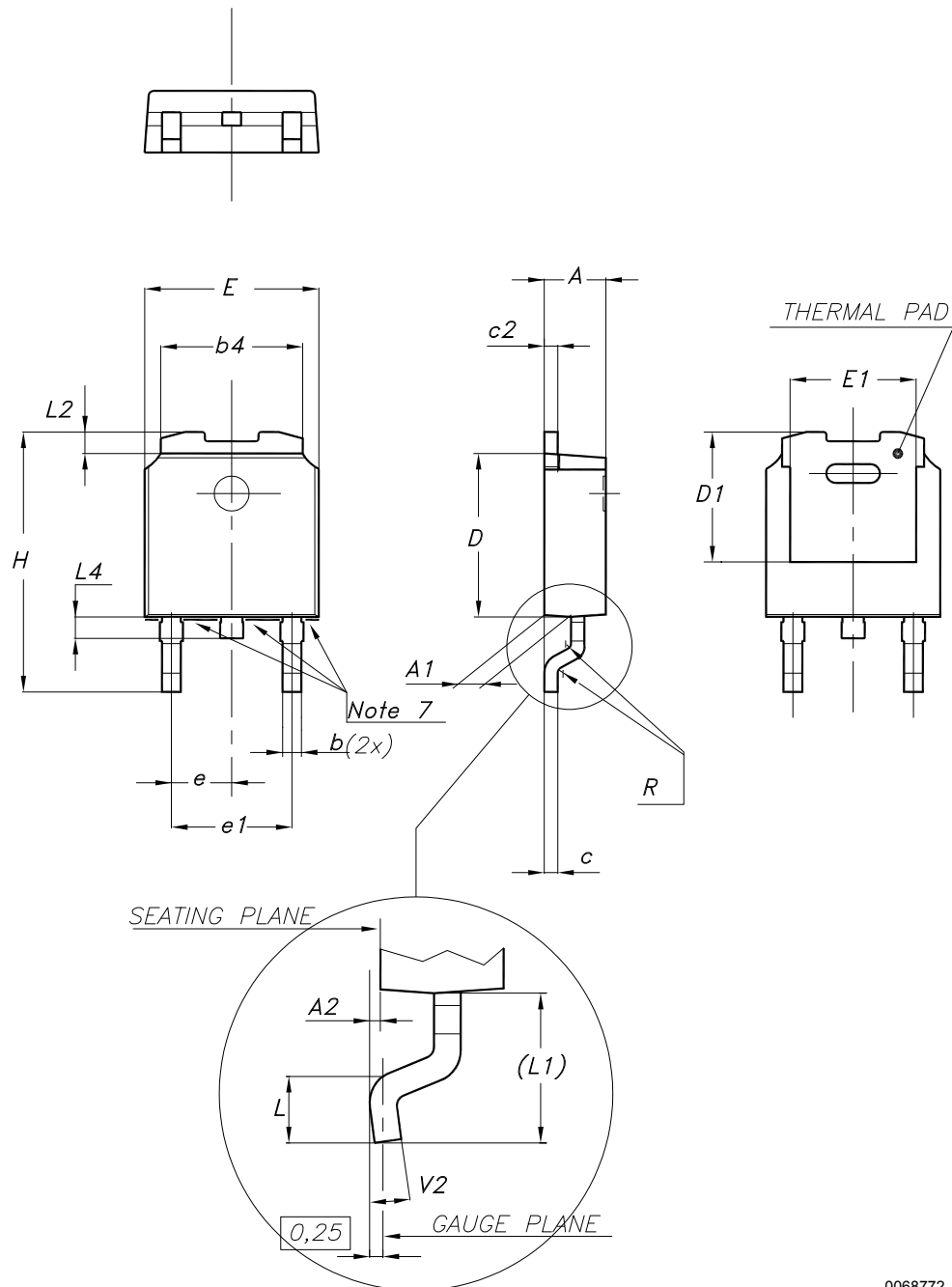
AM05540v2

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 20. DPAK (TO-252) type A2 package outline



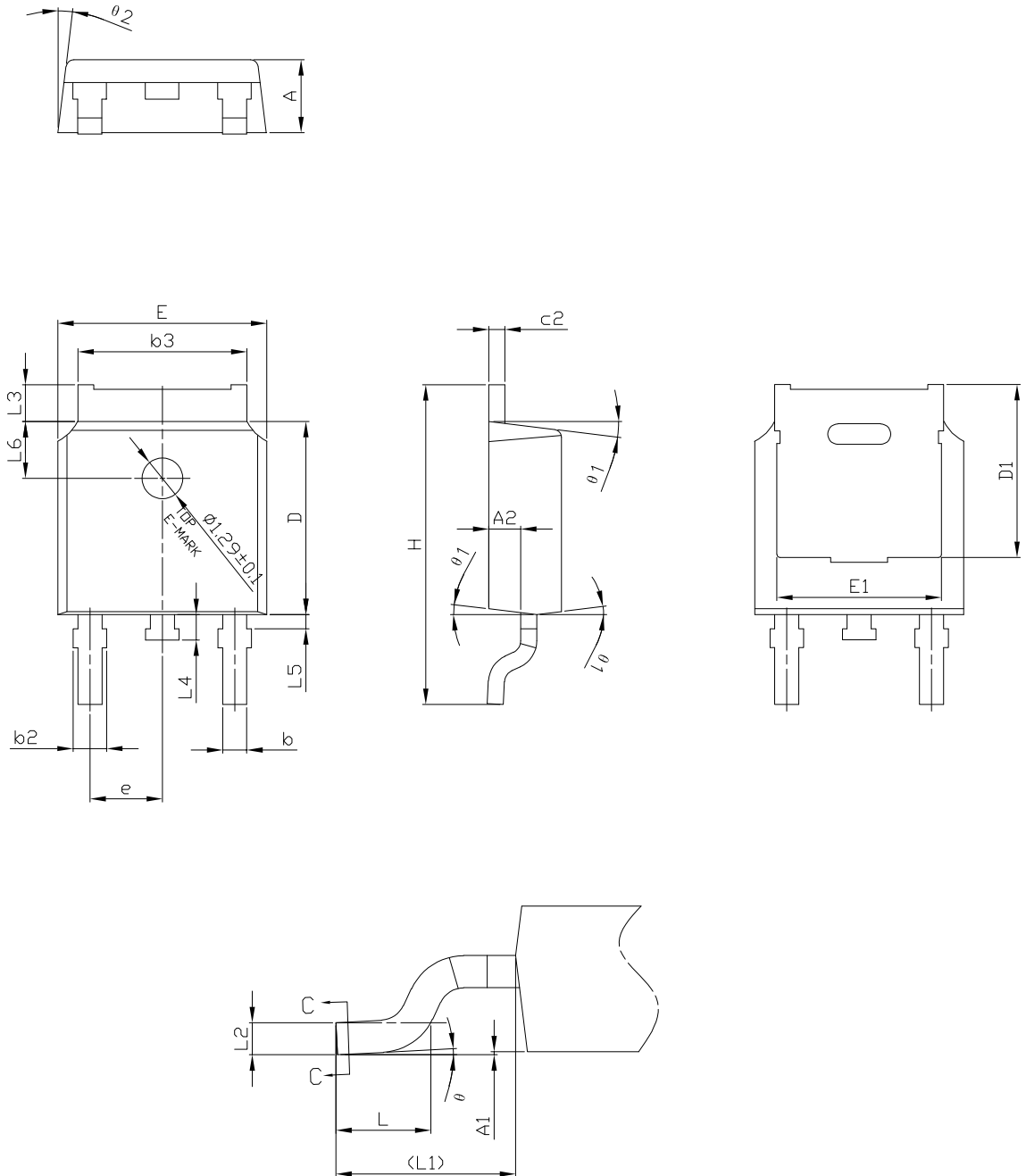
0068772_type-A2_rev34

Table 8. DPAK (TO-252) type A2 mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 5.10 | 5.20 | 5.30 |
| e | 2.159 | 2.286 | 2.413 |
| e1 | 4.445 | 4.572 | 4.699 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| L1 | 2.60 | 2.80 | 3.00 |
| L2 | 0.65 | 0.80 | 0.95 |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

4.2 DPAK (TO-252) type C3 package information

Figure 21. DPAK (TO-252) type C3 package outline

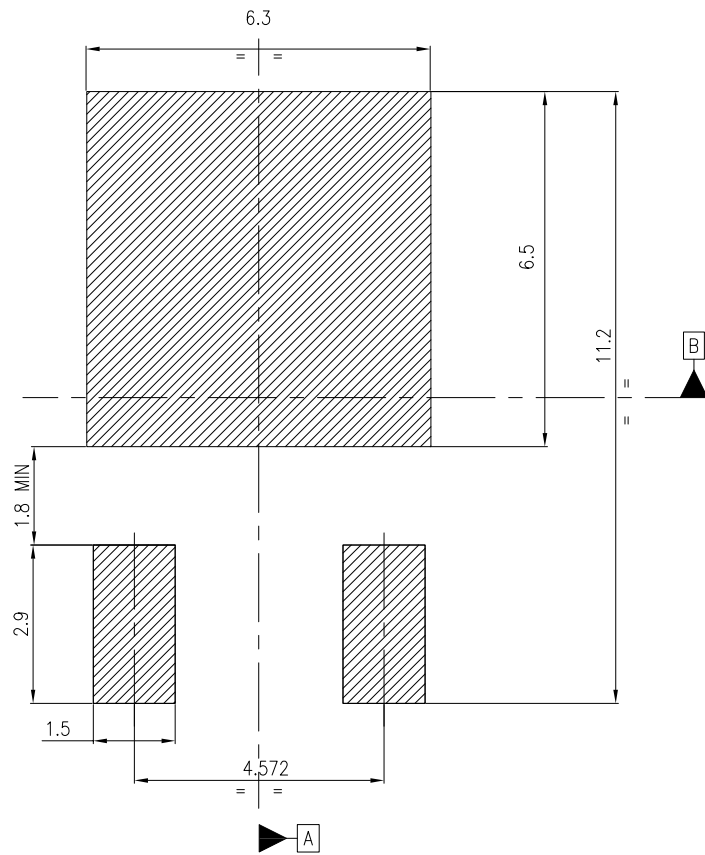


0068772_type-C3_rev34

Table 9. DPAK (TO-252) type C3 mechanical data

| Dim. | mm | | |
|------|----------|-------|-------|
| | Min. | Typ. | Max. |
| A | 2.20 | 2.30 | 2.38 |
| A1 | 0.00 | | 0.10 |
| A2 | 0.90 | 1.01 | 1.10 |
| b | 0.72 | | 0.85 |
| b2 | 0.72 | | 1.10 |
| b3 | 5.13 | 5.33 | 5.46 |
| c | 0.47 | | 0.60 |
| c2 | 0.47 | | 0.60 |
| D | 6.00 | 6.10 | 6.20 |
| D1 | 5.20 | 5.45 | 5.70 |
| E | 6.50 | 6.60 | 6.70 |
| E1 | 5.00 | 5.20 | 5.40 |
| e | 2.186 | 2.286 | 2.386 |
| H | 9.80 | 10.10 | 10.40 |
| L | 1.40 | 1.50 | 1.70 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.90 | | 1.25 |
| L4 | 0.60 | 0.80 | 1.00 |
| L5 | 0.15 | | 0.75 |
| L6 | 1.80 REF | | |
| θ | 0° | | 8° |
| θ1 | 5° | 7° | 9° |
| θ2 | 5° | 7° | 9° |

Figure 22. DPAK (TO-252) recommended footprint (dimensions are in mm)



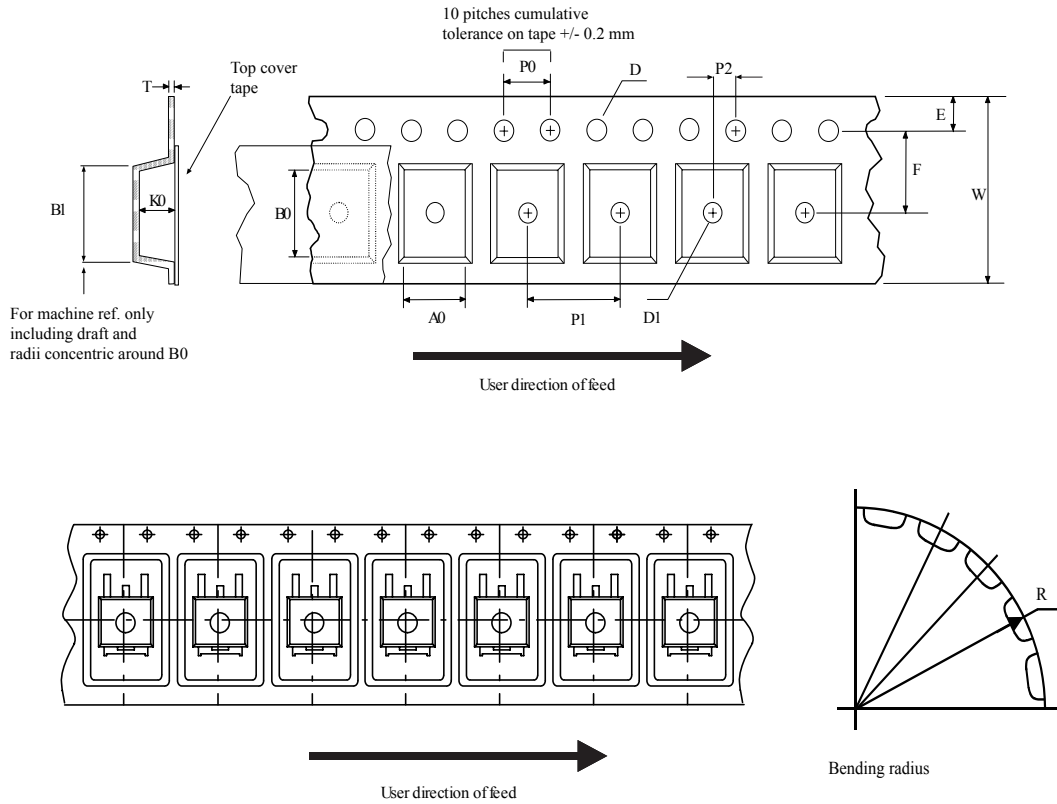
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\boxed{\oplus 0.05 \text{ A B}}$

FP_0068772_34

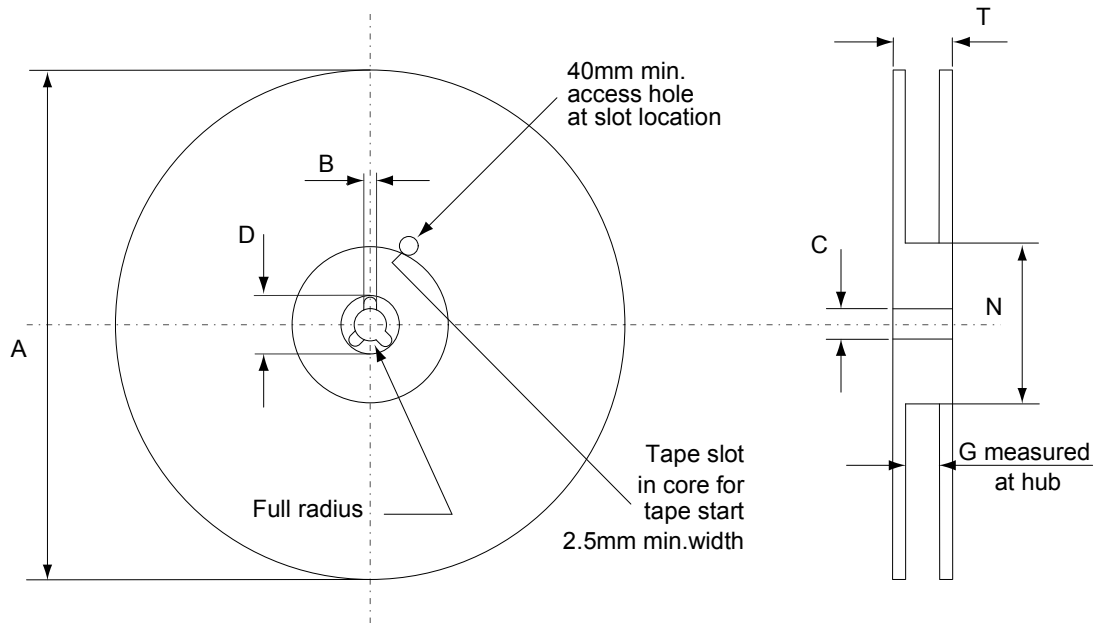
4.3 DPAK (TO-252) packing information

Figure 23. DPAK (TO-252) tape outline



AM08852v1

Figure 24. DPAK (TO-252) reel outline



AM06038v1

Table 10. DPAK (TO-252) tape and reel mechanical data

| Dim. | Tape | | Dim. | Reel | |
|------|------|------|-----------|------|------|
| | mm | | | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 09-Feb-2010 | 1 | First release. |
| 04-Mar-2011 | 2 | <ul style="list-style-type: none"> – Document status promoted from preliminary data to datasheet; – Added new package, mechanical data: D²PAK. |
| 22-Nov-2013 | 3 | <ul style="list-style-type: none"> – Updated: title on the cover page and RDS(on) values. – Modified: EAS value and note 3 in Table 2 – Modified: RDS(on) value in Table 4, typical values in Table 5 and 7 – Updated: the entire Table 5 – Added: Section 2.1: Electrical characteristics (curves) – Updated: Section 4: Package mechanical data and Section 5: Packaging mechanical data – Updated: Figure 11 and 18 – Minor text changes. |
| 03-Aug-2018 | 4 | <p>The part numbers STB18N55M5 and STF18N55M5 have been moved to a separate datasheet.</p> <p>Removed maturity status indication from cover page. The document status is production data.</p> <p>Updated title in cover page, Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 4 Package information.</p> <p>Minor text changes.</p> |
| 24-Mar-2020 | 5 | <p>Updated title on <i>Figure 12. Normalized gate threshold voltage vs temperature</i> and <i>Figure 13. Normalized on-resistance vs temperature</i>.</p> <p>Updated <i>Section 4 Package information</i>.</p> <p>Minor text changes.</p> |
| 19-Jul-2023 | 6 | <p>The part number STP18N55M5 has been moved to a separate datasheet and the document has been updated accordingly.</p> <p>Updated Features on cover page.</p> <p>Updated Section 4.1 DPAK (TO-252) type A2 package information and replaced "Section 4.2 DPAK (TO-252) type C2 package information" with Section 4.2 DPAK (TO-252) type C3 package information.</p> <p>Minor text changes.</p> |

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| | Revision history | 16 |

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