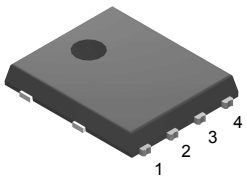
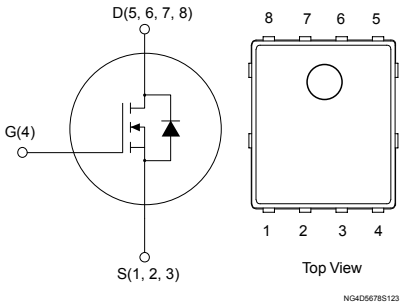
STL19N3LLH6AG

Datasheet

Automotive-grade N-channel 30 V, 23 mΩ typ., 10 A, STripFET™ H6 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT™ 5x6



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL19N3LLH6AG	30 V	33 mΩ	10 A	50 W

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Logic level
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STL19N3LLH6AG

Product summary	
Order code	STL19N3LLH6AG
Marking	19N3LLH6
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_{case} = 25 °C	10	A
	Drain current (continuous) at T_{case} = 100 °C	10	
I_{DM}(2)	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	50	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		

1. *Current limited by package. At T_{case} = 25 °C the silicon is able to sustain 30 A.*
2. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	3	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	31.3	

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board, t< 10 s.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}(1)	Avalanche current, repetitive or not repetitive	10	A
E_{AS}(2)	Single pulse avalanche energy	130	mJ

1. *Pulse width limited by T_{jmax}*
2. *Starting T_j = 25 °C, I_D = I_{AV}, V_{DD} = 25 V*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	30			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 30 V			1	µA
		V_{GS} = 0 V, V_{DS} = 30 V, T_{case} = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5 A		23	33	mΩ
		V_{GS} = 4.5 V, I_D = 5 A		33	43	

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	321	-	pF
C_{oss}	Output capacitance		-	68	-	
C_{rss}	Reverse transfer capacitance		-	34	-	
Q_g	Total gate charge	V_{DD} = 15 V, I_D = 10 A, V_{GS} = 0 to 4.5 V (see Figure 13. Test circuit for gate charge behavior)	-	3.7	-	nC
Q_{gs}	Gate-source charge		-	1	-	
Q_{gd}	Gate-drain charge		-	1.7	-	

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	2.4	-	ns
t_r	Rise time		-	2.5	-	
$t_{d(off)}$	Turn-off delay time		-	12.8	-	
t_f	Fall time		-	2.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
I_{SDM}(1)	Source-drain current (pulsed)		-		40	A

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 10 A	-		1.12	V
t_{rr}	Reverse recovery time	I_{SD} = A, di/dt = 100 A/µs,	-	15.1		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 24 V	-	7.5		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	1		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

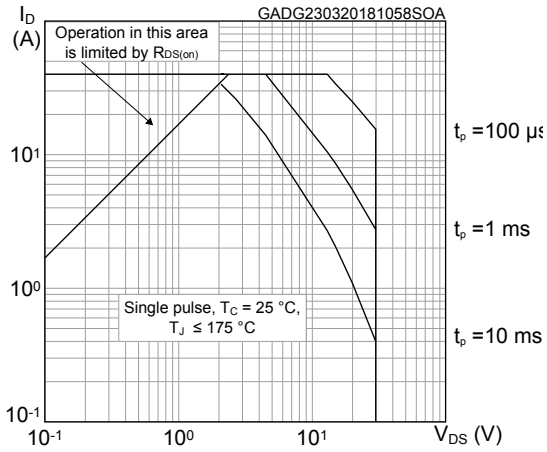


Figure 2. Thermal impedance

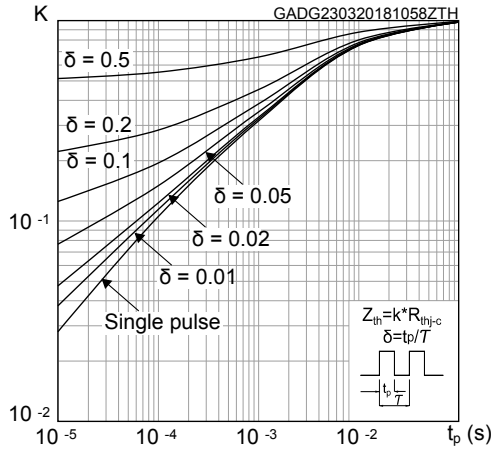


Figure 3. Output characteristics

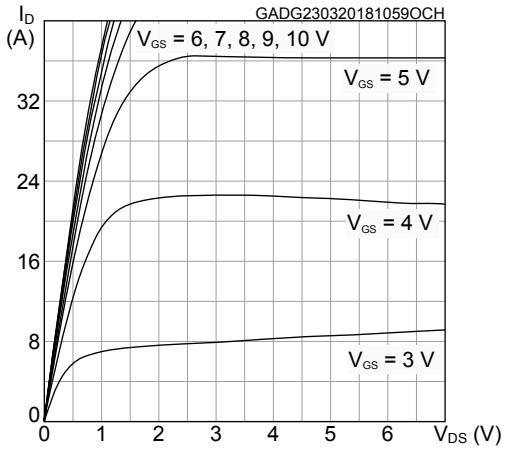


Figure 4. Transfer characteristics

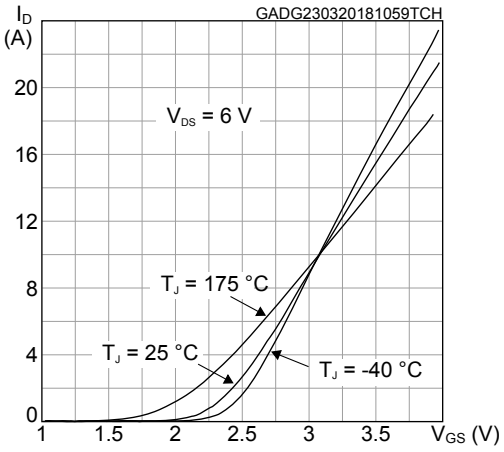


Figure 5. Gate charge vs gate-source voltage

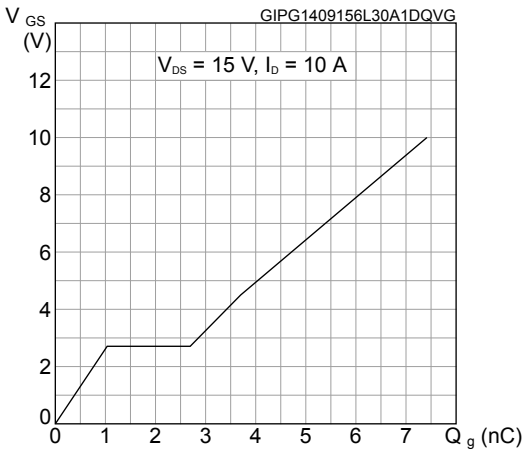


Figure 6. Static drain-source on-resistance

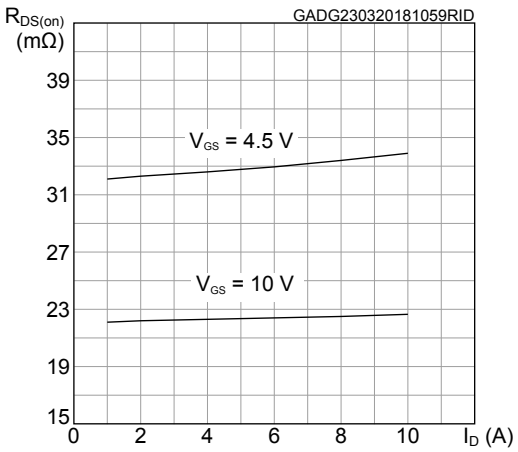


Figure 7. Capacitance variations

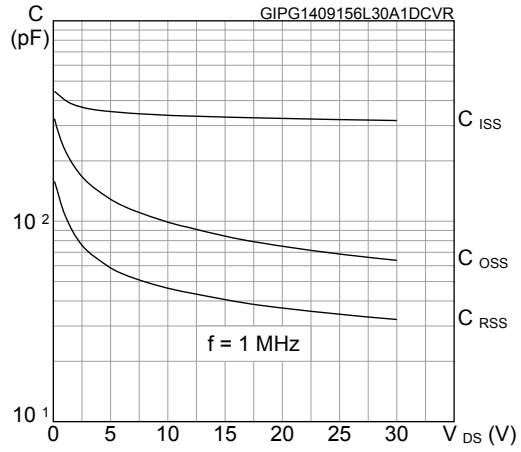


Figure 8. Normalized gate threshold voltage vs temperature

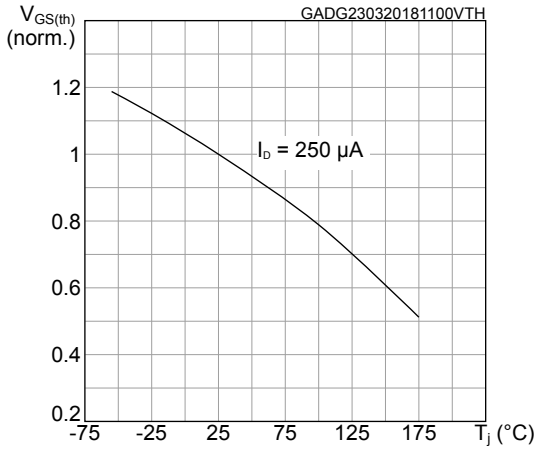


Figure 9. Normalized on-resistance vs temperature

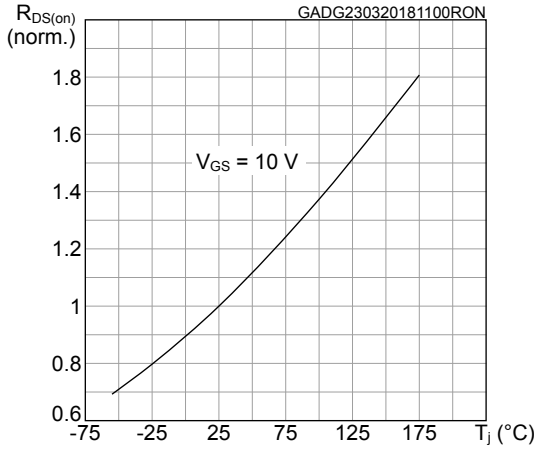


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

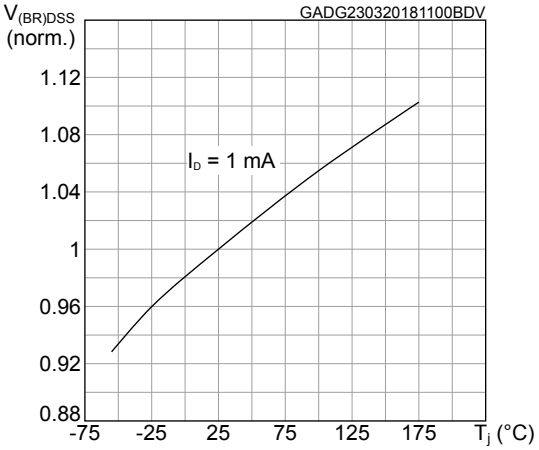
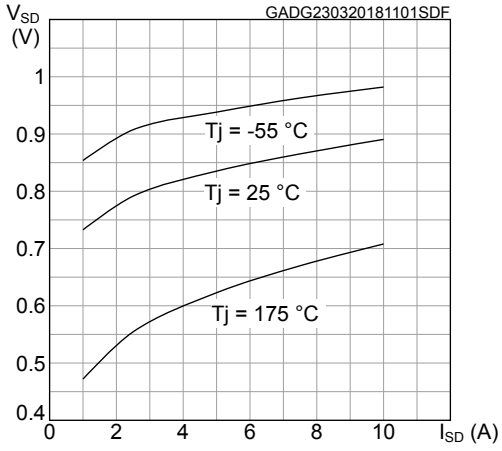


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

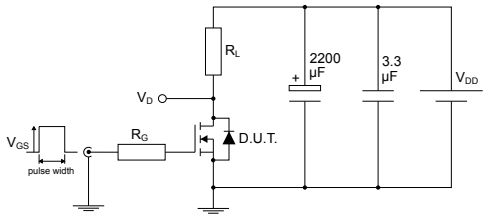


Figure 13. Test circuit for gate charge behavior

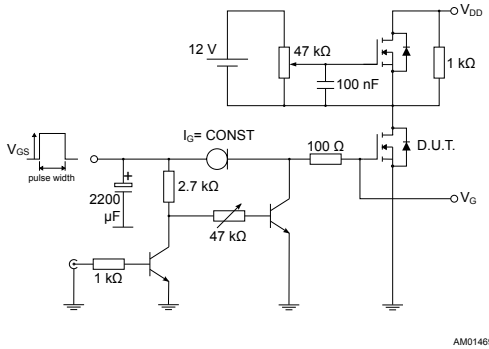


Figure 14. Test circuit for inductive load switching and diode recovery times

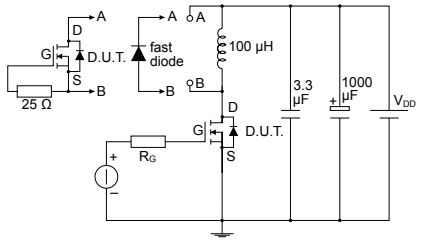


Figure 15. Unclamped inductive load test circuit

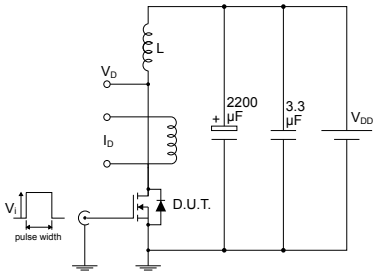


Figure 16. Unclamped inductive waveform

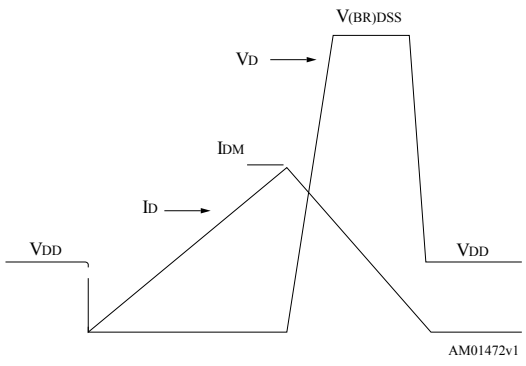
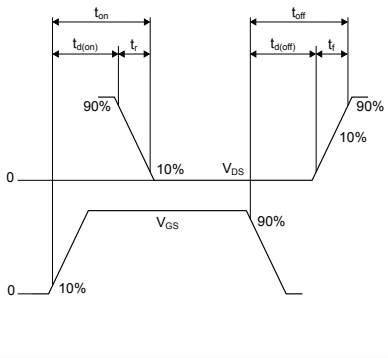


Figure 17. Switching time waveform

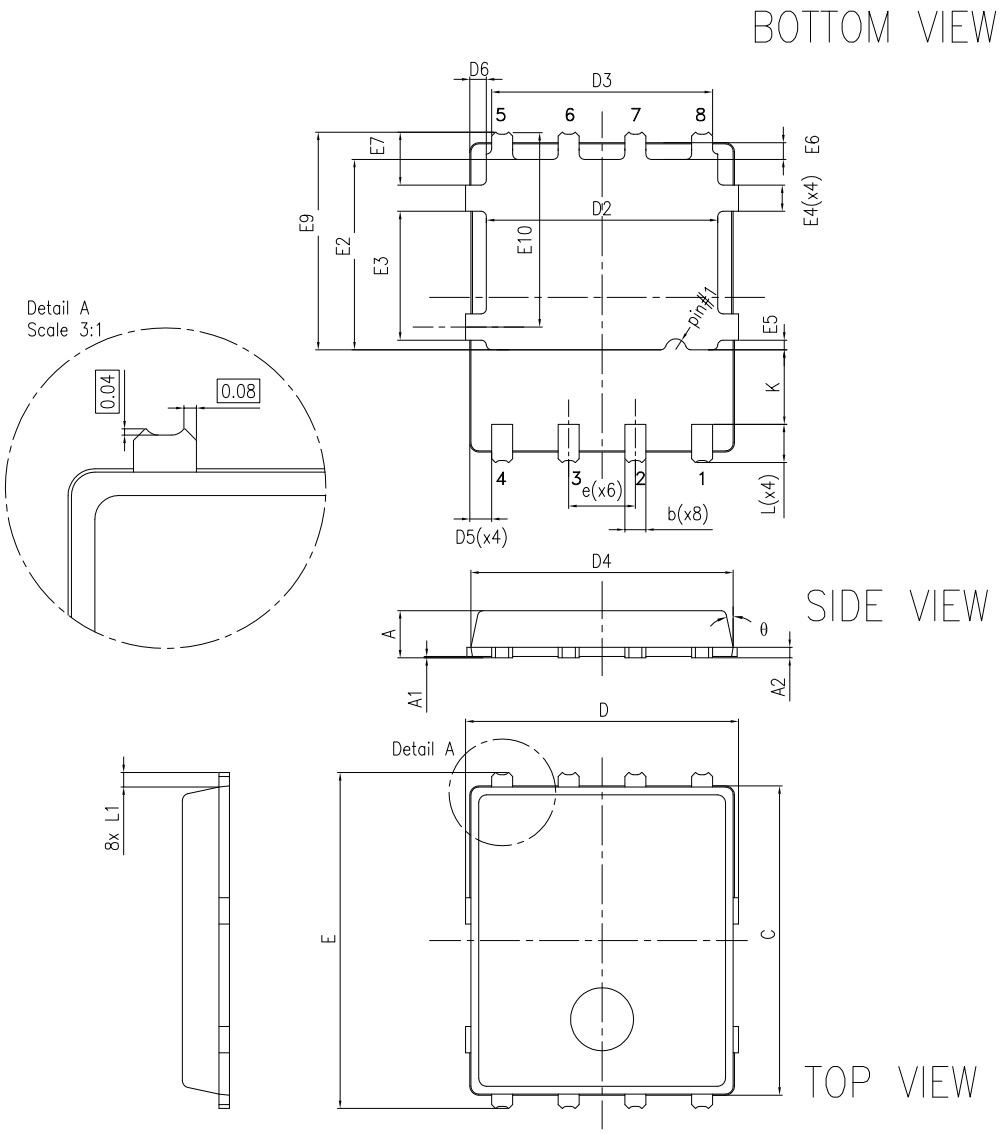


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 18. PowerFLAT™ 5x6 WF type R package outline

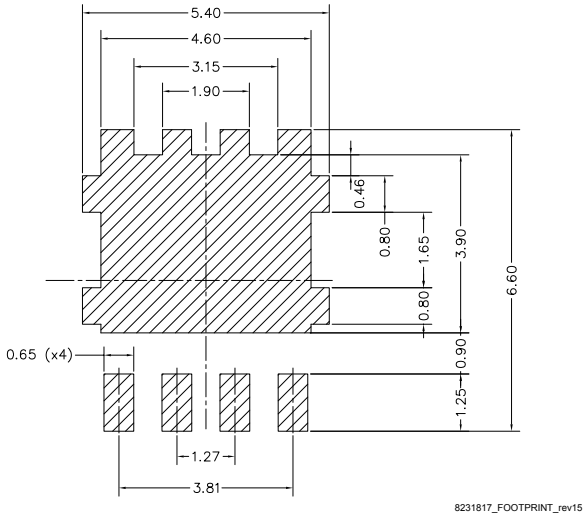


8231817_R_WF_Rev_15

Table 8. **PowerFLAT™ 5x6 WF type R mechanical data**

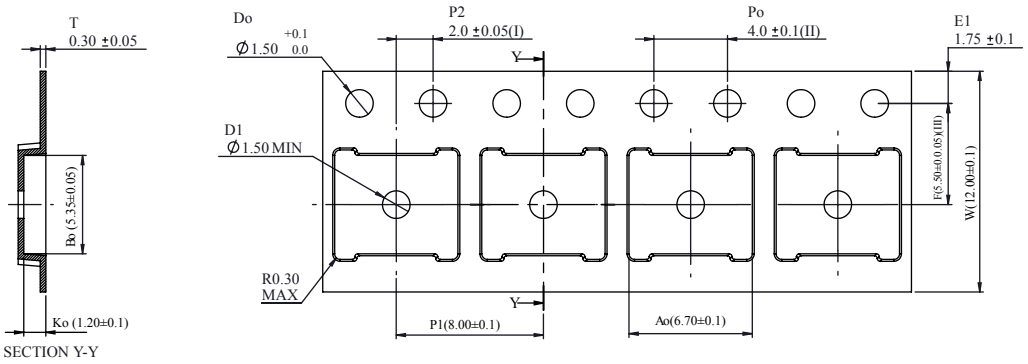
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
Θ	0°		12°

Figure 19. **PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)**



4.2 PowerFLAT™ 5x6 WF packing information

Figure 20. **PowerFLAT™ 5x6 WF tape (dimensions are in mm)**



(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.

Base and bulk qua ntity 3000 pcs

8234350_TapeWF_rev_C

Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

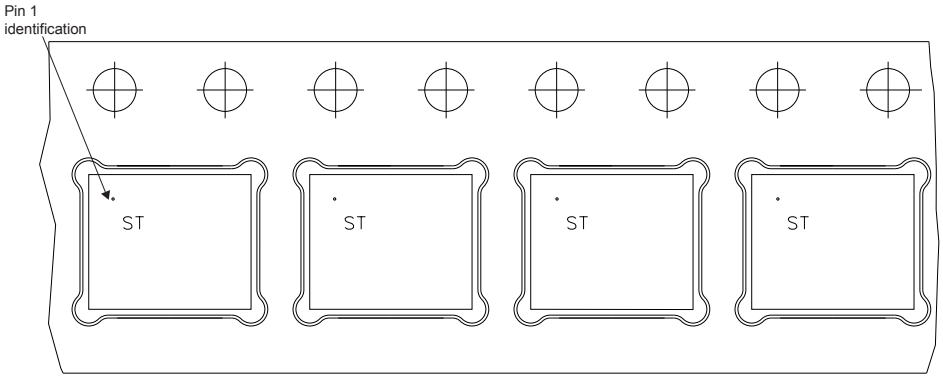
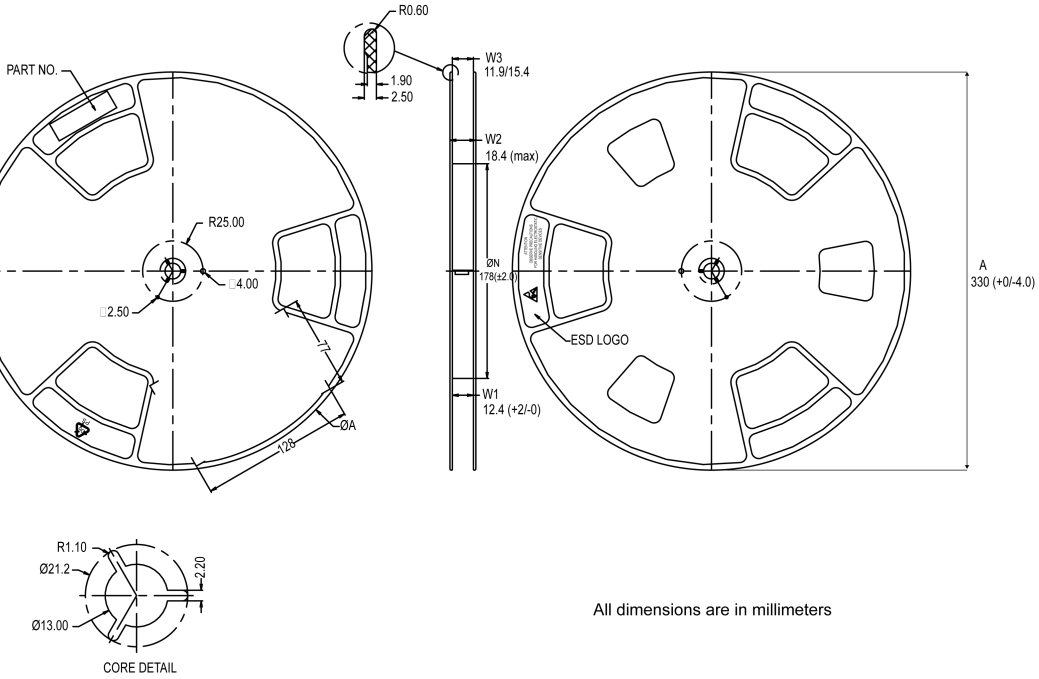


Figure 22. PowerFLAT™ 5x6 reel (dimensions are in mm)



Revision history

Table 9. **Document revision history**

Date	Version	Changes
05-Apr-2018	1	Initial release. The document status is production data.

Contents