1EDI EiceDRIVER™ Enhanced

1EDI30J12CP

Single JFET Driver IC

Preliminary Datasheet

Rev. 1.3, November 2014

Industrial Power Control

Edition 2014-11-12

Published by
Infineon Technologies AG
81726 Munich, Germany

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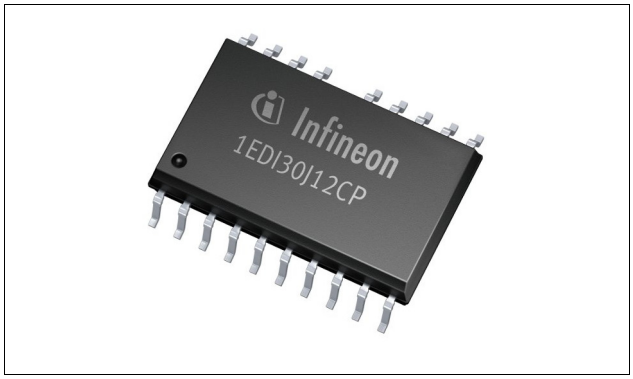
Single JFET Driver IC



Product Highlights

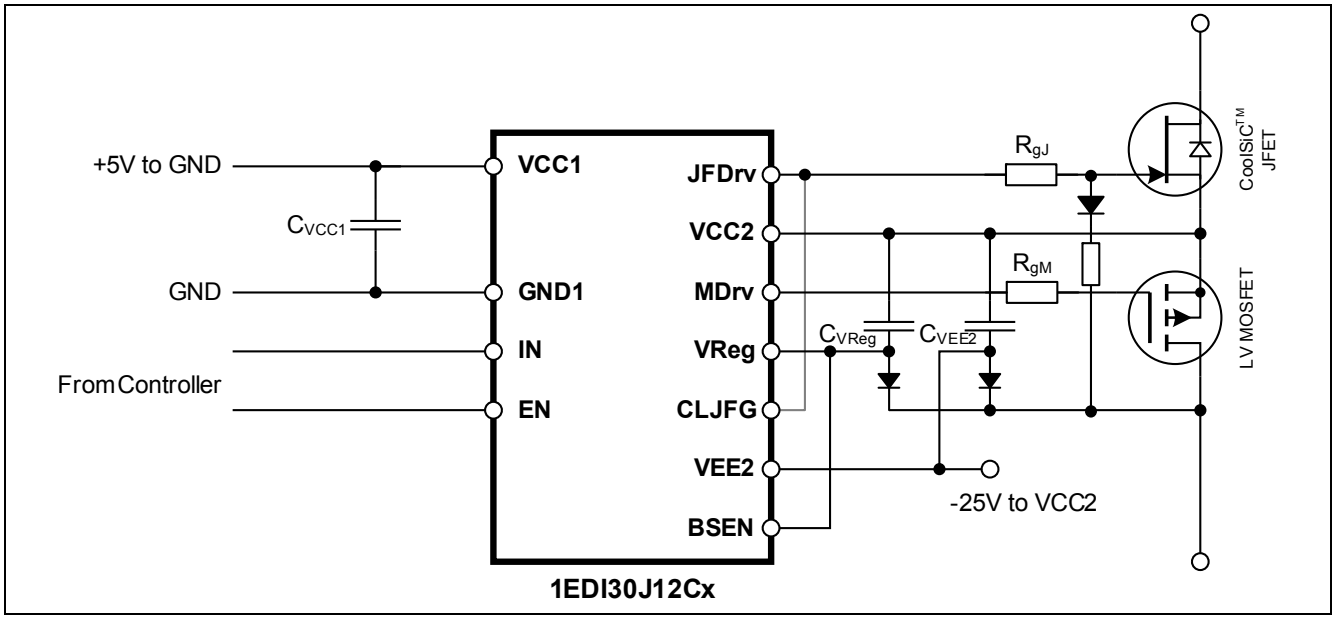
- Single driver for normally-on JFET
- Galvanic isolation
- Signal transmission via Coreless Transformer
- Supporting Direct Drive JFET Topology

Features

- Single channel isolated JFET driver
- Optimized for 1200V Infineon CoolSiC™ JFETs
- Extremely low propagation delay of typ. 80ns
- Extremly high common mode transient immunity of 100V/ns
- Minimal 3A rail-to-rail output
- Safe turn off during start up
- Supports bootstrap operation

Description

- The 1EDI30J12CP is an advanced single channel JFET gate driver. The driver is built to drive a normally-on CoolSiC™ JFET together with a low voltage P-channel MOSFET in a switching loss optimized Direct Drive JFET Topology.
- The device consists of two galvanic separated parts. The input signals are TTL level compatible with a high-voltage capability of up to 17.5V. The output chip is directly driving a CoolSiC™ JFET and MOSFET with rail to rail output stages.



Product Type	Package
1EDI30J12CP	PG-DSO-19-4

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1 Pin Configuration and Description

The pin configuration for 1EDI30J12CP in a PG-DSO-19-4 wide body package is shown in **Figure 1** and **Table 1**.

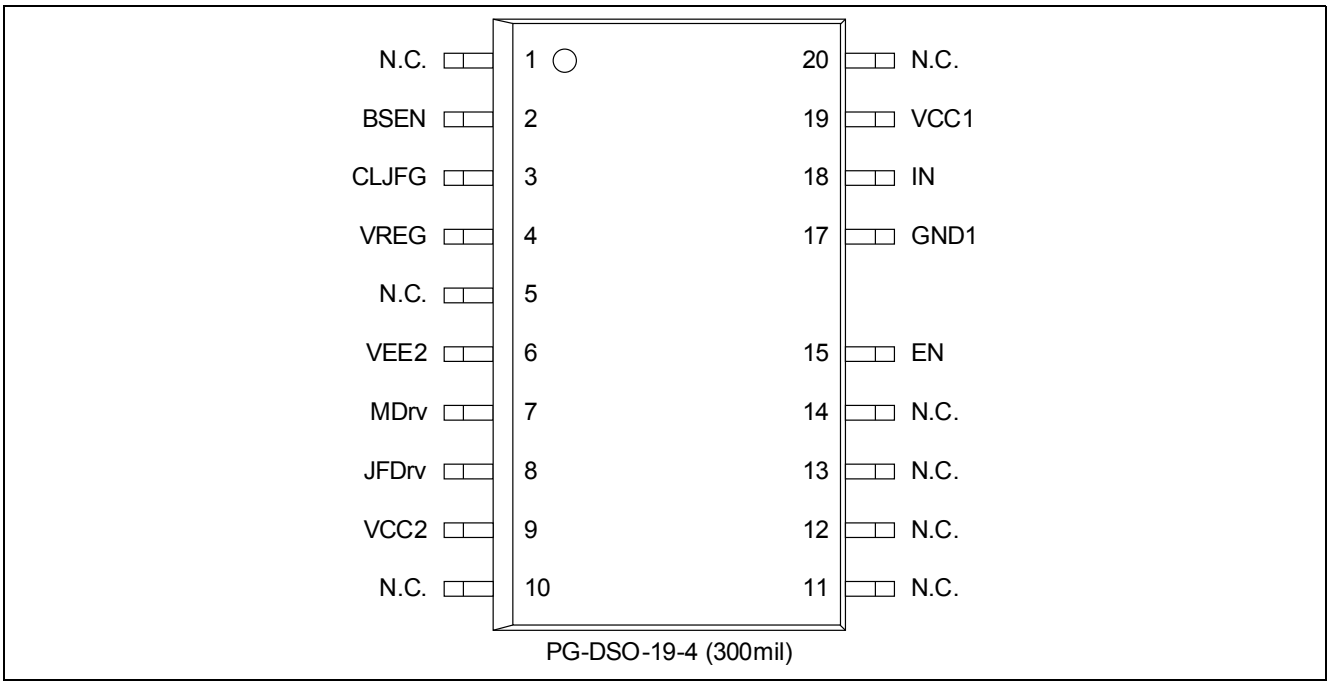


Figure 1 Pin Configuration PG-DSO-19-4

Table 1 Pin Configuration 1EDI30J12CP in PG-DSO-19-4, Wide Body

Pin	Symbol	Description
1	N.C.	Internally not connected[1)]
2	BSEN	Bootstrap Enable For bootstrap operation connect this pin to VCC2, for non bootstrap operation to VREG
3	CLJFG	Reserved[2)]
4	VREG	Voltage Regulator Output VREG is the output of the integrated linear regulator and the negative power supply for the gate drivers
5	N.C.	Internally not connected[1)]
6	VEE2	Negative Power Supply Output Side VEE2 is the input of the integrated linear regulator
7	MDrv	MOSFET Driver Output
8	JFDrv	JFET Driver Output
9	VCC2	Positive Power Supply Output Side VCC2 is the positive supply input of the JFET driver and MOSFET driver, connected to the sources of the JFET and the MOSFET
10	N.C.	Internally not connected[1)]
11	N.C.	Internally not connected[1)]
12	N.C.	Internally not connected[1)]
13	N.C.	Internally not connected[1)]
14	N.C.	Internally not connected[1)]

Table 1 Pin Configuration 1EDI30J12CP in PG-DSO-19-4, Wide Body (cont'd)

Pin	Symbol	Description
15	EN	Driver Enable
17	GND1	Signal Ground Input Side
18	IN	Driver Input
19	VCC1	Positive Supply Input Side
20	N.C.	Internally not connected[1)]

1) Pads of N.C. pins must be left unconnected, separated from each other and floating for maximum creepage/clearance distance

2) Connect to JFDrv Pin or leave pin unconnected and floating

2 Representative Block Diagram

A simplified functional block diagram is given in **Figure 2** representing the principle functionality of the driver.

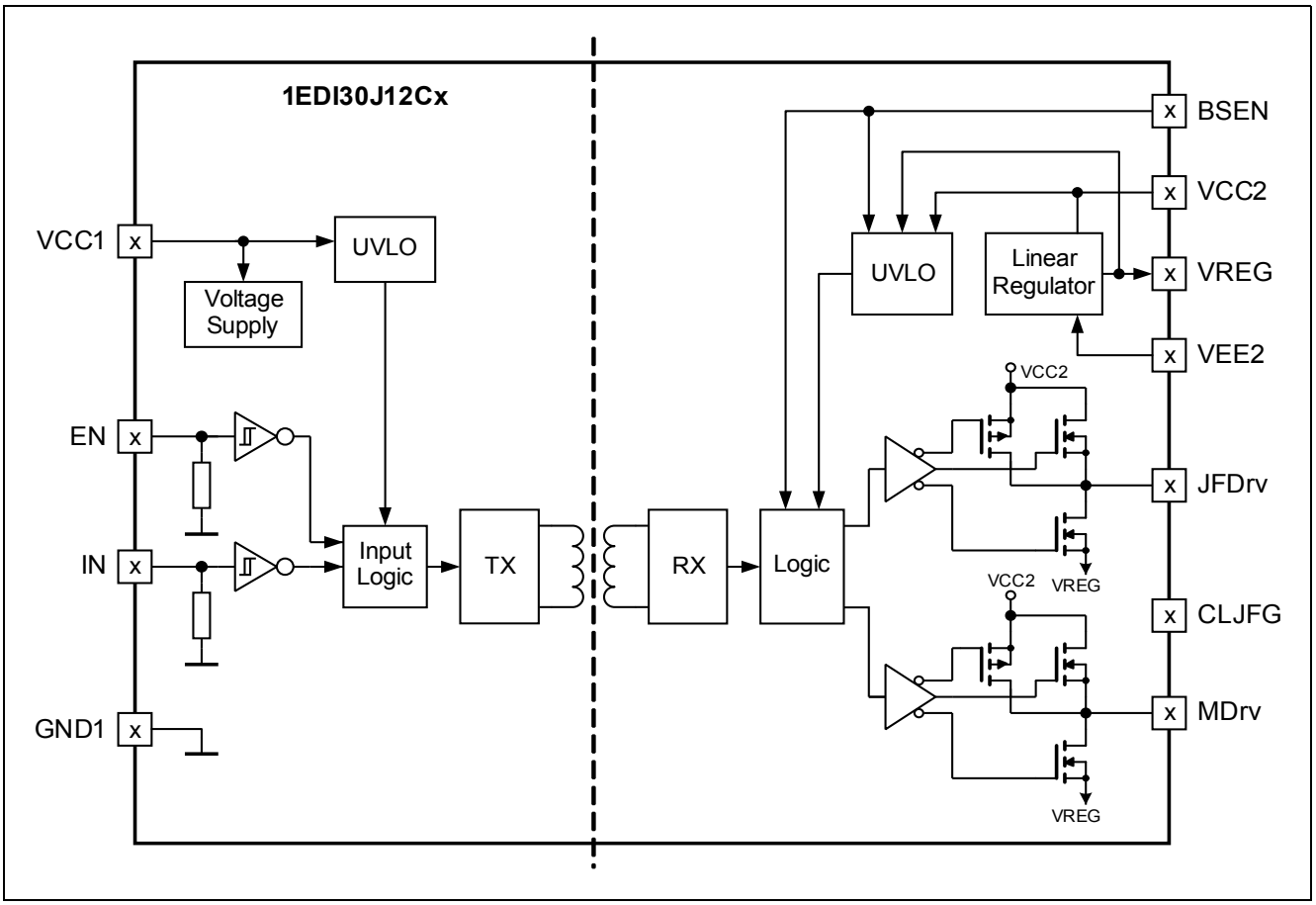


Figure 2 Representative Block Diagram

3 Functional Description

3.1 Introduction

The 1EDI30J12Cx is an advanced JFET (junction gate field-effect transistor) gate driver. The driver is built to drive a normally-on CoolSiC™ JFET together with a low voltage p-channel MOSFET in a switching loss optimized cascode operation called Direct Drive JFET Topology.

As MOSFET (metal–oxide–semiconductor field-effect transistor; referred to as pMOS, LV MOSFET) a 30 V p-channel OptiMOS™ MOSFET with low R_{DSon} is typically used (e.g. OptiMOS™ BSC030P03NS3 G).

The driver consists of two galvanic separated parts. The inputs can be connected to any controller with varying signal levels. The pins can handle signals up to 17.5V, however the thresholds remains at TTL levels.
The output side is connected to the high voltage side of the application, incorporates two rail to rail output stages. The two gate drivers, one for the JFET and one for the MOSFET, drive the gates between VCC2 and the regulated output VREG.

The 1EDI30J12Cx supports two different start up modes selectable by the bootstrap enable pin BSEN. A specialized bootstrap operation mode for supplying the driver via a bootstrap diode. And a standard operation mode for direct supply realised with a floating isolated supply source.

The output side has a built in linear voltage regulator to generate an accurate JFET driver supply voltage inside the window between pinch off voltage and punch through voltage of Infineon's CoolSiC™ JFETs . In addition, the internal regulator separates the driver supply voltage from a common supply voltage for low side switches, so all low side switches could be supplied by one negative supply. Further in isolated supply topologies it offers the support of wide supply range due to preregulation. So voltage drops due to bad transformer coupling can be handled.

Cascodes were introduced in the past for faster switching made possible by the elimination of the JFETs Cgd acting as a feedback to the control gate. The disadvantage by eliminating the feedback is that the dV/dt of the switch gets uncontrolled.

New JFET devices like CoolSiC™ JFET offers a reduced gate charge, therefore driving the JFET gate directly offers advantages in controlling the switching speed with lower EMI and less ringing.

3.2 Theory of Operation

The optimized cascode operation offered by the 1EDI30J12Cx driver called Direct Drive JFET Topology differs from the normal cascode in the way it is controlling the switch. The normal cascode controls the normally-on JFET by indirectly controlling the source potential of the JFET via the low-voltage MOSFET.

In the Direct Drive JFET Topology the MOSFET is used to keep the normally-on JFET in a safe off-state during start up of the application as in the normal cascode. When the driver auxilliary supply voltage is high enough to release the Under Voltage Lock Out (UVLO) the MOSFET is permanently turned on and the JFET is driven directly according to the input signal.

The input signal is transferred across the isolating Coreless Transformer (CLT) from input side to output side. A high at the input pin turns on the JFET. The 1EDI30J12Cx is a non inverting driver.

When the VCC1 supply voltage has reached the turn on threshold and the signal at the EN pin is high, the input side is able to send the IN signal to the output side.

Depending on the UVLO of the output side, the input signal is either ignored if $|V_{VREG}|$ is below the UVLO-on-threshold or is applied amplified at the gate of JFET.

When the VCC1 voltage potential reaches the turn off threshold, the input side sends an off signal to the output side to ensure a defined switch off state before the driver is disabled.

The driver can be disabled using the EN pin: in case the EN pin is pulled to low, the output is switched off regardless of the signal applied to the IN pin.

3.2.1 Supply options

Two different isolated supply configurations are possible depending on the reference node of the supply.

1. The external power supply is related to VCC2 (see **Figure 3** high-side switch and **Figure 10**).
   This configuration is possible for both high and low-side switches, but each driver has to be separately supplied in order to guarantee the correct start up behavior. It is not possible to share the same supply among more than one driver.
2. The external power supply is related to the MOSFET drain potential (see **Figure 3** low-side switches and **Figure 12**).
   This allows for using the same power supply to more than one driver stage as long as their MOSFET drains are connected to the same potential. Which makes this configuration most suitable to be used on drivers connected to low-side switches.

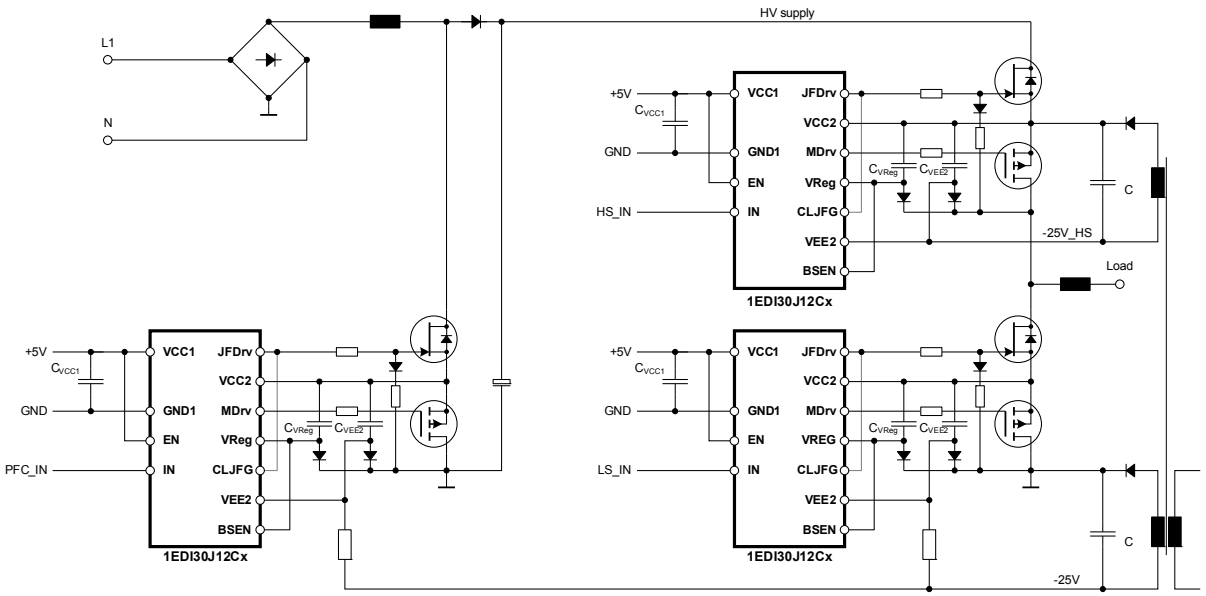


Figure 3 Application drawing for isolated supply (PFC+HB)

Additionally it is possible to supply the driver via bootstrapping. In this supply mode a high-side driverstage can share the same isolated high-side supply (see **Figure 6**). It is also possible to transfer the power from the high-side to a low-side driverstage via a bootrapping capacitor (see **Figure 13**). Further information about the bootstapping supply can be found in **Chapter 3.2.4**.

3.2.2 Normal start up

This section describes a normal start up in which the auxiliary supplies of the driver are enabled before a voltage is applied over the switch (JFET drain to pMOS drain). The timing diagram of this start up is shown in **Figure 4**.

The negative driver supply voltage is applied to VEE2. VREG is following the supply voltage ramp with the regulator drop of approximately 2V, depending on the capacitor size and the ramping speed of VEE2. When VREG reaches the UVLO threshold the driver is turning on the p-channel MOSFET. After MDrv has reached the on-threshold the JFET gate driver stage is active and follows the IN signals with a short propagation delay of typical 80ns.

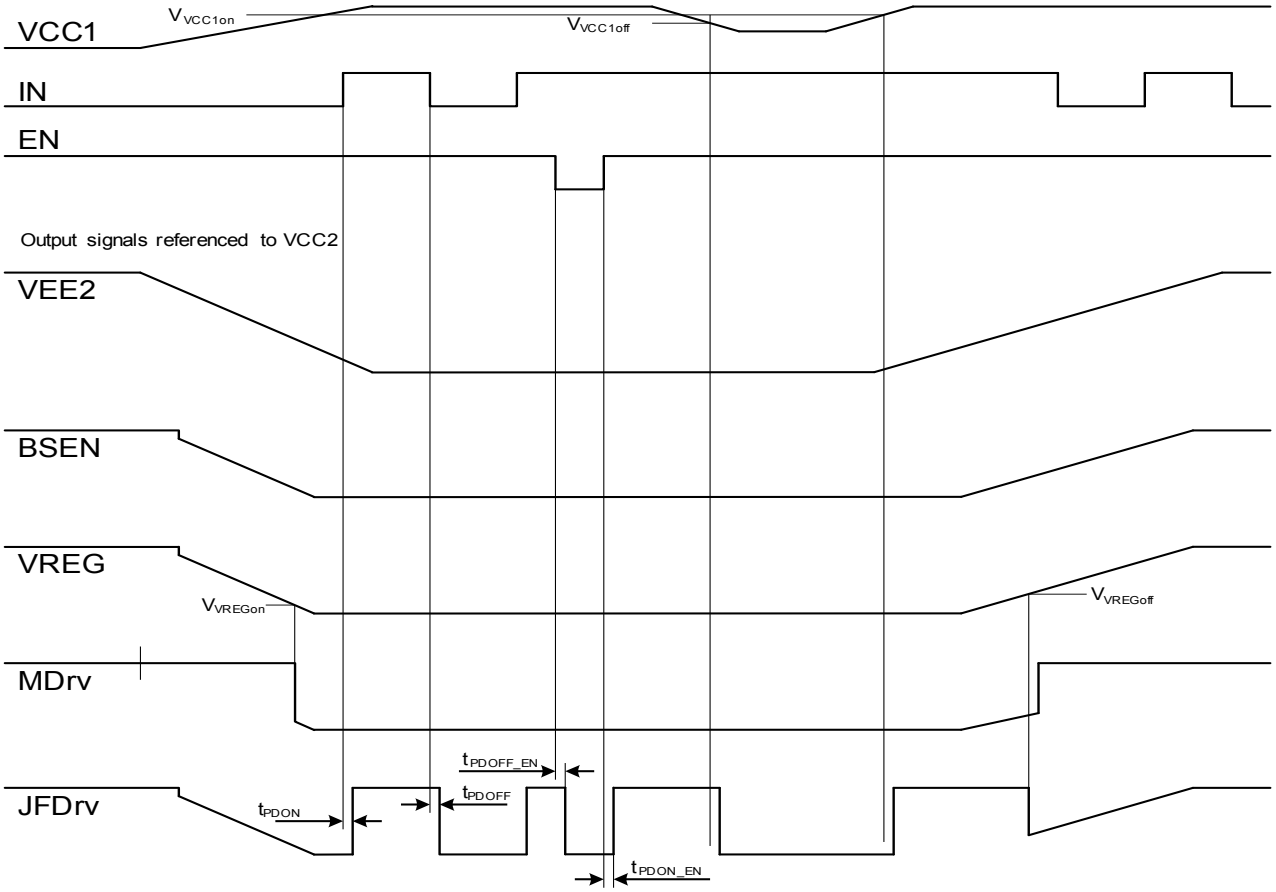


Figure 4 **Principle start up, auxiliary supplies present before a voltage is applied over the switch** (Signal names are chosen equivalent to the pin names of the driver)

3.2.3 Reverse start up with self-pinch-off

One of the biggest questions that arise when dealing with normally-on devices is the situation that comes up when the auxiliary power supply fails or is not ready at the point when the high voltage is applied over the switch.

This event is depicted in **Figure 5**. Due to the normally-on behavior of the JFET and the cascoded normally-off MOSFET, the voltage is being blocked at the MOSFET. The Vds voltage that is building up over the switched-off MOSFET is being mirrored to the JFET Vgs voltage via the diode connecting the MOSFET drain to the JFET gate (see **Chapter 6.2**) until the level reaches the JFET pinch off voltage and the JFET itself blocks the voltage.

When the JFET is pinched off a small current is still flowing through the JFET charging the capacitors CVEE2 and CVReg which supply the driver. In this way the JFET acts as a linear regulator powering the output stages of the driver at the pinch off voltage.

As soon as the auxiliary supply is larger than the pinch off voltage the auxiliary supply is charging VEE2. As it reaches the under voltage lockout level, the JFET is kept off and the MOSFET is turned on. From this point onwards the driver is transmitting the IN signal to the JFET gate.

This behavior of acting in a self-regulating manner enables the driver to also work in a bootstrapping scheme.

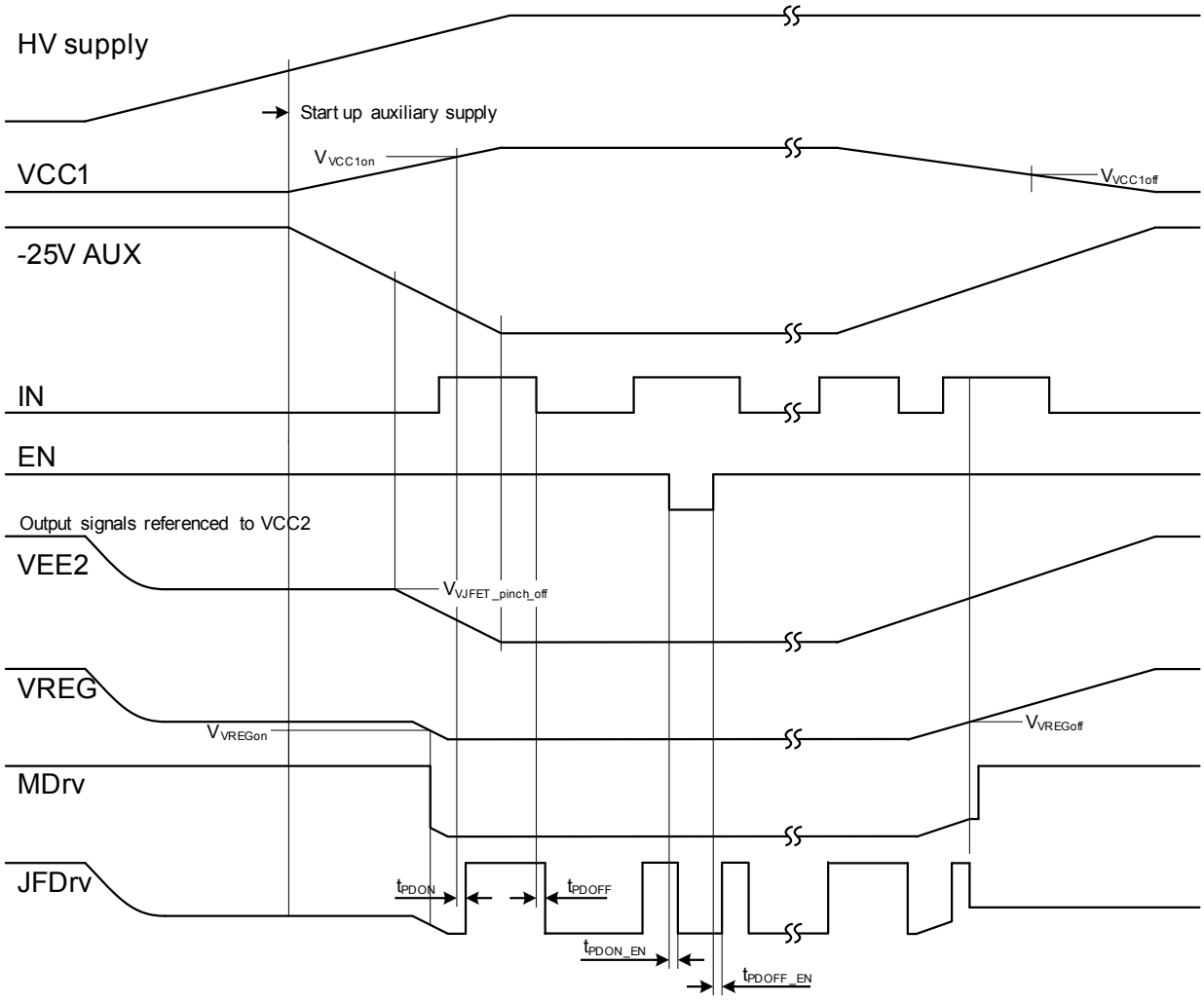


Figure 5 **Principle start up with the auxiliary supplies not present when voltage is applied over the switch** (Signal names are chosen equivalent to the pin names of the driver)

3.2.4 Bootstrap supply mode and start up

In bootstrap supply mode, the capacitors at VEE2 and VREG are charged to the pinch off voltage of the JFET as described in **Chapter 3.2.3** (Infineon CoolSiC™ JFET family has the lowest gate threshold voltage at -12 V). When the BSEN pin is connected to VCC2 the bootstrap supply mode is active. In this case a lower UVLO threshold is used and the driver is active at approximately -9.0 V.

After passing this lower UVLO threshold the driver is ready to receive IN signals from the input stage. This input signal is transferred to a switching logic which turns on the p-channel MOSFET. After the V_{MDrv} has passed the MOSFET gate turn on threshold the JFET is turned on. The voltage drop across the MOSFET and JFET channel is nearly zero. The potential of VCC2 is identical to JFET drain voltage. A negative supply related to the JFET drain (positive potential of DC-link capacitor, half bridge supply) can charge the input capacitor C_{VEE2} through a high voltage bootstrap diode. An example of a high-side bootstrap supply can be seen in **Figure 6**.

If the input stage is sending a low to the driving stage, first the JFET is turned off. After the JFDrv has passed the off threshold the MOSFET is turned off.

The propagation delay in bootstrap mode is therefore enlarged by the MOSFET gate charging time. After VREG has passed the higher normal UVLO level, the MOSFET is permanently kept on and the delay changes to the fast

datasheet values of typical 80ns. A timing diagram showing the various signals in this startup mode is depicted in **Figure 7**. **Figure 8** shows a diagram detailing the reason for the prolonged popagation delay.

The longer propagation delay can be indicated to the input side by using an optocoupler. The optocoupler diode is inserted between BSEN and VCC2. During the start up phase in bootstrap mode BSEN is applying an output current of at least 2 mA while IN is high.

During the bootstrap start up phase the power dissipation in the driver is increased. Therefore, the controller has to make sure that the driver does not remain in bootstrap start up mode for longer periods of time in order not to overheat the driver.

During the boostrap start-up phase, the propagation delay is larger and the effective JFET conduction time shorter compared to standard operating mode. This means, the controller has to take care to compensate for the longer propagation delays and shorter on-times, e.g. in a half-bridge configuration, the dead-times have to be increased. After the start-up phase is finished, the controller has to reduce the dead-times to normal operating values, not to risk body-diode conduction over long periods of time, which can lead to higher power dissipation of the JFETs.

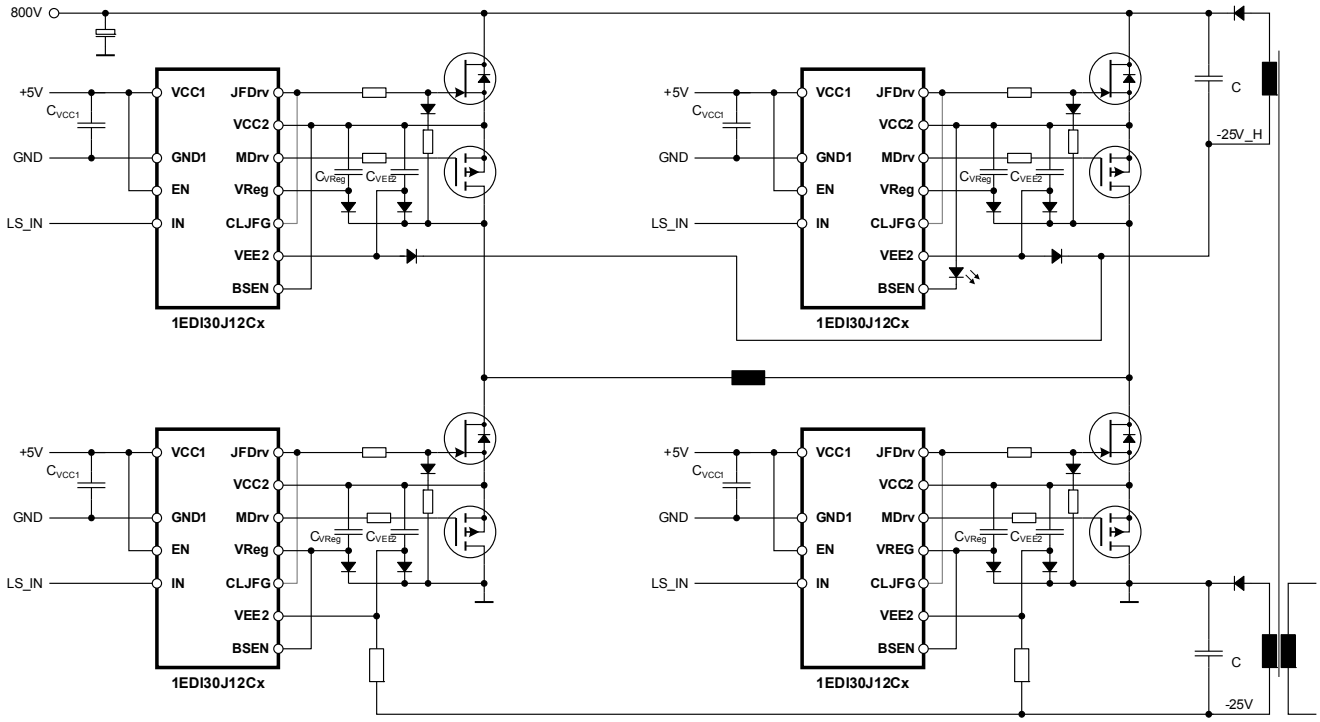


Figure 6 Application drawing for high side bootstrap supply (FB)

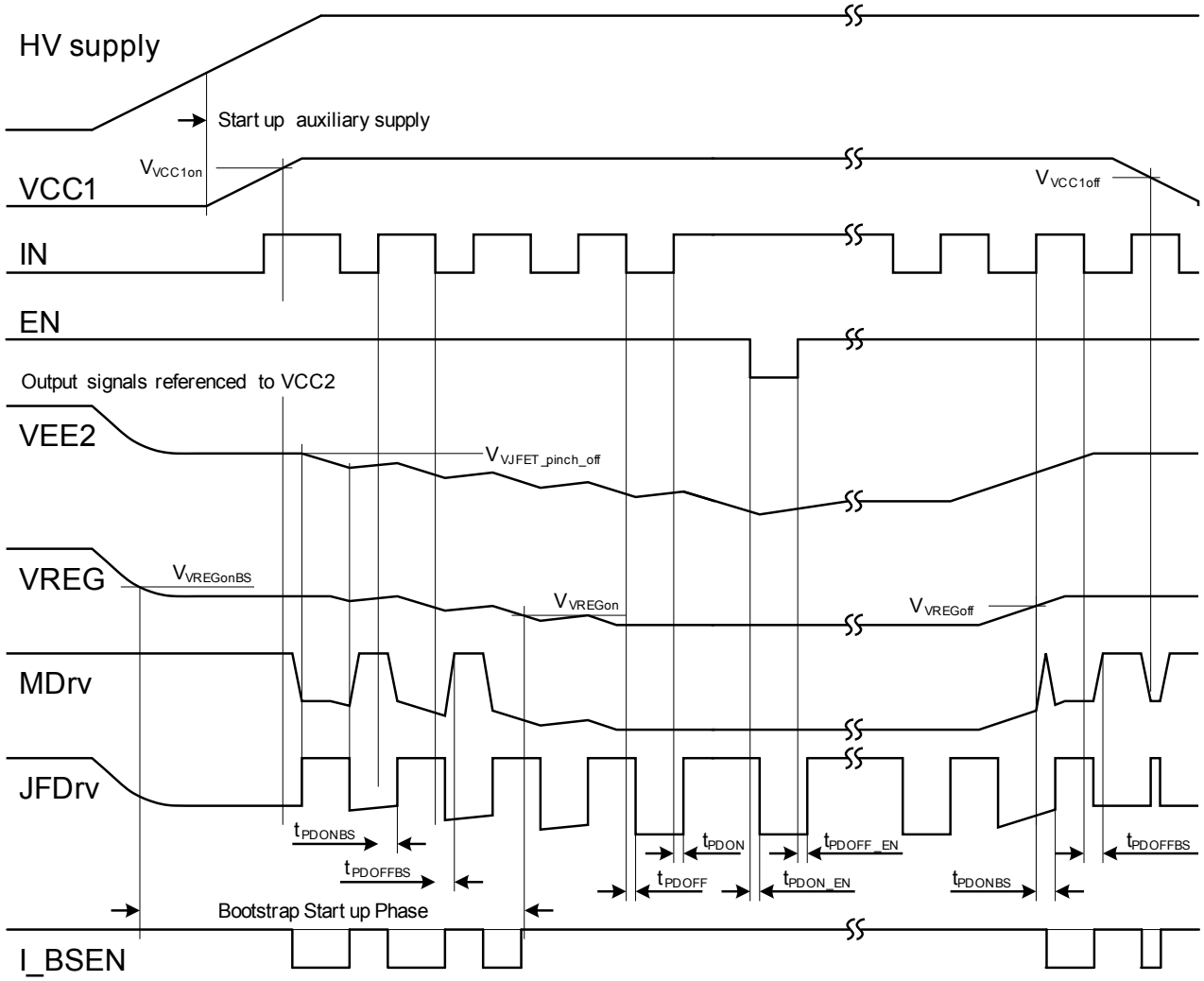


Figure 7 **Start up bootstrap supply mode for high side located cascodes (BSEN connected to VCC2)**
(Signal names are chosen equivalent to the pin names of the driver)

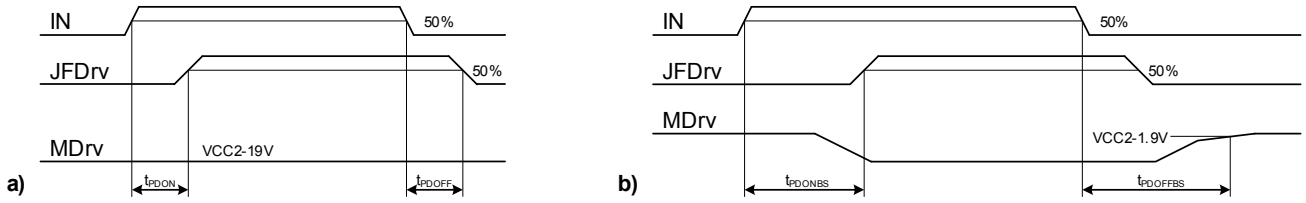


Figure 8 **Timing of IN to JFDrv, a) normal mode, b) bootstrap mode**

3.3 Protection Features

3.3.1 Active Shut Down

The Active Shut Down feature ensures MOSFET off-state under all circumstances even if the output side supply is inactive. The p-channel MOSFET gate is held actively high until V_{REG} is passing the output UVLO thresholds of the driver.

3.3.2 Interlock between MOSFET Gate and JFET Gate

The JFET can only be switched on, if the MOSFET is on, otherwise the low voltage MOSFET will be destroyed by overvoltage. To ensure proper operation of the cascode, the driver is monitoring the MOSFET gate voltage at MDrv pin and the JFET gate voltage at JFDrv pin. Only if the MOSFET is on, indicated by MDrv pin having low potential, the JFET is allowed to turn on. Similar in opposite direction, MOSFET turn off is only allowed if the JFET is in its off state.

3.3.3 Bootstrap Start up Mode Indicator

The 1EDI30J12Cx indicates at BSEN pin that the driver has entered the bootstrap start up phase with an output current of min 2mA to drive an opto coupler if IN signal is driven high.

4 Characteristics

Unless otherwise noticed, voltages of the input side signals (pins VCC1, IN, EN, GND1) are measured with respect to input ground (pin GND1), all other voltages are measured with respect to positive output supply (pin VCC2).

Currents in the following tables are defined as positive currents flowing out of the pin (unless otherwise specified).

The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Absolute maximum ratings are listed in **Table 2**. Stresses above the max. values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

For the same reason make sure that any capacitors that will be connected to pins VCC1 and VCC2 are discharged before assembling the application circuit.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Positive supply voltage input side	V_{VCC1}	-0.3	18	V	
Voltage at pin IN, EN	V_{IN}	-0.3	V_{VCC1}+0.3	V	
Input to output isolating voltage	V_{ISO}	-1200	+1200	V	1)
Negative supply voltage output side (VEE2)	V_{VEE2}	-30	V_{VCC2}+0.3	V	
Voltage at pin BSEN	V_{BSEN}	V_{VREG}-0.3	V_{VCC2}+0.3	V	
Voltage at pin VREG	V_{VREG}	-21	V_{VCC2}+0.3	V	
VEE2 max dV/dt	$\|dV_{VEE2}\|$		125	V/ms	C_{VReg}= 2.2µF
Voltage at pin JFDrv	V_{JFDrv}	V_{VREG}-0.3	V_{VCC2}+0.3	V	
Voltage at pin MDrv	V_{MDrv}	V_{VREG}-0.3	V_{VCC2}+0.3	V	
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_S	-55	150	°C	2)3)
Maximum power dissipation	P_{TOT}		1.0	W	PG-DSO-19-4, T_A=25°C
ESD capability	V_{ESD}	—	2	kV	Human Body Model4)

1) With reference to GND1

2) Prolonged storage at high temperatures reduces the lifetime of the product

3) Tested according to EIA/JESD22-A103D

4) According to EIA/JESD22-A114-B (discharging at 100pF Capacitor through 1.5kΩ Resistor)

4.2 Thermal Characteristics

Table 3 Thermal Characteristics

Parameter	Symbol	Values	Unit	Remarks
		Typ.		
Thermal resistance Junction-Ambient	R_{thJA25}	85	K/W	PG-DSO-19-4, T_A=25°C; Layout: **Figure 16**

4.3 Operating Range

Table 4 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Positive supply voltage input side	V_{VCC1}	4.75	17.5	V	
Logic input voltage input side (IN, EN)	V_{IN}	0	V_{VCC1}	V	
Negative supply voltage output side (VEE2)	V_{VEE2}	-28	-22	V	VREG in regulation, full PSRR
Negative supply voltage output side (VEE2)	V_{VEE2}	-28	-19	V	$V_{VREG} > V_{VREGoff}$ [1]
Output capacitance for VREG	C_{VREG}	0.22	2.2	µF	from VREG to VCC2[1], ESR_{CVREG} < 15mOhm
Common mode transient immunity	$\|dV_{ISO}/dt\|$	—	100	V/ns	[1]
Junction temperature	T_J	-40	150	°C	[1][2]

1) The parameter is not subject to production test - verified by design/characterization

2) According to product qualification conditions (tested according to EIA/JESD22-A108D)

4.4 Electrical Characteristics

The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from -40°C to 150°C. Typical values represent the nominal values related to T_J=25°C. Unless otherwise noticed, voltages of the input side signals (pins VCC1, IN, EN, GND1) are measured with respect to input ground (pin GND1) all other voltages are measured with respect to positive output supply (pin VCC2). Supply voltages are V_{VCC1} = 5 V and V_{VEE2} = -25 V if not otherwise mentioned.

The following characteristics are specified

- Power Supply (**Table 5**)
- Logic Input (**Table 6**)
- JFET Driver (**Table 7**)
- MOSFET Driver (**Table 8**)
- Dynamic Characteristics (**Table 9**)

Table 5 Power Supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC1 quiescent current	$I_{VCC1qu1}$	—	430	650	µA	IN = statically low, EN = statically high
VCC1 quiescent current	$I_{VCC1qu2}$	120	240	500	µA	EN = statically low
VCC1 supply current	$I_{VCC1supp}$	—	1.2	1.6	mA	IN = 1MHz
VCC1 turn on threshold	V_{VCC1on}	4.15	4.55	4.75	V	
VCC1 turn off threshold	$V_{VCC1off}$	3.9	4.25	4.55	V	
VCC1 turn on/off hysteresis	$V_{VCC1hys}$	0.15			V	
VEE2 quiescent current 1	$I_{VEE2qu1}$	—	380	500	µA	output chip off due to UVLO
VEE2 quiescent current 2	$I_{VEE2qu2}$	—	800	1100	µA	IN = low, output chip on
VREG output voltage[1)2)]	V_{VREG0}	-19.5	-18.85	-18.1	V	1µF from VREG to VCC2, V_{VEE2}< -22V, Load 0mA
VREG output voltage loaded[1)2)]	V_{VREG50}	-19.0	-18.25	-17.5	V	1µF from VREG to VCC2, V_{VEE2}< -22V, Load 50mA
VREG turn on threshold[1)3)]	V_{VREGon}	-17.4	-16.9	-16.4	V	
VREG turn off threshold[1)3)]	$V_{VREGoff}$	-17.0	-16.4	-16.0	V	
VREG turn on/off hysteresis[1)3)]	$V_{VREGhys}$		0.5		V	
VREG turn on threshold BS[1)3)]	$V_{VREGonBS}$	-9.8	-9.5	-9.0	V	V_{BSEN} > -3V[1)]
VREG turn off threshold BS[1)3)]	$V_{VREGoffBS}$	-9.2	-8.8	-8.3	V	V_{BSEN} > -3V[1)]
VREG turn on/off hysteresis BS[1)3)]	$V_{VREGhysBS}$		0.7		V	V_{BSEN} > -3V[1)]
VREG load current	I_{VREG}			50	mA	including loads from MDrv and JFDrv

1) Voltage refer to VCC2
2) DC voltage
3) ULVO threshold output chip

Table 6 Logic Input

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
IN, EN low input voltage	V_{INL}			1.0	V	
IN, EN high input voltage	V_{INH}	2.0			V	
IN, EN input current	I_{IN}		30	400	µA	$V_{IN}=V_{VCC1}$
BSEN low input voltage	V_{BSENL}			V_{VREG} + 2.0	V	
BSEN high input voltage	V_{BSENH}	V_{VREG} + 3.0			V	
BSEN output current	I_{BSEN}		-3.5	-2	mA	$V_{BSEN} > V_{VREG}$ + 5.7V, V_{IN} = high, $V_{VREGon} < V_{VREG} < V_{VREGonBS}$
BSEN output current	I_{BSENPD}	-70	-38	-15	µA	V_{IN}= low

Table 7 JFET Driver (Reference is VCC2)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High Level Output Voltage	V_{JFDrvH}	-2.0	-1.75		V	I_{JFDrv}=200mA;
		-4.0	-3.5		V	I_{JFDrv}=2A;
		—	-4.1		V	I_{JFDrv}=3A[1)]
High Level Output Peak Current	I_{JFDrvH}	3.0	4.0		A	[1)]
Output Voltage at low state	V_{JFDrvL}		V_{VREG} + 0.17	V_{VREG} + 0.35	V	I_{JFDrv}=-200mA;
			V_{VREG} + 1.9	V_{VREG} + 4.0	V	I_{JFDrv}=-2A;
		—	3.0		V	I_{JFDrv}=-3A[1)]
Low Level Output Peak Current	I_{JFDrvL}	-3.0	-4.0		A	[1)]
Rise Time JFDrv	t_{JFDrvR}	—	23	30	ns	C_{LOADJ}= 4.7 nF, VL=20% to VH 80%
Fall Time JFDrv	t_{JFDrvF}	—	22	35	ns	

1) The parameter is not subject to production test - verified by design/characterisation

Table 8 MOSFET Driver (Reference is VCC2)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High Level Output Voltage	V_{MDrvH}	-1.75	-1.35		V	I_{MDrv}=150mA
		-4.0	-3.15		V	I_{MDrv}=1.5A

Table 8 MOSFET Driver (Reference is VCC2) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
High Level Output Peak Current	I_{MDrvH}	2	3		A	1)
Output Voltage at Low State	V_{MDrvL}		V_{VREG} +0.26	V_{VREG} +0.55	V	I_{MDrv}=-150mA
			V_{VREG} +1.0	V_{VREG} -2.1	V	I_{MDrv}=-0.5A
			2.0	—	V	I_{MDrv}=-1.0A 1)
Low Level Output Peak Current	I_{MDrvL}		-2	-1	A	1)
Rise Time MDrv	t_{MDrvR}		65	110	ns	V_{VREG}=19V, C_{LOADM}= 22 nF, VL 20% to VH 80%
Fall Time MDrv	t_{MDrvF}		165	270	ns	

1) The parameter is not subject to production test - verified by design/characterisation

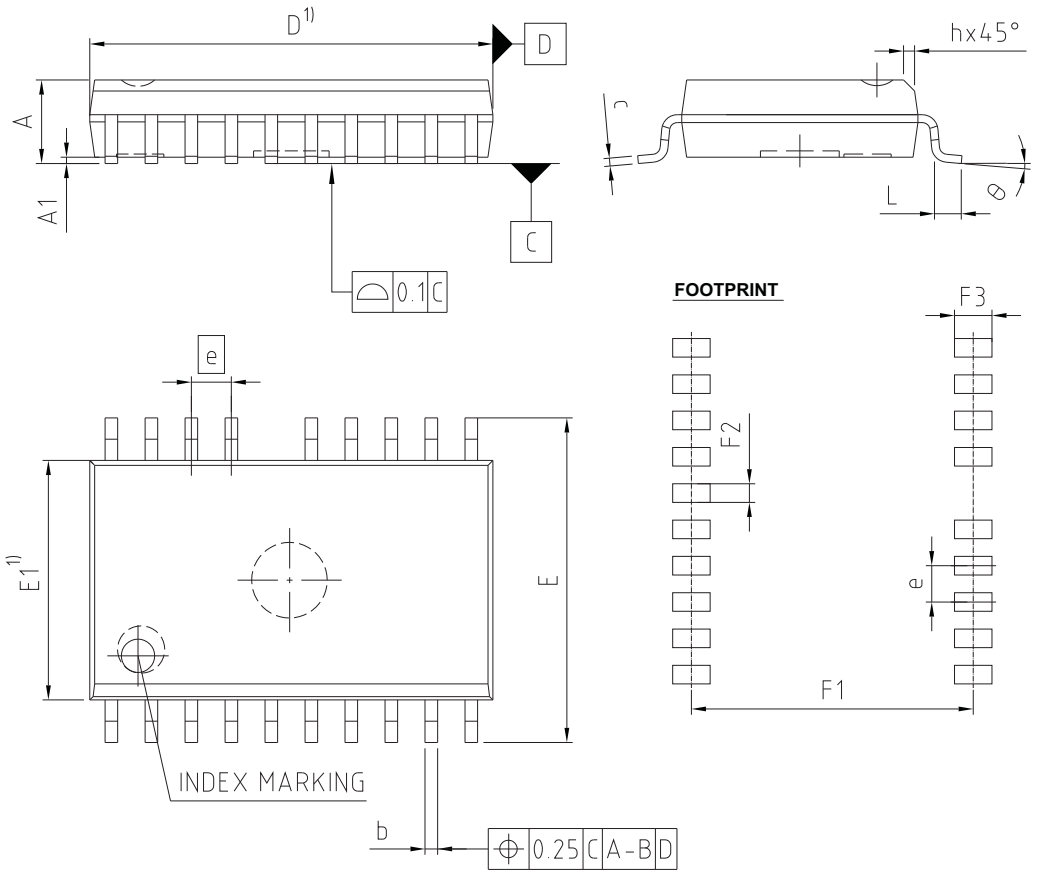
Table 9 Dynamic Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input to output propagation delay ON (IN: L to H)	t_{PDON}	53	80	106	ns	V_{VCC1}=5V, C_{LOADJ}= 100 pF, V_{IN}=50%, V_{JFDrv}=50%, V_{EN}=H T_J=25°C
Input to output propagation delay OFF (IN: H to L)	t_{PDOFF}	53	80	106	ns	
Enable to output propagation delay ON (EN: L to H)	t_{PDON_EN}	170	290	390	ns	V_{VCC1}=5V, C_{LOADJ}= 100 pF, V_{EN}=50%, V_{JFDrv}=50%, V_{IN}=H
Enable to output propagation delay OFF (IN: H to L)	t_{PDOFF_EN}	60	110	140	ns	
Input to output propagation delay distortion t_{PDON}-t_{PDOFF}	$t_{PDDISTO}$	-4.0		12	ns	V_{VCC1}=5V, C_{LOADJ}= 100 pF, V_{IN}=50%, V_{JFDrv}=50%, V_{EN}=H
Input to output propagation delay distortion due to temp	$t_{PDDISTOT}$	-20		20	ns	1)
Input to output propagation delay ON bootstrap mode 2)	t_{PDONBS}			300	ns	V_{VREG}=-19V, V_{VCC1}=5V, C_{LOADJ}= 100 pF, C_{LOADM}=22nF, V_{IN}=50%, V_{JFDrv}=50%
Input to output propagation delay OFF bootstrap mode 2)	$t_{PDOFFBS}$			300	ns	V_{VREG}=-19V, V_{VCC1}=5V, C_{LOADJ}= 100 pF, C_{LOADM}=22nF, V_{IN}=50%, V_{MDRV}=-1.9V
IN input pulse surpression	T_{MININ}	29	40	68	ns	
Switching frequency	f_{SW}			2	MHz	V_{VCC1}=5V

1) The parameter is not subject to production test - verified by design/characterisation

2) See **Figure 8**

5 Outline Dimensions



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	2.65	-	0.104
A1	0.10	0.30	0.004	0.012
b	0.30	0.51	0.012	0.020
c	0.23	0.32	0.009	0.013
D	12.60	13.00	0.496	0.512
E	10.00	10.65	0.394	0.419
E1	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
N	19		19	
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.030
T	0°	8°	0°	8°
F1	9.73		0.383	
F2	0.65		0.026	
F3	1.67		0.066	

DOCUMENT NO.
Z8B00160774

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
19.04.2011

REVISION
02

Figure 9 PG-DSO-19-4

Notes

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/cms/en/product/technology/packages/**.*

6 Application Hints

This chapter gives some hints on how the auxiliary supplies can be set up to supply the driver.

6.1 Driver Supply Set up

Figure 10 shows the standard topology where the auxiliary supply is connected between VCC2 and VEE2. In this case the internal regulator is used to create the -19 V VReg supply.

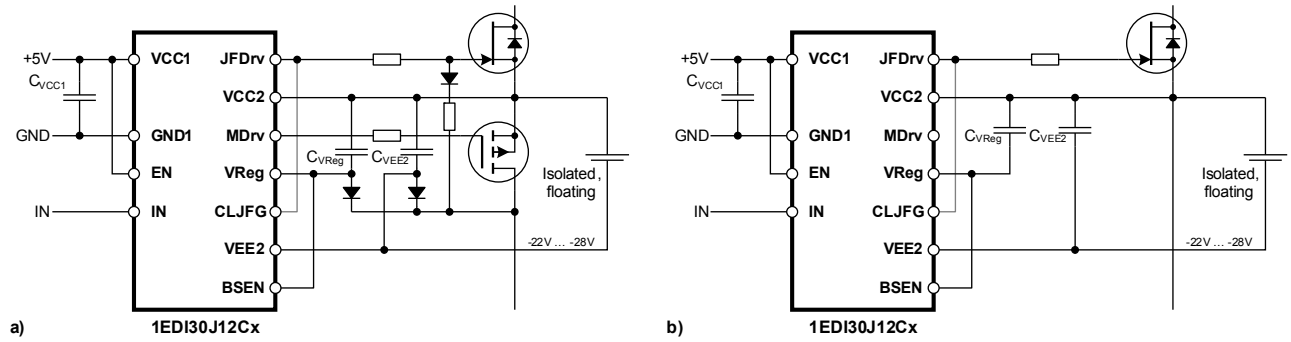


Figure 10 Isolated and floating supply, a) cascode configuration, b) only JFET

It is also possible to supply the driver with -19 V directly. In this case (shown in **Figure 11**) the pins VReg and VEE2 are shorted and CVEE2 as well as the corresponding diode are not needed. It has to be made sure that the -19 V supply is accurate within +/- 5 %.

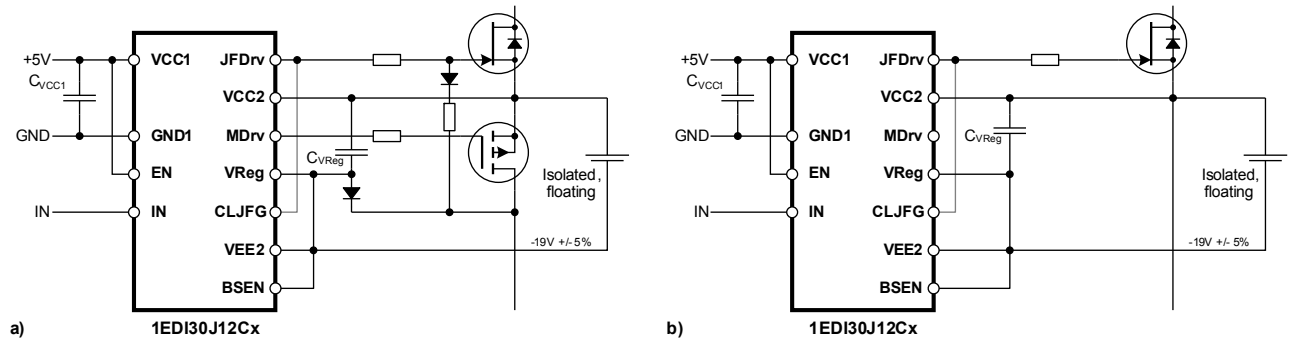


Figure 11 Isolated and floating direct supply, a) cascode configuration, b) only JFET

The third option of connecting the auxiliary supply is to connect it between the MOSFET drain and VEE2 (**Figure 12**). Since the auxiliary power supply is not connected to the reference node of the driver stage (VCC2) an additional 10 Ω resistor is needed between the power supply and the VEE2 pin. This resistor limits the current coming from the supply when current is switched through the MOSFET. When a current is switched through the MOSFET a voltage is induced in the parasitic inductances of the MOSFET which leads to a voltage difference between the reference node of the driver and the supply reference node. As in the first described method the internal regulator is active and supplies the driver stages with the needed -19 V.

When using this power supply option for switches which MOSFET drains are connected to the same node and potential one power supply can be used to power two or more driver stages. The best example are the low side switches in a H-bridge (see **Figure 6** and **Figure 14**).

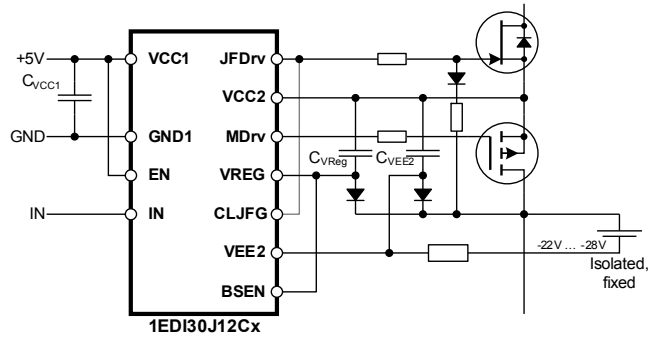


Figure 12 MOSFET drain related supply

An alternative method of supplying the low-side driver is via a bootstrapping scheme from the high-side supply (shown in **Figure 13**). This cascaded bootstrap supply transfers the needed energy via a bootstrapping capacitor (C_{BS}) to the low-side.

Additional information on how to activate the bootstrap mode can be found in **Chapter 3.2.4 Bootstrap supply mode and start up**.

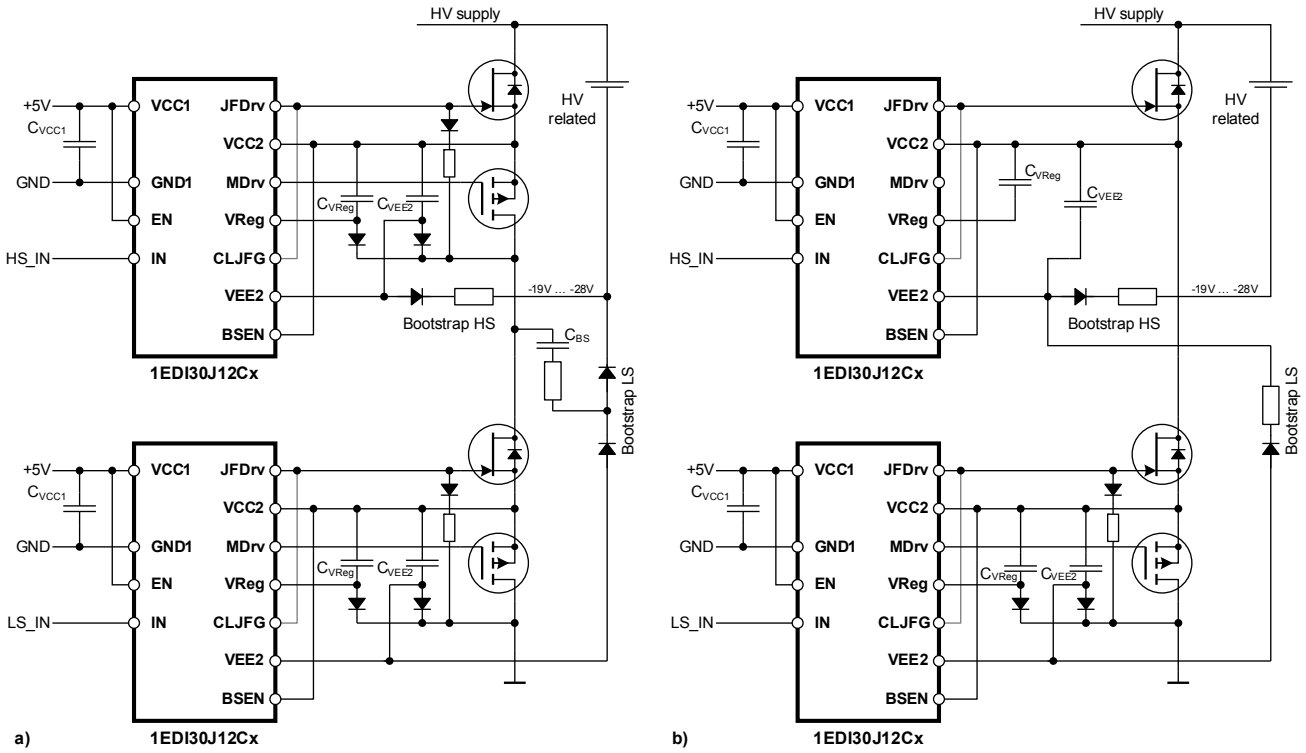


Figure 13 Cascaded bootstrap supply, a) cascode configuration, b) only JFET

In case a normally off behavior is not needed or desired the JFET can be used without the cascoded MOSFET. Topologies depicting a normally on circuit are shown in **Figure 10** b), **Figure 11** b) and **Figure 13** b).

In these cases a short circuit in a failure event cannot be prevented due to the fact that every safety aspect of the Direct Drive JFET Topology is deactivated.

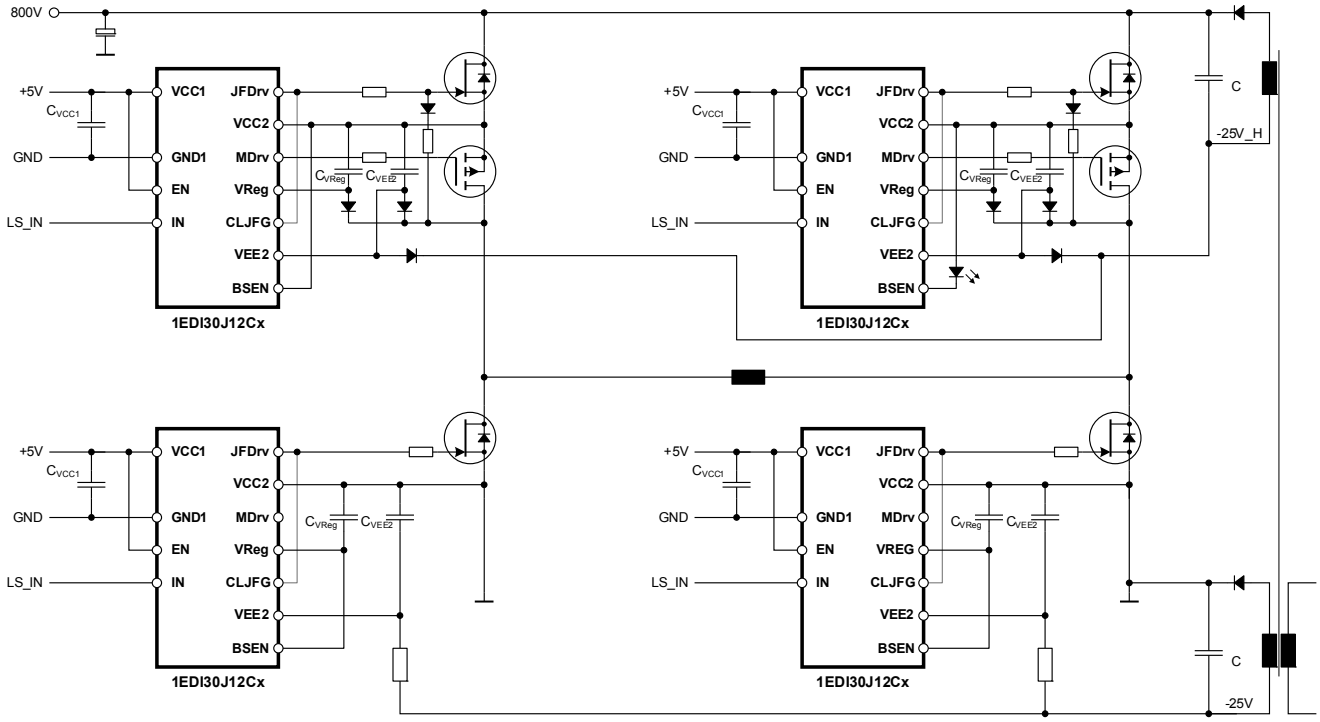


Figure 14 Application drawing for high side bootstrap supply (FB), low-side normally-on (refer to Figure 6 for low-side normally-off variant)

Figure 14 shows a full bridge with a normally-on low-side configuration. The high-side stages are powered with bootstrapping while the low-side stages are powered with an isolated and fixed supply that is GND related. The corresponding normally-off variant can be seen in Figure 6

6.2 Gate clamping diode

The external gate clamping diode connects the JFET gate to the MOSFET drain potential. In case the auxiliary power supply of the driver is not active due to power supply failure or reverse startup this diode ensures the normally-off behavior of the circuit.

Due to the normally-on behavior of the JFET and the cascoded normally-off MOSFET, the voltage is being blocked at the MOSFET. The Vds voltage that is building up over the switched-off MOSFET is being mirrored to the JFET Vgs voltage via gate clamping diode connecting the MOSFET drain to the JFET gate until the level reaches the JFET pinch off voltage and the JFET itself blocks the voltage (see Chapter 3.2.3).

The voltage rating of the diode is mainly depenent on the parasitic inductance between JFET source and MOSFET drain times the current change over time. An Infineon BAS16 diode capable of blocking 80 V should be sufficient for most layouts.

A resistor should be placed in series with the diode to limit the current through the diode. It has to be matched to the maximum current rating of the used diode. Typically it should be around 5 times larger than the gate resistance in order not to slow down the turn-on of the JFET.

6.3 Reference Layout, Thermal Layout, Layout Guide Lines

In this chapter the reference and thermal layouts are displayed. Please contact our local sales team for additional information about placement priorities.

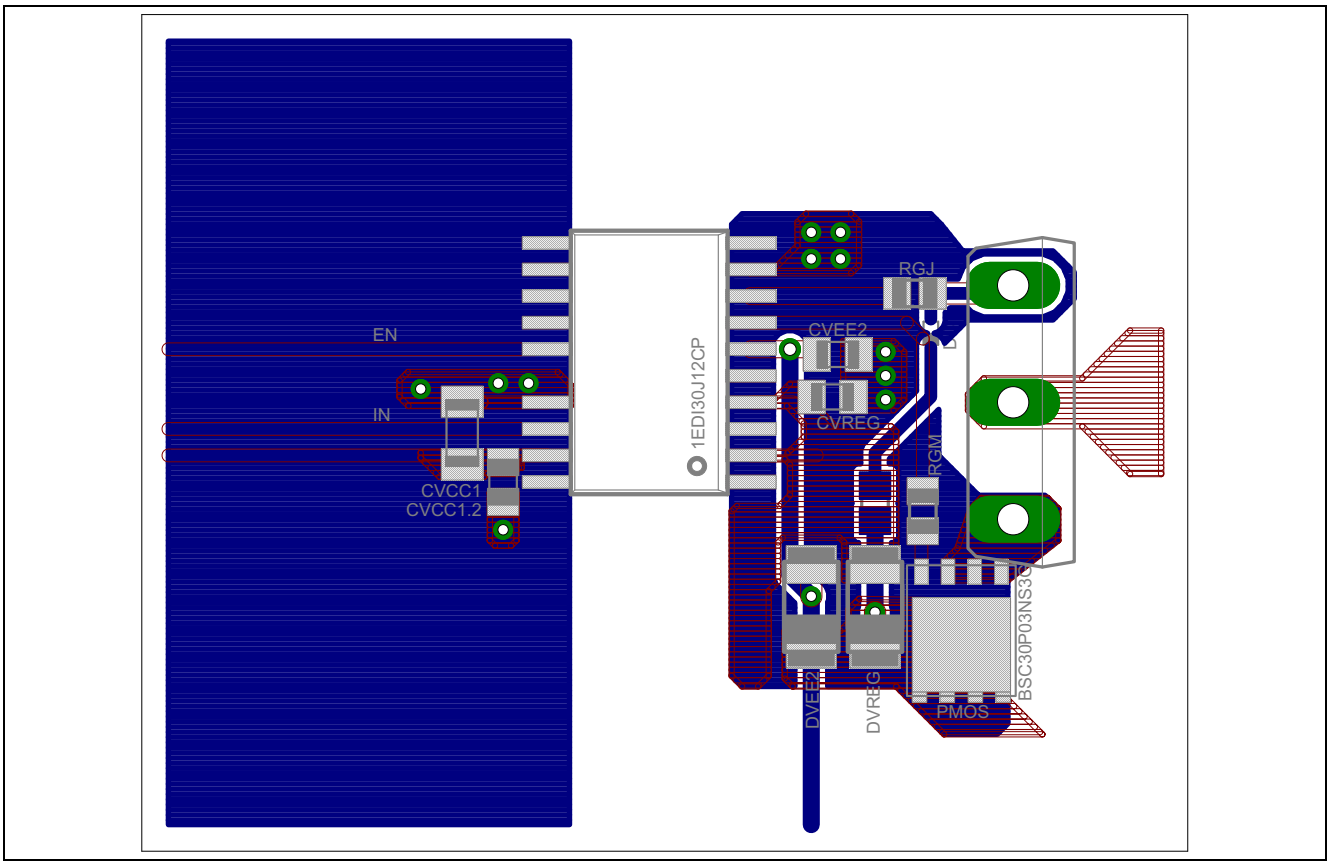


Figure 15 Typical layout of a1EDI30J12CP driver stage

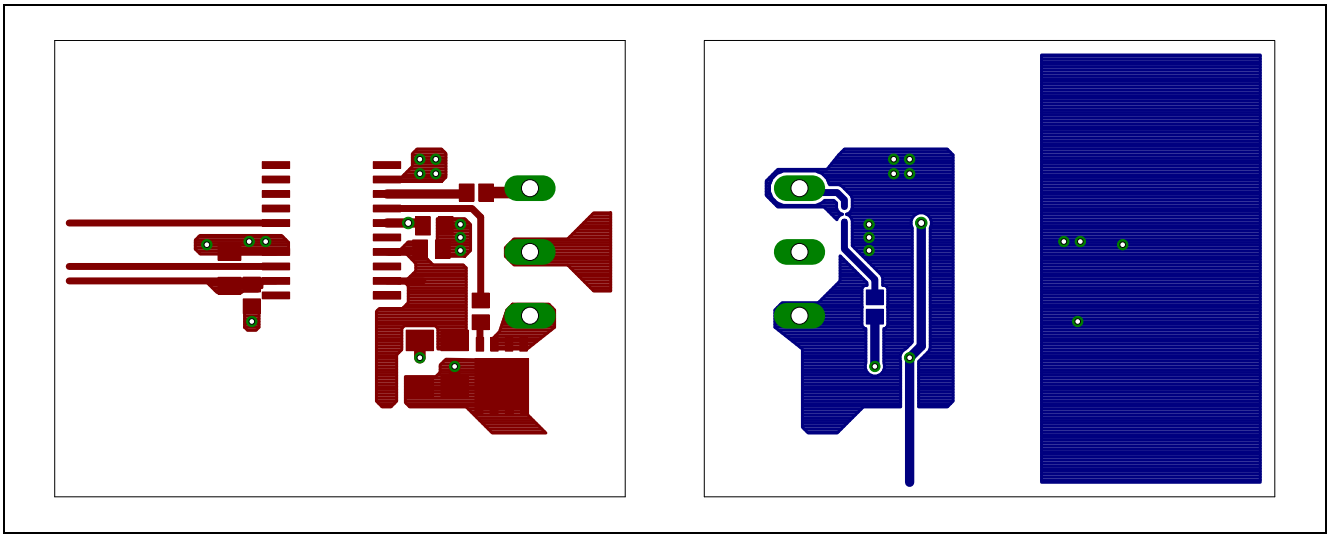


Figure 16 Thermal reference layout of a 1EDI30J12CP driver stage

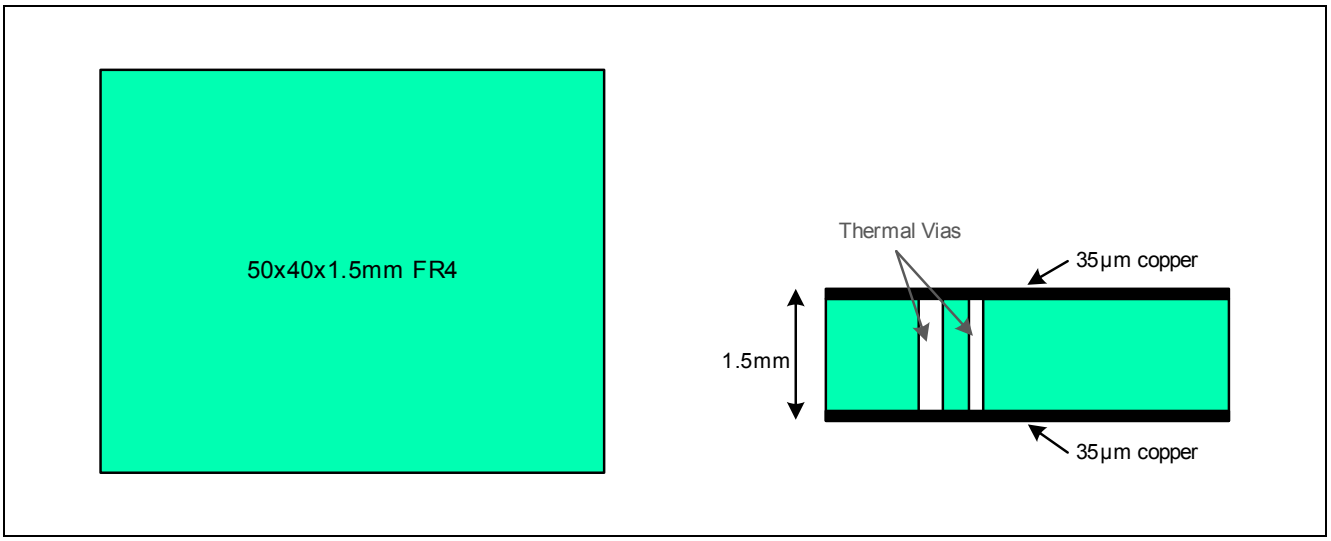


Figure 17 PCB Stack - Thermal reference layout

1EDI EiceDRIVER™ Enhanced 1EDI30J12Cx

Revision History: 2014-11-12, Rev. 1.3[1)]

Previous Revision: 1.2

Page	Subjects (major changes since last revision)
---	Removed 1EDI30J12CL (150mil variant)
---	

1) Preliminarydatasheeet may be changed without notice.

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