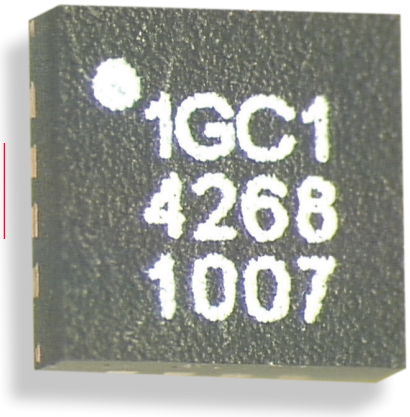
Keysight 1GC1-4268
DC - 12 GHz Packaged Divide-by-2 Prescaler

HMMC-5624-BLK 7” diameter reel/500 each

HMMC-5624-TR1 bubble strip/10 each

Data Sheet



Features

- Wide frequency range: 0.2 - 12 GHz
- High input power sensitivity: On–chip pre– and post–amps
  - 15 to +10 dBm (1 to 8 GHz)
  - 10 to +8 dBm (8 to 10 GHz)
  - 5 to +2 dBm (10 to 12 GHz)
- P_{out}: +0 dBm (0.5 V_{p-p})
- Low phase noise:
  - 153 dBc/Hz @ 100 kHz offset
- (+) or (–) Single supply bias with wide range: 4.5 to 6.5 V
- Differential I/0 with on–chip 50 Ω matching
- Available in RoHs compliant, 16 pin
- 3 mm x 3 mm QFN SMT package with integral heat sink

KEYSIGHT TECHNOLOGIES

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Description

The 1GC1-4268 is a packaged GaAs HBT MMIC prescaler which offers DC to 12 GHz frequency translation for use in communications and EW systems incorporating high–frequency PLL oscillator circuits and signal–path down conversion applications.
The differential I/O compatible prescaler provides a large input power sensitivity window, low phase noise and is packaged in a 3 mm x 3 mm 16-pin QFN SMT package.

- Package type:
  Quad flat - no pins (SMT QFN)
- Package dimensions:
  3.0 x 3.0 mm (0.118 x 0.118 in)
- Package thickness:
  0.90 ±0.10 mm
  (0.035 ±0.0039 in)
- Pin pitch: 0.5 mm (0.0197 in)
- Pin width: 0.20 mm (0.008 in)

Absolute maximum ratings[1]

(@ T_A =25 °C, unless otherwise indicated)

Symbol	Parameters/conditions	Min	Max	Units
V_{CC}	Bias supply voltage		+7	Volts
V_{EEE}	Bias supply voltage	-7		Volts
V_{CC} - V_{EEE}	Bias supply delta	0	+7	Volts
V_{Logic}	Logic threshold voltage	V_{CC}-1.5	V_{CC}-1.2	Volts
$P_{in\ (CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or RF_{in} Ports)		V_{CC} ± 0.5	Volts
T_{op} [2]	Pkg heatsink operating temp.	–40	+85	°C
T_{st}	Storage temperature	–65	+165	°C
T_{max}	Maximum solder reflow temp. (Max. 3 cycles @ 30 sec/cycle)		260	°C

1. Operation in excess of any parameter limit (except T_{op}) may cause permanent damage to the device.
2. MTTF > $1x10^6$ hours @ $T_{op} \leq 85$ °C. Operation in excess of maximum package pin operating temperature (T_{op}) will degrade MTTF.

DC specifications/physical properties

(T_A = 25 °C, $V_{CC} - V_{EE}$ = 5.0 volts, unless otherwise listed)

Symbol	Parameters/conditions	Min	Typ	Max	Units
$V_{CC} - V_{EE}$	Operating bias supply difference[1]	4.5	5.0	6.5	Volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current	34	40	46	mA
$V_{RFin(q)}$ $R_{Fout(q)}$	Quiescent DC voltage appearing at all RF ports		V_{CC}		Volts
V_{Logic}	Nominal ECL logic level (VLogic contact self–bias voltage, generated on–chip)	V_{CC} -1.45	V_{CC} -1.32	V_{CC} -1.25	Volts

1. Prescaler will operate over full specified supply voltage range. V_{CC} or V_{EE} not to exceed limits specified in Absolute maximum ratings section.

RF specifications

(T_A = 25 °C, Z_0 = 50 Ω, $V_{CC} - V_{EE}$ = 5.0 volts)

Symbol	Parameters/conditions	Min	Typ	Max	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation[1] (P_{in} = –10 dBm)		0.2	0.5	GHz
$f_{Self-Osc.}$	Output self–oscillation frequency[2]		3.4		GHz
P_{in}	@ DC, (square–wave input)	-15	> -25	+10	dBm
	@ $f$in = 500 MHz, (sine–wave input)	-15	> -20	+10	dBm
	$f$in = 1 to 8 GHz	-15	> -20	+10	dBm
	$f$in = 8 to 10 GHz	-10	> -15	+5	dBm
	$f$in = 10 to 12 GHz	-5	> -10	-1	dBm
RL	Small–signal input/output return loss (@f_{in} < 10 GHz)		15		dB
S_{12}	Small–signal reverse isolation (@f_{in} < 12 GHz)		30		dB
φ_N	SSB phase noise (@ P_{in} = 0 dBm, 100 kHz offset from a f_{out} = 1.2 GHz carrier)		-153		dB/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} = 10 GHz, P_{in} = –10 dBm)		1		ps
T_r or T_f	Output transition time (10 to 90% rise/fall time)		70		ps
P_{out}[3]	@ f_{out} < 1 GHz	-2.0	0.0		dBm
	@ f_{out} = 2.5 GHz	-3.5	-1.5		dBm
	@ f_{out} = 3.5 GHz	-4.5	-2.5		dBm
$\|V_{out(p-p)}$[4]	@ f_{out} < 1 GHz		0.5		Volts
	@ f_{out} = 2.5 GHz		0.42		Volts
	@ f_{out} = 3.5 GHz		0.37		Volts
$P_{Spitback}$	f_{out} power level appearing at RF_{in} or RF_{in} (@ f_{in} 10 GHz, unused RF_{out} or RF_{out} unterminated)		-50		dBm
	f_{out} power level appearing at RF_{in} or RF_{in} (@ f_{in} = 10 GHz, both RF_{out} & RF_{out} terminated)		-55		dBm
$P_{feedthru}$	Power level of ¦in appearing at RF_{out} or RF_{out} (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to $P_{in}(f_{in})$)		-30		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to $P_{out}(f_{out})$)		-25		dBc

1. For sine–wave input signal. Prescaler will operate down to DC for square–wave input signal. Min. divide frequency limited by input slew rate.
2. Prescaler can exhibit this output signal under bias in the absence of an RF input signal. This condition can be eliminated by use of theInput DC offset technique described on page 4.
3. Fundamental of output square wave's Fourier series.
4. Square wave amplitude calculated from P_{out}.

Applications

The 1GC1-4268 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase–noise PLL control circuitry or broadband frequency translation is required.

Operation

The device is designed to operate when driven with either a single–ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is “slew–rate” limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to DC when driven with a square–wave.

Due to the presence of an off–chip RF–bypass capacitor inside the package (connected to the Vthe device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not directly connected to any DC bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

AC–coupling

All RF ports are DC connected on–chip to the V_{CC} contact through on– chip 50 Ω resistors. Under any bias conditions where V_{CC} is not DC grounded, the RF ports should be AC coupled via series capacitors mount- ed on the PC–board. Only under bias conditions where V_{CC} is DC grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be “floated” and bias applied as the difference between V_{CC} and V_{EE}.

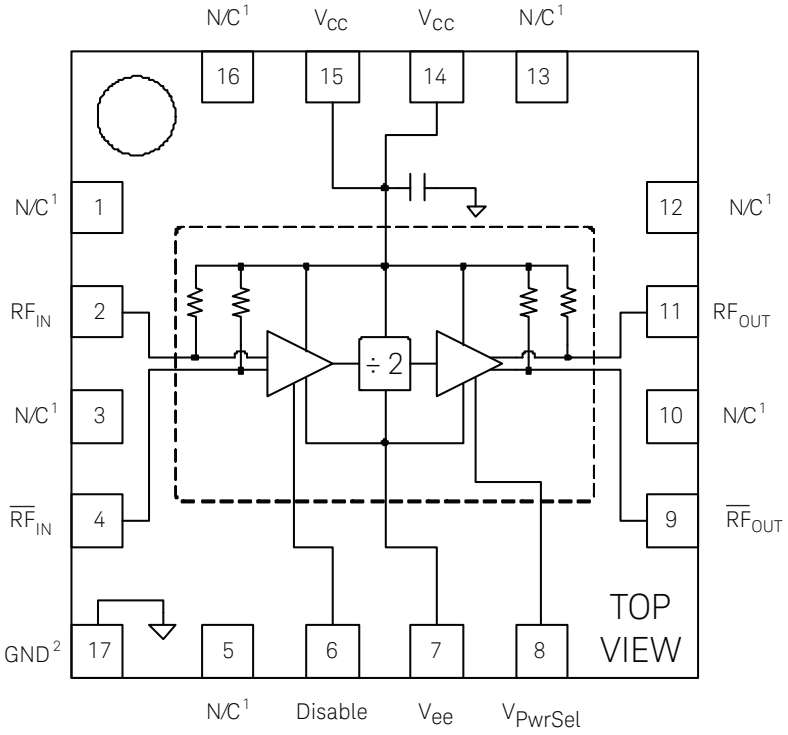
Input DC offset

If an RF signal with sufficient signal to noise ratio is present at the RF input pin, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain “ideal” conditions where the input is well matched at the right input frequency, the component may “self–oscillate”, especially under small signal input powers or with only noise present at the input. This “self–oscillation” will produce a undesired output signal also known as a false trigger.

To prevent false triggers or self–oscillation conditions, apply a 20 to 100 mV DC offset voltage between the RF_{in} and RF_{in} ports. This prevents in innoise or spurious low level signals from triggering the divider.

Adding a 10 KΩ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of 25 mV between the RF inputs. Note however, that the input sensitivity will be reduced slightly due to the presence of this offset.

An input DISABLE pin is also provided to allow the prescaler input pre-amp to be locked into either a logic “High” or “Low” state, thereby preventing false triggers.



1. N/C pins can be left open, but it is recommended to connect these to RF/DC ground.
2. Pin 17 is the center heat slug this must be connected to RF/DC ground. Use filled vias to prevent solder voids.
3. Discrete parallel plate capacitor or equivalent: 250 VWDC, +/- 10% capacitance tolerance

Figure 1: 1GC1-4268 simplified schematic

Assembly Techniques

Independent of the bias applied to the package, the backside of the package should always be connected to both a good RF ground plane and a good thermal heat sinking region on the PC–board to optimize performance. For single–ended output operation, the unused RF output pin should be terminated into 50 Ω to a contact point at the V_{CC} potential or to RF ground through a DC blocking capacitor.

Figure 2 shows the package / PCB assembly diagram for single–ended or differential input frequency operation through 12 GHz. For positive supply operation, V_{CC} is typically biased to a positive voltage between +4.5 and +6.5 volts and V_{EE} is grounded. For negative supply operation, V_{EE} is typically biased between –4.5 to –6.5 volts and V_{CC} is grounded. In either case, the supply contact to the package bias pin(s) must be capacitively bypassed (0.01 mF, recommended) to provide good bias stability, input sensitivity and low input power feed through. The bypass capacitor should be located as close as possible to the package pin.

In general, AC coupling capacitors are recommended on the RFin and RFout connections to the package. For positive supply operation, V_{CC} is positively biased resulting in a positive DC voltage appearing at RF_{in} or RF_{out}. In this case a AC coupling cap is required. For singulated package dimensions of the 3 mm x 3 mm QFN package, refer to Figure 3. The QFN SMT package is compatible with industry standard solder-reflow attach processes.

Moisture Compatibility

Injection mold components like the 1GC1-4268 are moisture-sensitive. The product is tested to the Moisture and Reflow Sensitivity Level 3A as per IPC/Jedec J-STD-020 and must be mounted within 168 hours of opening the shipping container. Store and handle parts for reflow and for rework per IPC/Jedec J-STD-033B.

Tape and Reel

The 1GC1-4268 is available in tape and reel format to facilitate automatic pick and place manufacturing. Figure 4 shows the tape dimension for the 1GC1-4268 packaged solution.

RoHS Compliance

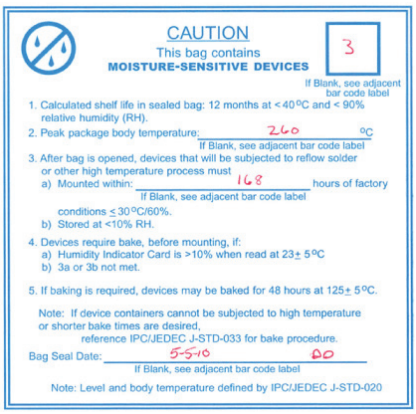
This part is RoHS compliant, meeting the requirements of the EU *Restriction of Hazardous Substances Directive* 2011/65/EU, commonly known as RoHS. Six substances are regulated: lead, mercury, cadmium, chromium VI (hexavalent chromium), polybrominated biphenyls (PBB), and polybrominated biphenyl ethers (PBDE). RoHS compliance requires that any residual concentration of these substances is below the Directive's maximum concentration values (MCV): cadmium 100 ppm by weight and all others 1000 ppm by weight.

ESD and Handling Precautions

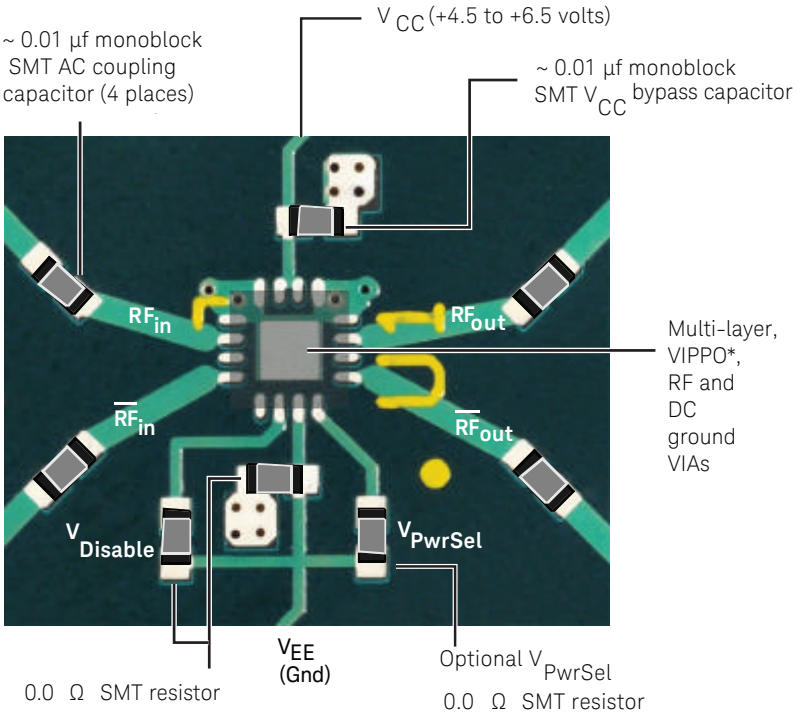
GaAs MMICs in either chip or SMT packages are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability. Keysight Technologies, Inc., *GaAs MMIC ESD, Die Attach and Bonding Guidelines - Application Note* (5991-3484EN) provides basic information on these subjects.

Additional References

PN #18, "HBT Prescaler Evaluation Board."

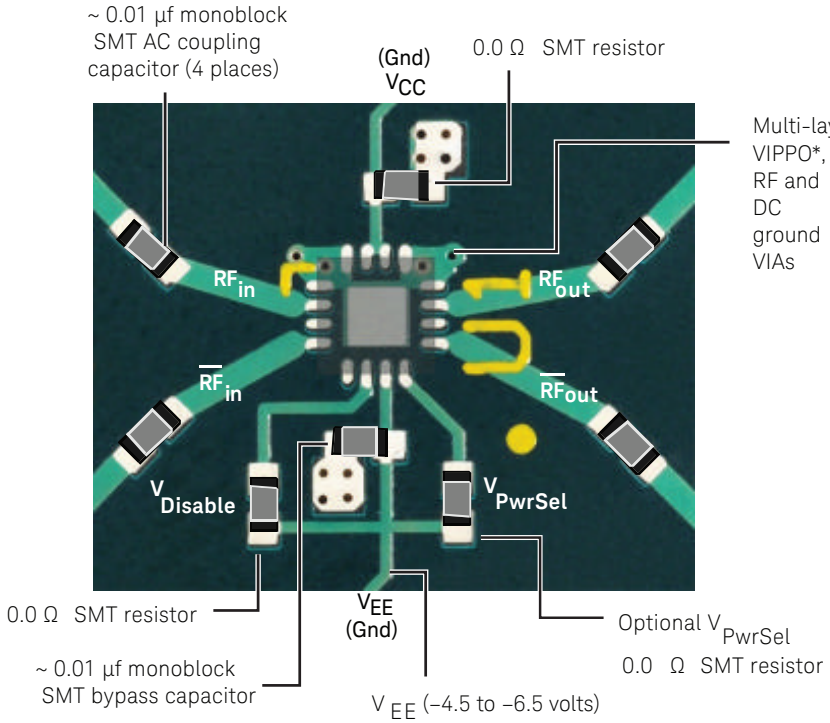


Positive Supply



a.) Single–supply, positive–bias configuration

Negative Supply



b.) Single–supply, negative–bias configuration

Optional V_{PwrSel} pin connection:

w/pin connected to GND: HIGH P_{out} assembly
(0.0 dBm [0.5 Vp–p] @ ICC =58 mA)

w/pin NOT connected to GND: LOW P_{out} assembly
(-6.0 dBm [0.25p–p] @ ICC =40 mA)

1. Supply bypass capacitors should be positioned as close as possible to the package supply pin.
2. V_{EE} MUST be grounded (positive supply configuration) or biased to a negative supply (negative supply operation.) V_{PwrSel} connections are optional depending on the output power and supply current requirements of the application.
3. The package backside grounding pad MUST be soldered to a good RF ground trace and thermal heatsinking area on the PC board to achieve optimum forward and reverse isolation. The package backside grounding pad is NOT DC connected to the device DC ground.
4. For single–ended output operation the unused RFout or RFout Pin should be terminated in 50 Ω to V_{CC} or to ground through an AC coupling capacitor (positive supply operation) or to ground (negative supply operation) to achieve optimum input sensitivity and reverse “Spitback” performance.
5. PCB ground paddle should incorporate multi-layer, “via In pad platted over (VIPPO)* RF and DC grounding vias.

Optional V_{PwrSel} pin connection:

w/pin connected to V_{EE}: HIGH P_{out} assembly
(+00 dBm [0.5 V_{p-p}] @ I_{EE} = –58 mA)

w/pin NOT connected to V_{EE}: LOW P_{out} assembly
(-6.0 dBm [0.25V_{p-p}] @ I_{EE} = –40 mA)

Figure 2: 1GC1-4268 assembly diagram

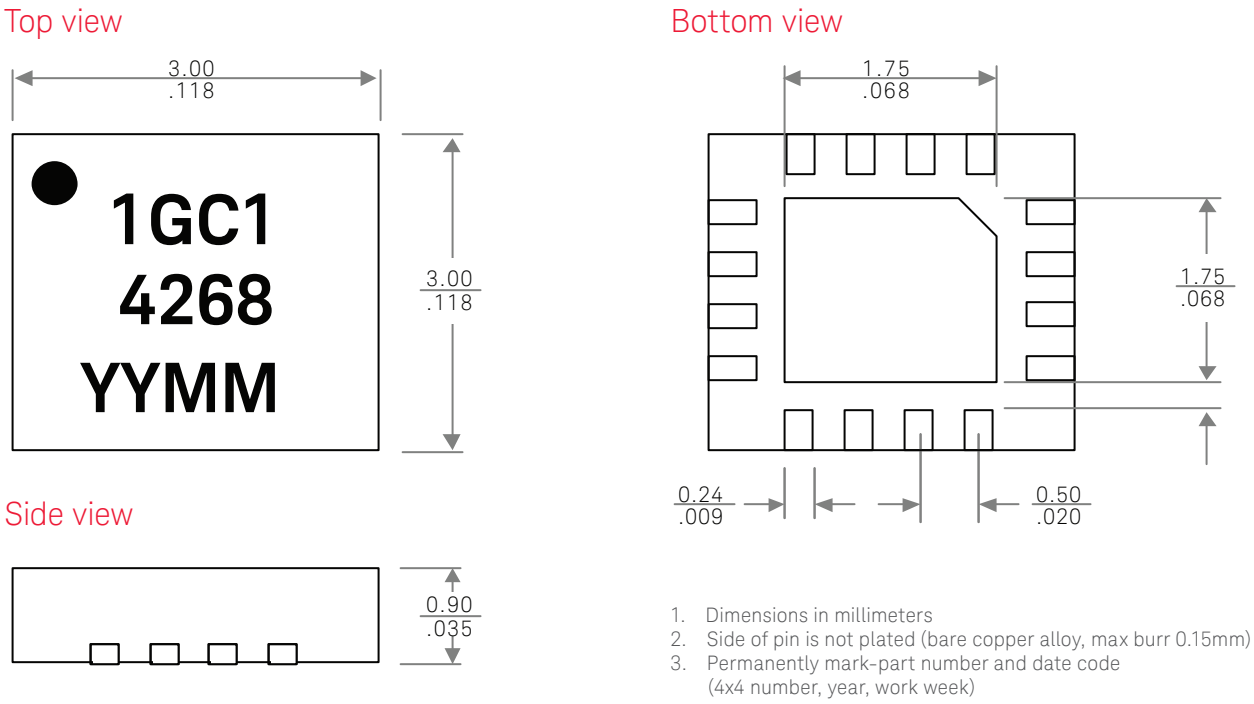


Figure 3. Package and dimensions

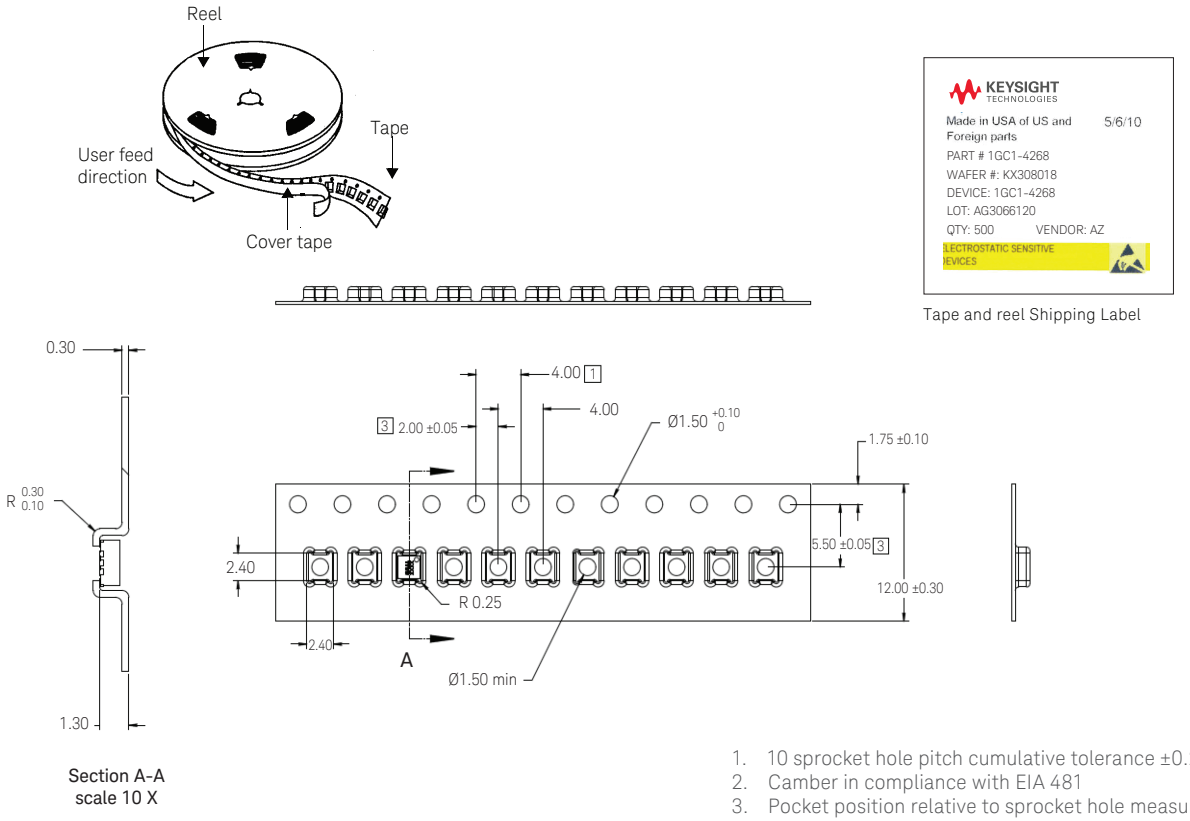


Figure 4. 1GC1-4268 assembly diagram (single–dupply, positive–bias configuration shown)

Supplemental Data

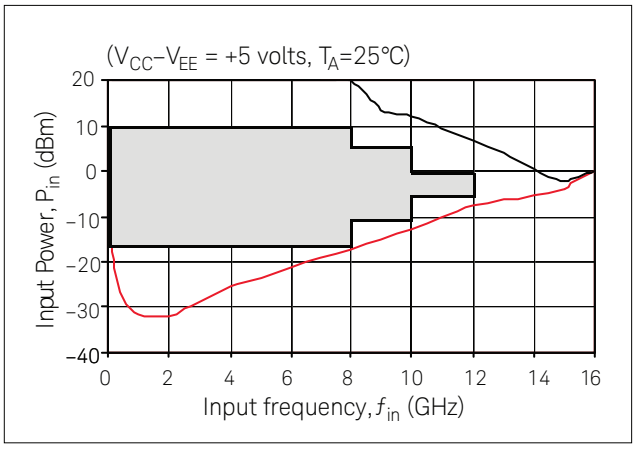


Figure 5. Typical input sensitivity window

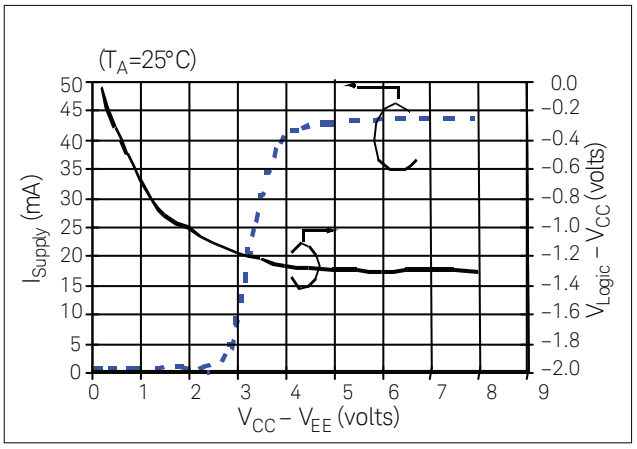


Figure 6. Typical supply current & V_{Logic} vs. supply voltage

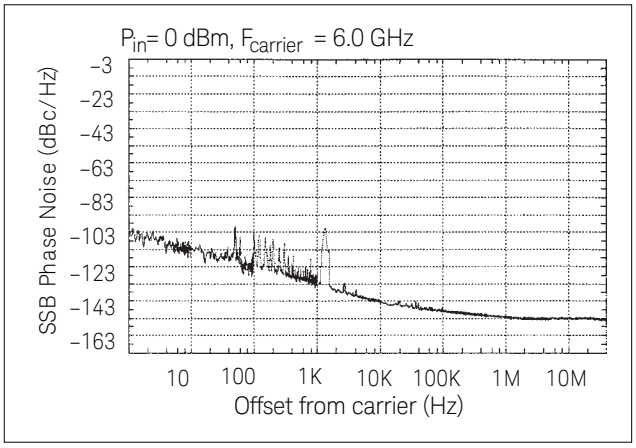


Figure 7. Typical phase noise performance

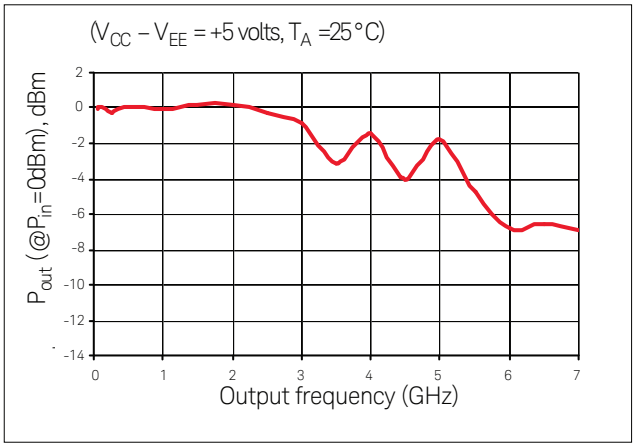


Figure 8. Output power vs. output frequency, f_{out}(GHz)

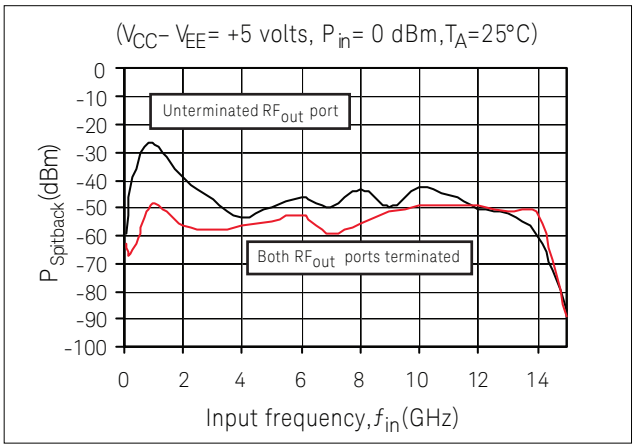


Figure 9. Typical "Spitback" power P(f_{out}) appearing at RF input port

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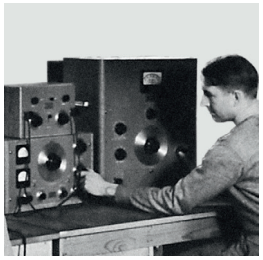

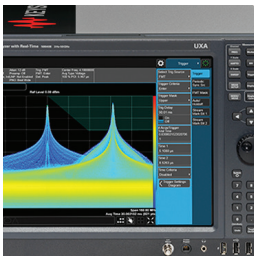

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The product described in this data sheet is **RoHS Compliant** and **RoHS Process Compatible** with a maximum temperature of 260 °C and a maximum of 3 temperature cycles.

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