Keysight 1GC1-8290

DC - 12 GHz Multi-Modulus Packaged Prescaler

1GC1-8290-BLK 7” diameter reel/500 each

1GC1-8290-TR1 bubble strip/10 each

Data Sheet

Features

- Multi–modulus (ECL selectable)
  divide by 1,2,4,8, or 16
- Input frequency range:
  0.1 to 12 GHz (sinewave input)
  DC to 12 GHz (squarewave input)
- High input power sensitivity:
  On–chip pre– and post–amps
  -20 to +10 dBm (Typ. 0.5 to 6 GHz)
  –15 to +10 dBm (Typ. 6 to 10 GHz)
  –10 to +5 dBm (Typ. 10 to 12 GHz)
- Dual–mode P_{out}:
  0.0 dBm [0.5 V_{p-p}] @ 96 mA
  +6.0 dBm [1.0 V_{p-p}] @ 118 mA
- Low phase noise:
  –153 dBc/Hz @ 100 kHz offset
- Positive or negative single supply bias operation
- Wide bias supply range:
  4.5 to 6.5 volt operating range
- Differential I/0 with on–chip
  50 Ω matching
- Available in RoHS compliant, 20 pin 4 mm x 4 mm QFN SMT package with integral heat sink

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Description

The 1GC1-8290 GaAs HBT MMIC prescaler offers broadband frequency translation for use in communications and EW systems incorporating high–frequency PLL oscillator circuits and signal–path down conversion applications. The prescaler provides multiple–modulus division and input signal pass–through capability as well as a large input sensitivity window, and low phase–noise. The 1GC1-8290 is available in either die form (1GC1-4021) or a 20–pin surface-mount QFN package (1GC1- 8290). In addition to the features listed above the component offers differential I/O, dual–output power mode plus an input disable pin to eliminate any false triggers or self–oscillation condition.

- Package type: Quad flat - no pins (SMT QFN)
- Package dimensions: 4.0 x 4.0 mm (0.157 x 0.157 in)
- Package thickness: 0.90 ± 0.10 mm (0.035 ± 0.0039 in)
- Pin pitch: 0.5 mm (0.0197 in)
- Pin width: 0.2 mm (0.009 in)

Absolute maximum ratings[1]

(@ TA = 25 °C, unless otherwise indicated)

Symbol	Parameters/conditions	Min	Max	Units
V_{CC}	Bias supply voltage		+7	Volts
V_{EE}	Bias supply voltage	–7		Volts
$V_{CC} – V_{EE}$	Bias supply delta	0	+7	Volts
$V_{A1,A2,A3}$	Modulus select voltage	V_{Logic} –2	V_{CC}	Volts
$V_{Disable}$	Pre–amp disable voltage	V_{EE}	V_{CC}	Volts
V_{Logic}	Logic threshold voltage	V_{CC} –1.5	V_{CC} –1.2	Volts
$P_{in(CW)}$	CW RF input power		+10	dBm
V_{RFin}	DC input voltage (@ RF_{in} or RF_{in} ports)		V_{CC} ±0.5	Volts
T_{op} [2]	Pkg heatsink operating temp.	–40	+85	°C
T_{st}	Storage temperature	–65	+165	°C
T_{max}	Maximum solder reflow temp. (Max. 3 cycles @ 30 sec/cycle)		260	°C

1. Operation in excess of any parameter limit (except T_{op}) may cause permanent damage to the device.
2. MTTF >1X10^6 hours @ T_{op} ≤ 85 °C. Operation in excess of maximum package pin operating temperature (T_{op}) will degrade MTTF.

DC specifications/physical properties

(T_A = 25 °C, V_{CC} – V_{EE} = 5.0 volts, unless otherwise listed)

Symbol	Parameters/conditions	Min	Typ	Max	Units
V_{CC} – V_{EE}	Operating bias supply difference[1]	4.5	5.0	6.5	Volts
$\|I_{CC}\|$ or $\|I_{EE}\|$	Bias supply current (HIGH output power configuration[2]: VP_{wrSel} = V_{EE})	100	118	136	mA
	Bias supply current (LOW output power configuration: VP_{wrSel} = open)	83	96	110	mA
$V_{RFin(q)}$ $V_{RFout(q)}$	Quiescent DC voltage appearing at all RF ports		V_{CC}		Volts
V_{Logic}	Nominal ECL logic level (On–chip, self–biased ECL–threshold voltage)	V_{CC} – 1.40	V_{CC} –1.34	V_{CC} –1.25	Volts

1. Prescaler will operate over full specified supply voltage range. V_{CC} or V_{EE} not to exceed limits specified in Absolute maximum ratings section.
2. High output power configuration: $P_{out}[V_{out}]$=+6.0 dBm [1.0V_{p-p}], Low output power configuration: $P_{out}[V_{out}]$= 0.0 dBm [0.5 V_{p-p}].

RF specifications

(T_A = 25 °C, Z_0 = + 50 Ω, V_{CC}–V_{EE} = 5.0 volts)

Symbol	Parameters/conditions	Min	Typ	Max	Units
N_{Ratio}	Divide modulus, N: f_{out}=f_{in}/N, pass–through: N=1		1,2,4,8, or 16		
$f_{in(max)}$	Maximum input frequency of operation[1] (P_{in} = –5 dBm, modulus = 1)	6	8		GHz
	Maximum input frequency of operation (P_{in} = –5 dBm, modulus = ≥2)	12	16		GHz
$f_{in(min)}$	Minimum input frequency of operation[2] (P_{in} = –1 dBm)		0.1	0.3	GHz
$f_{Self-Osc.}$	Output self–oscillation frequency[3]		13.6 / N		GHz
P_{in}	@ DC, (square–wave input)	–20	–25 to > +10	+10	dBm
	@ f_{in} = 500 MHz, (sine–wave input)	–18	–28 to > +10	+10	dBm
	f_{in} = 1 to 4 GHz	–18	–25 to > +10	+10	dBm
	f_{in} = 4 to 6 GHz	–11	–20 to > +10	+9	dBm
	f_{in} = 6 to 10 GHz	–9	–15 to +10	+6	dBm
	f_{in} = 10 to 12 GHz	–7	–10 to +5	+1	dBm
RL	Small–signal input/output return loss (@ f_{in}< 12 GHz)		12		dB
S_{12}	Small–signal reverse isolation (@ f_{in}< 12 GHz)		25		dB
φ_N	SSB phase noise (@ P_{in} = +10 dBm, 100 kHz Offset from a f_{in} = 10.2 GHz carrier, N = 2)		–153		dBc/Hz
Jitter	Input signal time variation @ zero–crossing (f_{in} =10 GHz, P_{in} = –10 dB)		1		pS
T_r or T_f	Edge speed (10 to 90% rise/fall time)		70		pS

1. For output amplitudes with less than 3 dB roll–off from 1 GHz output power values.
2. For sine–wave input signal. Prescaler will operate down to DC for square–wave input signal. Minimum divide frequency limited by input slew–rate.
3. N = Divide modulus. Prescaler may exhibit this output signal under bias in the absence of an RF input signal. This condition may be eliminated by use of the Pre–amp Disable ($V_{Disable}$) feature, or the differential Input de–biasing techniques.

RF specifications (continued)

(T_A = 25 °C, Z0 = + 50 Ω, V_{CC}–V_{EE} = 5.0 volts)

Symbol	Parameters/conditions	Min	Typ	Max	Units
			High output power operating mode[1]		
P_{out}	@ f_{out} < 1 GHz	4.0	6.0		dBm
	@ f_{out} = 3 GHz	3.0	5.5		dBm
	@ f_{out} = 6 GHz	1.0	4.0		dBm
$\|V_{out(p-p)}\|$	@ f_{out} < 1 GHz		0.99		Volts
	@ f_{out} = 3 GHz		0.94		Volts
	@ f_{out} = 6 GHz		0.79		Volts
$P_{Spitback}$	Output frequency power level appearing at RF_{in} or $\overline{RF}_{in}$ ports. (@ f_{in} 12 GHz, N>1, unused RF_{out} unterminated)		-28		dBm
	Power level of output signal appearing at RF_{in} or $\overline{RF}_{in}$ ports. (@ f_{in} 12 GHz, N>1, unused RF_{out} terminated into 50 Ω)		-40		dBm
$P_{feedthru.}$	Power level of input signal appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to Pin(f_{in}), N>1)		25		dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out}(f_{out}))		22		dBc
			Low output power operating mode[2]		
P_{out}	@ f_{out} < 1 GHz		–2.0	0.0	dBm
	@ f_{out} = 3 GHz		–3.0	–0.5	dBm
	@ f_{out} = 6 GHz		–5.0	–2.0	dBm
$\|V_{out(p-p)}\|$	@ f_{out} < 1 GHz			0.5	Volts
	@ f_{out} = 3 GHz			0.47	Volts
	@ f_{out} = 6 GHz			0.39	Volts
$P_{Spitback}$	Output frequency power level appearing at RF_{in} or $\overline{RF}_{in}$ ports. (@ f_{in} 12 GHz, N>1, unused RF_{out} unterminated)			–34	dBm
	Power level of output signal appearing at RF_{in} or $\overline{RF}_{in}$ ports. (@ f_{in} 12 GHz, N>1, unused RF_{out} terminated into 50 Ω)			–47	dBm
$P_{feedthru}$	Power level of input signal appearing at RF_{out} or $\overline{RF}_{out}$ (@ f_{in} = 12 GHz, P_{in} = 0 dBm, referred to P_{in}(f_{in}), N>1)			25	dBc
H_2	Second harmonic distortion output level (@ f_{out} = 3.0 GHz, referred to P_{out}(f_{out}))			22	dBc

1. V_{PwrSel}=V_{EE}.
2. V_{PwrSel}=open circuit.

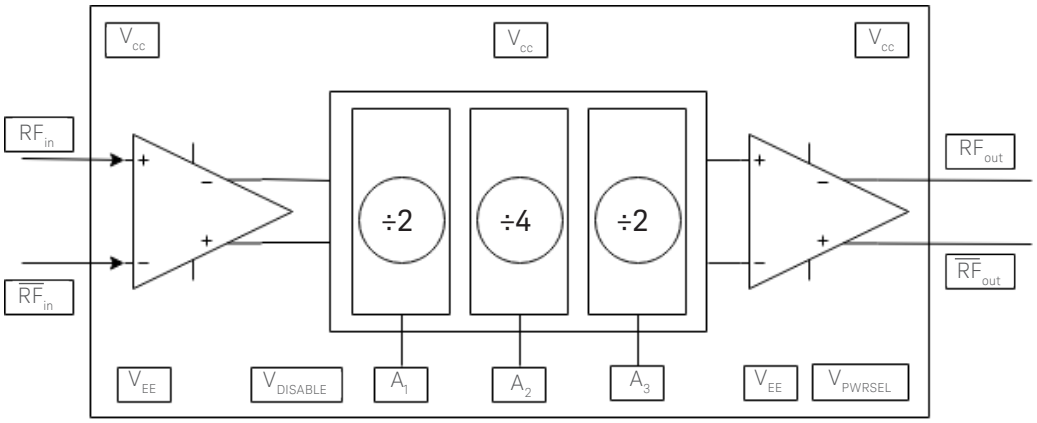


Figure 1. 1GC1-8290 Simplified schematic
See figure 6 for 1GC1-8290 pin connections

Applications

The 1GC1-8290 is designed for use in high frequency communications, microwave instrumentation and EW radar systems where low phase noise PLL control circuitry or broadband frequency translation is required.

Operation

The package is designed to operate when driven with either a single–ended or differential sinusoidal input signal over a 100 MHz to 12 GHz bandwidth. Below 300 MHz the prescaler input is "slew–rate" limited requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to DC when driven with a square–wave as long as the slew rate is greater than 0.18 V/nS or 10% to 90% edge speeds of ~ 3 nS. AC coupling at the RFin pin is recommended for most applications.

The package can be operated from either a single positive or single negative supply. For positive supply operation VCC is nominally biased at any voltage in the +4.5 to +6.5 volt range with V_{EE} (or V_{EE} & V_{PwrSel}) grounded. For negative bias operation, V_{CC} is typically grounded and a negative voltage between – 4.5 to –6.5 volts is applied to V_{EE} (or V_{EE} & V_{PwrSel}). The package will operate in pass– through mode (with unity divide modulus) or at any of four different divide ratios including 2, 4, 8, or 16 according to following table:

Modulus select truth table

1GC1-8290	**Select lines**[1]		
Divide modulus	**A_1**	**A_2**	**A_3**
÷ 1	L	L	L
÷ 2	L	L	H
÷ 4	L	H	L
÷ 8	L	H	H
÷ 16	H	X	X

1. See Table Below.

Valid input logic threshold values (ECL–compatible)[1]

(T_A = 25 °C)

Function	**Symbol**	**Conditions**	**Valid input control levels and resulting current values (mA)**
Input disable	$V_{Disble(High)}$ [Disable]		(V_{Logic} + 0.25) through V_{CC}
	$V_{Disable(Low)}$ [Enable]		V_{EE} through (V_{Logic} – 0.25)
	$I_{Disable}$	$V_D > V_{EE}$+3	($V_{Disable}$ –V_{EE} – 3) / 5000
		$V_D < V_{EE}$+3	0
Modulus select	Vselect (A1, A2, A3) (high–state)		(V_{Logic} + 0.25) through V_{CC}
	Vselect (A1, A2, A3) (low–state)		(V_{Logic} –2.0) through (V_{Logic} 0.25)
	Iselect (A1, A2, A3) (high & low–state)		($Vselect_{A1,A2,A3}$–V_{EE} – 3) / 5000

1. See DC specifications table for self–biased V_{Logic} operating values.

See Figure 6 for package pinouts and bias/RF connection locations.

Several features are designed onto this prescaler

Dual–output power feature

Bonding both V_{EE} and VP_{wrSel} pins to either ground (positive bias mode) or the negative supply (negative bias mode), will deliver ~6.0 dBm [1.0 V_{p-p}] at the RF output port while drawing ~118 mA supply current. Eliminating the V_{PwrSel} connection results in reduced output power and voltage swing, 0.0 dBm [0.5 V_{p-p}] but at a reduced current draw of ~96 mA resulting in less overall power dissipation.

Note: V_{EE} must *always* be bonded and V_{PwrSel} must *never* be biased to any potential other than V_{EE} or open–circuited.)

V_{Logic} ECL pin

Under normal conditions no connection or external bias is required to this pin and it is self–biased to the on–chip ECL logic threshold voltage (V_{CC}–1.34 V). The user can provide an external bias to this pin (1.5 to 1.2 volts less than V_{CC}) to force the prescaler to operate at a system generated logic threshold voltage.

Input disable feature

By applying an external bias to this pin (more positive than V CC –1.34 V), the input preamplifier stage is locked preventing false trigger frequency division and self–oscillation frequency

Input DC offset

Another method used to prevent false triggers or self–oscillation conditions is to apply a 20 to 100 mV DC offset voltage between the RFin and RFin ports. This prevents noise or spurious low level signals from triggering the divider.

Assembly techniques

Figures 4 and 5 show the package assembly diagram for single–ended or differential I/O operation through 12 GHz. For positive supply operation, V_{CC} is typically biased to a positive voltage between +4.5 and +6.5 volts and V_{EE} is grounded. For negative supply operation, V_{EE} is typically biased between –4.5 to –6.5 volts and V_{CC} is grounded. In either case the supply contact to the package bias pin must be capacitively bypassed (0.01 µF, recommended) to provide good bias stability, input sensitivity and low input power feedthrough. The bypass capacitor should be located as close as possible to the package pin.

Since the voltage applied to the modulus select lines must not be less than V_{Logic} –2.0 volts, 2 KΩ resistors are generally added between the select line controls and the V_{EE} supply rail.

In general, AC coupling capacitors are recommended on the RF_{in} and RF_{out} connections to the package. For positive supply operation, V_{CC} is positively biased resulting in a positive DC voltage appearing at RF_{in} or RF_{out}. In this case a AC coupling cap is required.

Due to on–chip 50 Ω matching resistors at all four RF ports, no external termination is required. However, improved input sensitivity and reverse "Spitback" performance (~12 dB) can be achieved by a) terminating the unused RF_{out} port to V_{CC} through 50 Ω, or b) through 50 Ω to ground via an AC coupling capacitor for positive supply operation or c) through 50 Ω directly to ground for negative supply operation.

For singulated package dimensions of the 4 mm x 4 mm QFN package, refer to Figure 6.

The QFN SMT package is compatible with industry standard solder-reflow attach processes.

Moisture Compatibility

Injection mold components like the 1GC1-8290 are moisture-sensitive. The product is tested to the Moisture and Reflow Sensitivity Level 3 as per IPC/Jedec J-STD-020 and must be mounted within 168 hours of opening the shipping container. Store and handle parts for reflow and for rework per IPC/Jedec J-STD-033B.

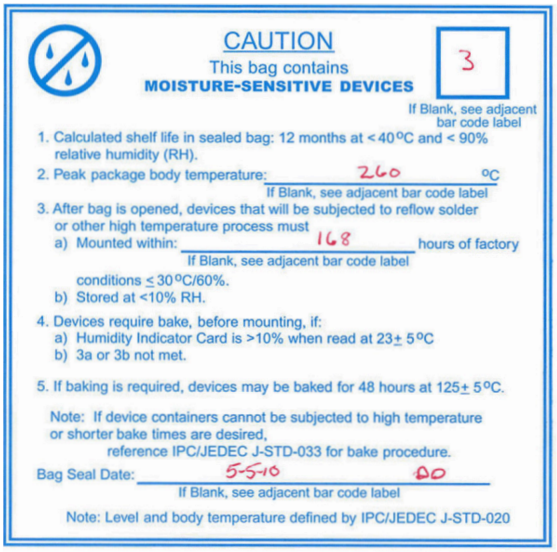


Figure 2. 1GC1-4251 moisture sensitivity label

Tape and Reel

The 1GC1-8290 is available in tape and reel format to facilitate automatic pick and place manufacturing. Figure 5 shows the tape dimension for the 1GC1-8290 packaged solution.

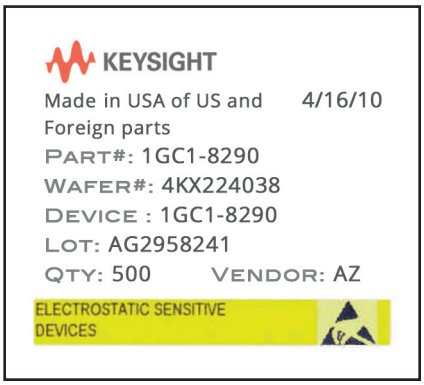


Figure 3. Tape and reel label

ESD and Handling Precautions

GaAs MMICs in either chip or SMT packages are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability.

Keysight Technologies, Inc., *GaAs MMIC ESD, Die Attach and Bonding Guidelines - Application Note* (5991-3484EN) provides basic information on these subjects.

Positive supply

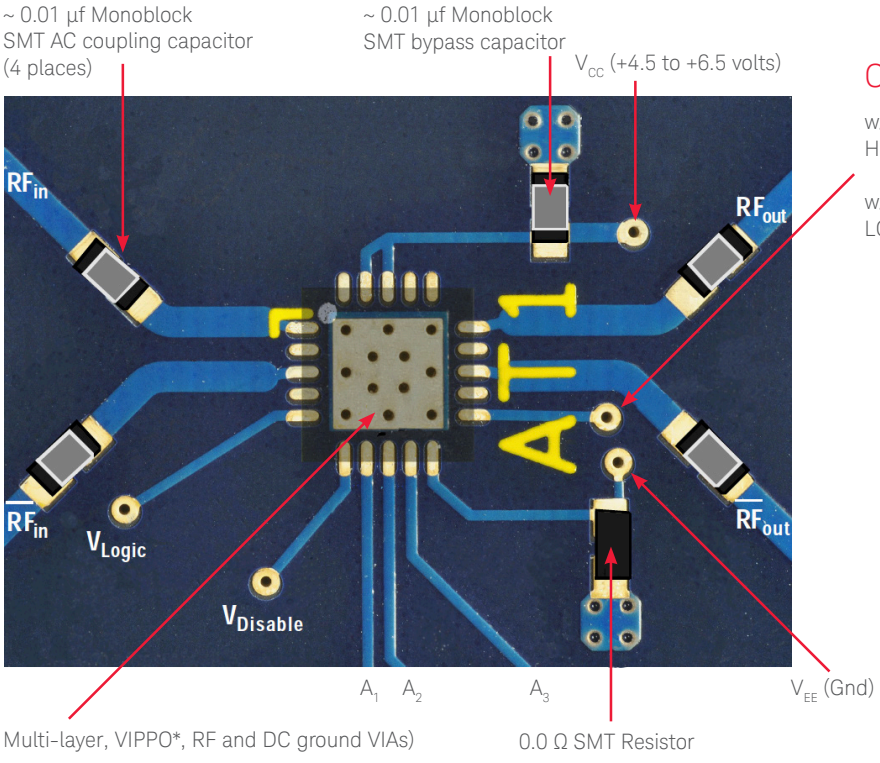


Figure 4. 1GC1-8290 assembly diagram: single–supply, positive–bias configuration

OPTIONAL V_{PwrSel} pin connection

w/pin connected to GND:
HIGH P_{out} assembly (6.0 dBm [1.0 V_{p-p}] @ I_{CC} = 118 mA)

w/pin NOT connected to GND:
LOW P_{out} assembly (0.0 dBm [0.5 V_{p-p}] @ I_{CC} = 96 mA)

Notes

1. Supply bypass capacitors should be positioned as close as possible to the package supply pin.
2. V_{EE} MUST be grounded (positive supply configuration) or biased to a negative supply (negative supply operation.) V_{PwrSel} connections are optional depending on the output power and supply current requirements of the application.
3. The package backside grounding pad MUST be soldered to a good RF ground trace and thermal heatsinking area on the PC board to achieve optimum forward and reverse isolation. The package backside grounding pad is NOT DC connected to the device DC ground.
4. For single–ended output operation the unused RFout or RFout Pin should be terminated in 50 Ω to V_{CC} or to ground through an AC coupling capacitor (positive supply operation) or to ground (negative supply operation) to achieve optimum input sensitivity and reverse "Spitback" performance.
5. PCB ground paddle should incorporate multi-layer, “Via In Pad Platted Over (VIPPO)* RF and DC grounding vias.

Negative supply

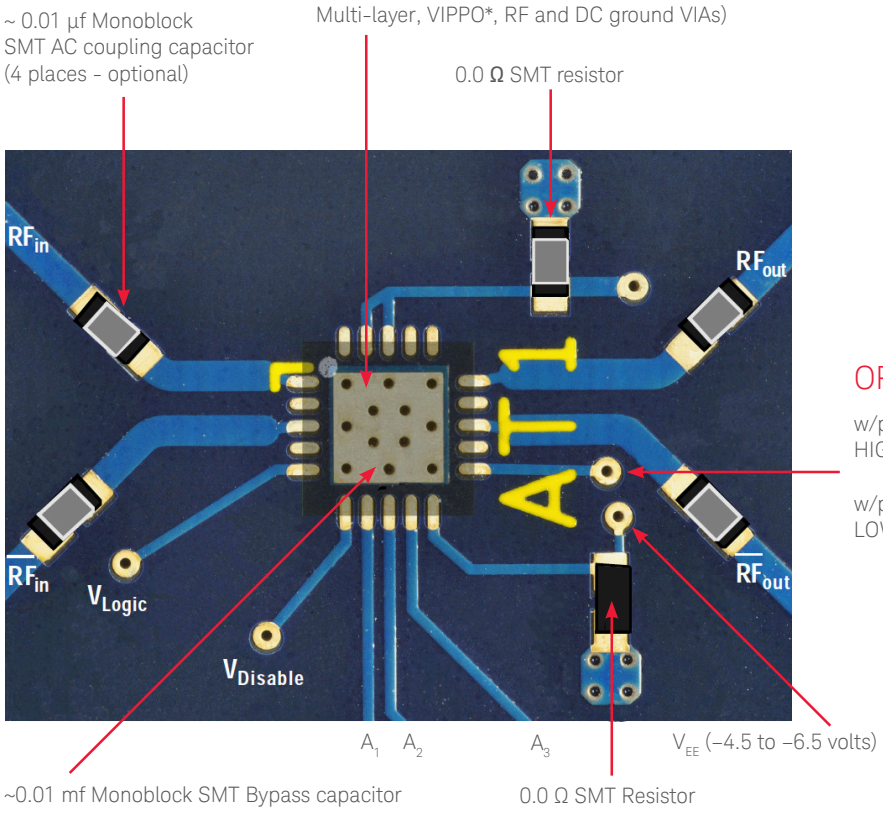
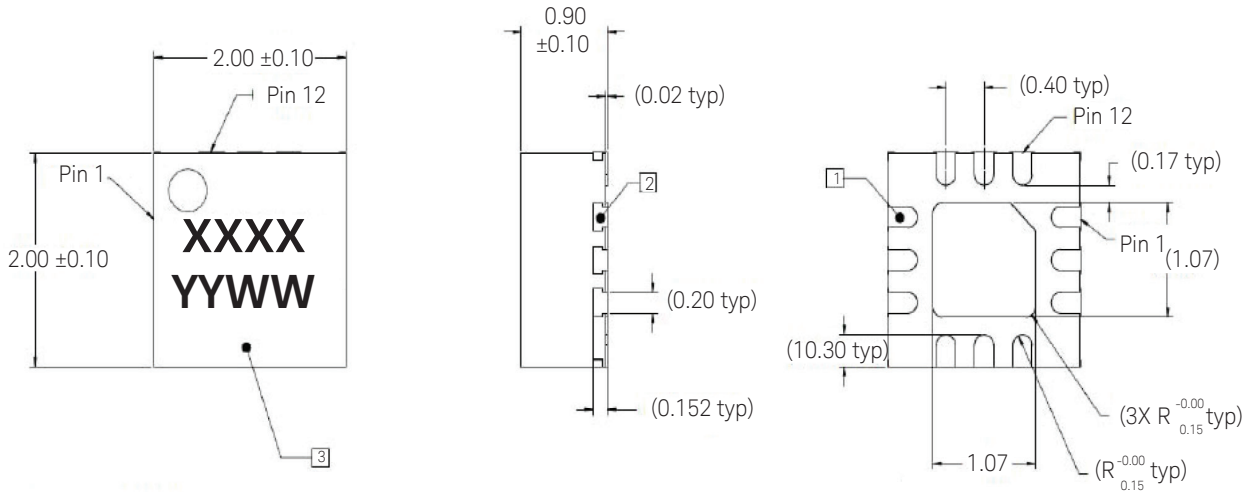


Figure 5. 1GC1-8290 assembly diagram: single–supply, negative–bias configuration

OPTIONAL V_{PwrSel} pin connection

w/pin connected to V_{EE}:
HIGH P_{out} assembly (+6.0 dBm [1.0 V_{p-p}] @ I_{EE} = –118 mA)

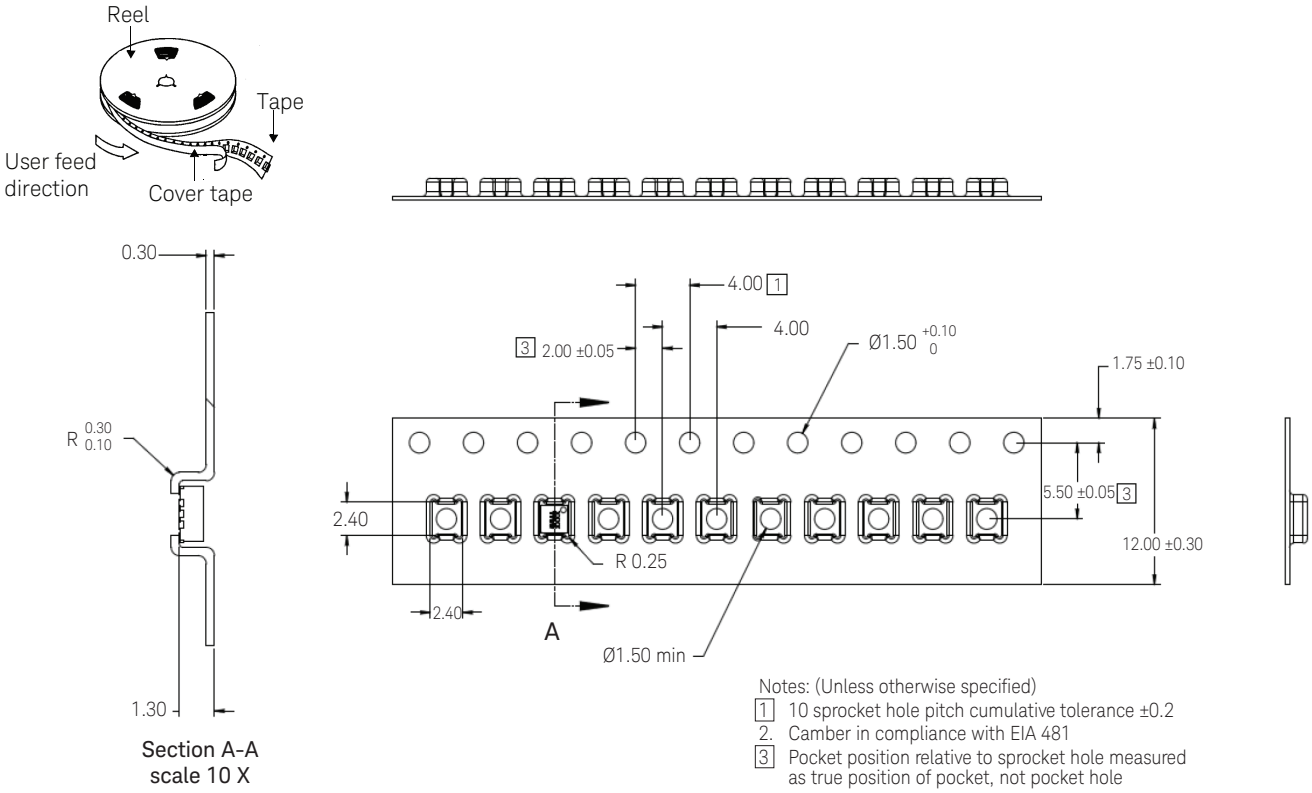
w/pin NOT connected to V_{EE}:
LOW P_{out} assembly (0.0 dBm [0.5 V_{p-p}] @ I_{EE} = 96 mA)



Topside label:
nnXX-nnXX = Keysight 4x4 part number
YYWW = Year - Work Week

3 Permanently mark 4x4 part number without leading '1G' and '42,' and date code (Example: 'C145' for 1GC1-4245 year, work week)
2 Side of lead is not plated (bare copper alloy) max burr 0.05 mm
1 Lead plating per assembly drawing
Notes: (Unless otherwise specified)

Figure 6. 1GC1-8290 package dimensions



Notes: (Unless otherwise specified)
1 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3 Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Figure 7. 1GC1-8290 tape and reel configuration

Supplemental Data

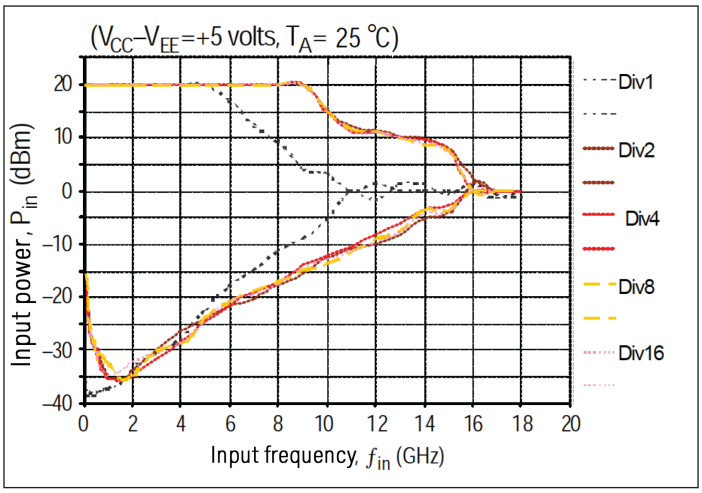


Figure 8. Input sensitivity window

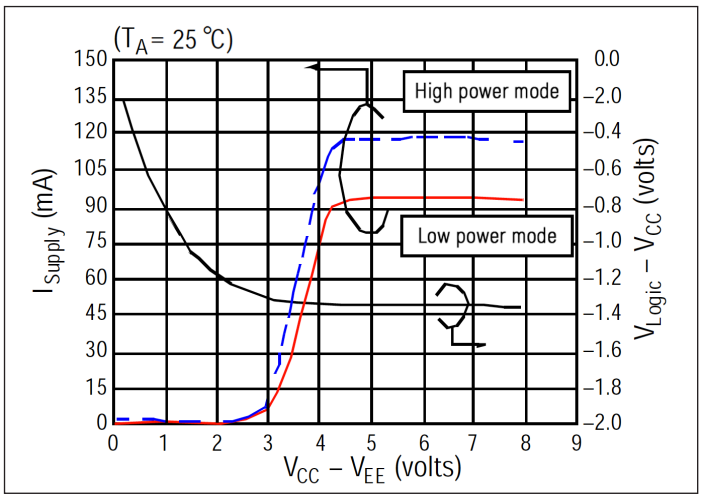


Figure 9. Supply current & V_{Logic} vs. supply voltage

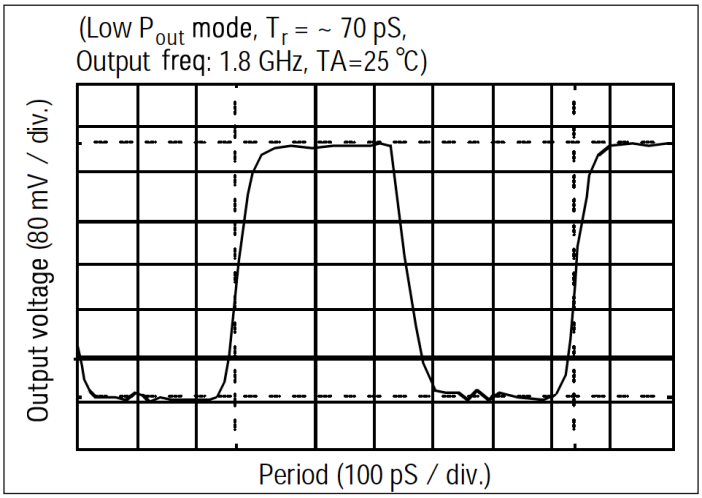


Figure 10. Output voltage waveform (Low P_{out} mode)

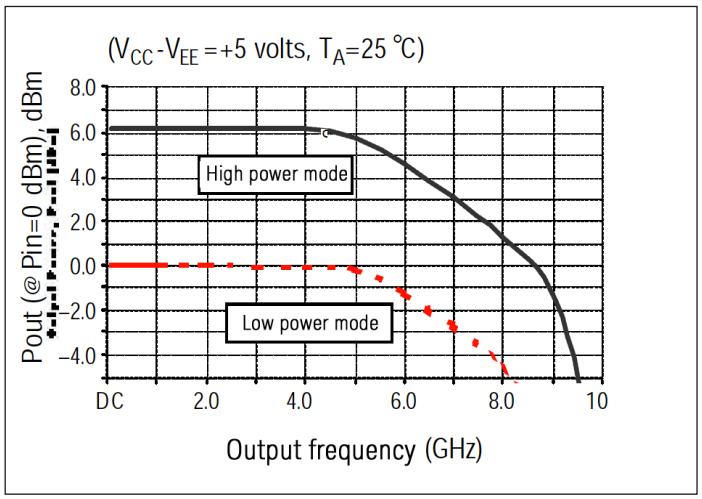


Figure 11. Output power vs. output frequency, f_{out} (GHz)

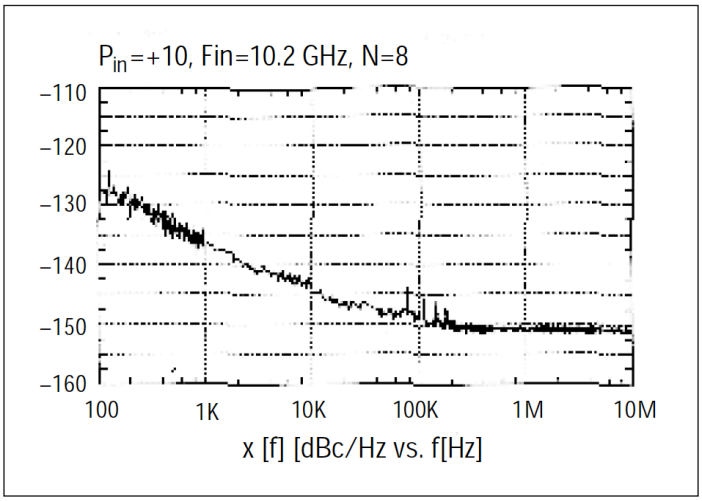


Figure 12. Phase noise performance

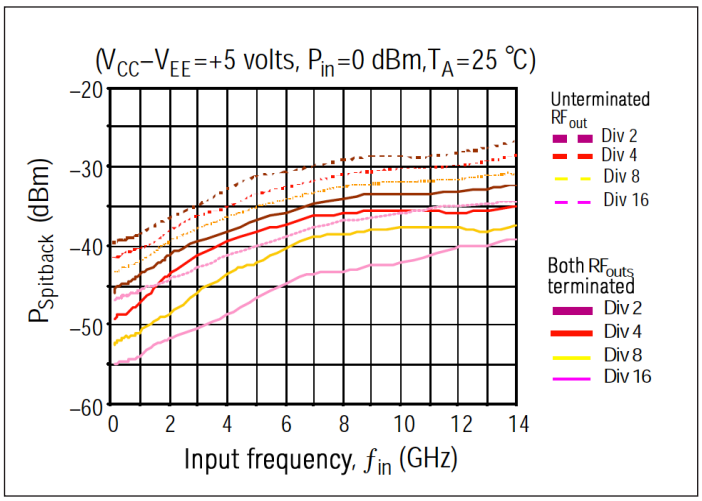


Figure 13. "Spitback" power P(f_{ou}) appearing at RF input port

Supplemental Data

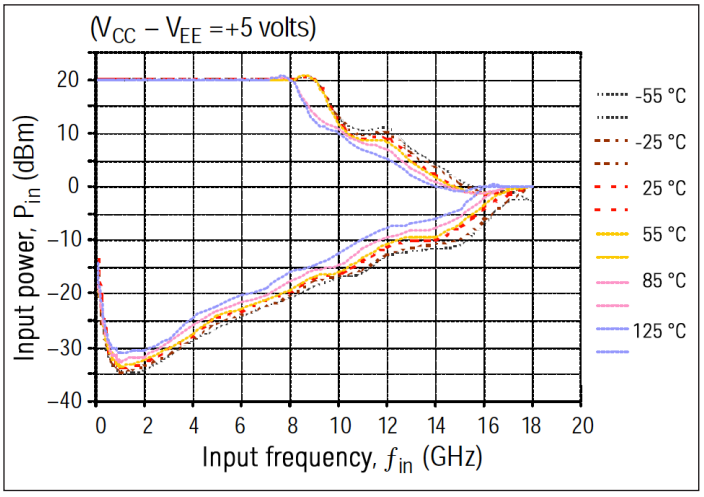


Figure 14. Typical divide–by–2 input sensitivity window (over temperature)

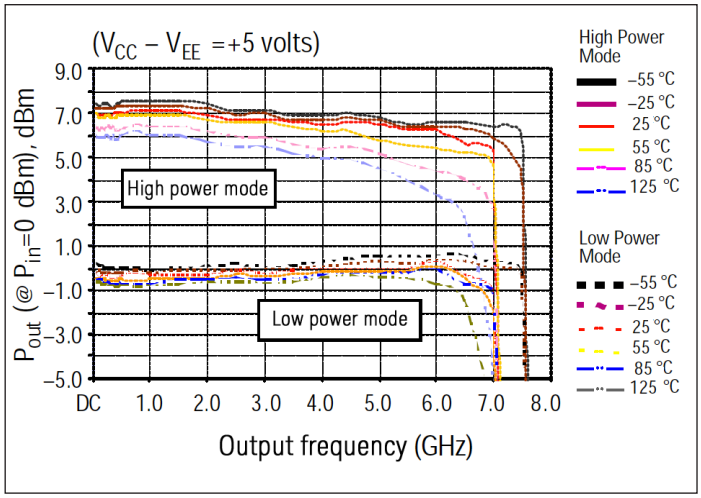


Figure 15. Typical divide–by–2 output power vs. output frequency (over Temperature)

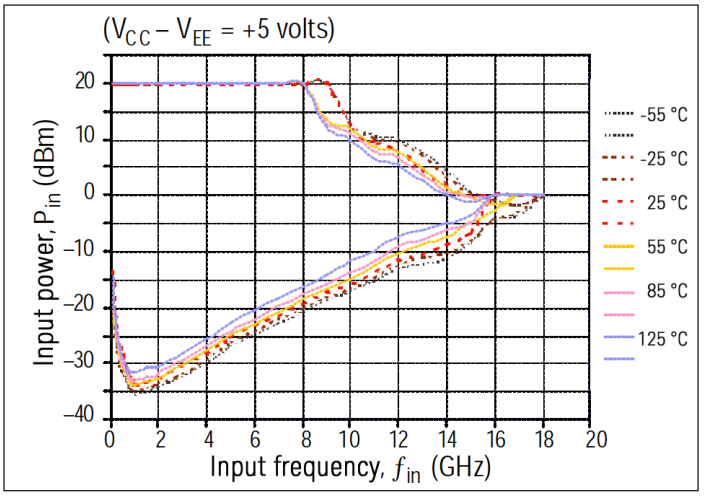


Figure 16. Typical divide-by-16 input sensitivity window (over temperature)

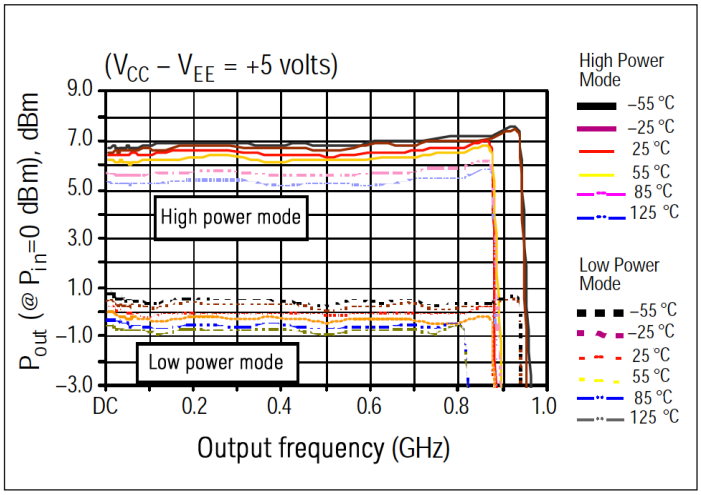


Figure 17. Typical divide-by-16 output power vs. output frequency (over temperature)

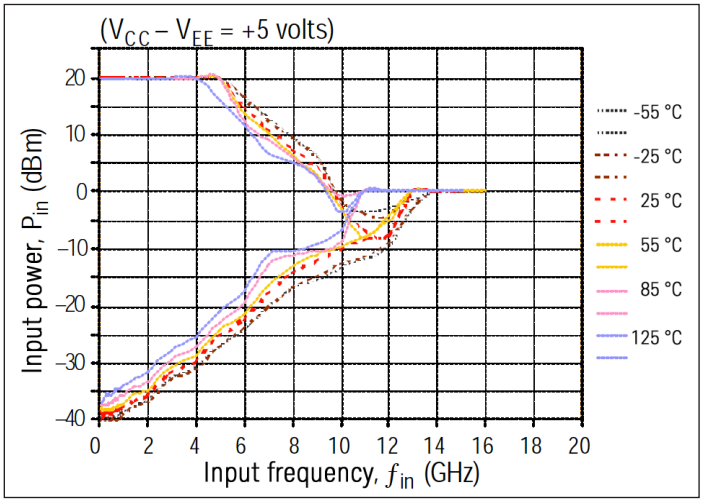


Figure 18. typical pass–through input sensitivity window (over temperature)

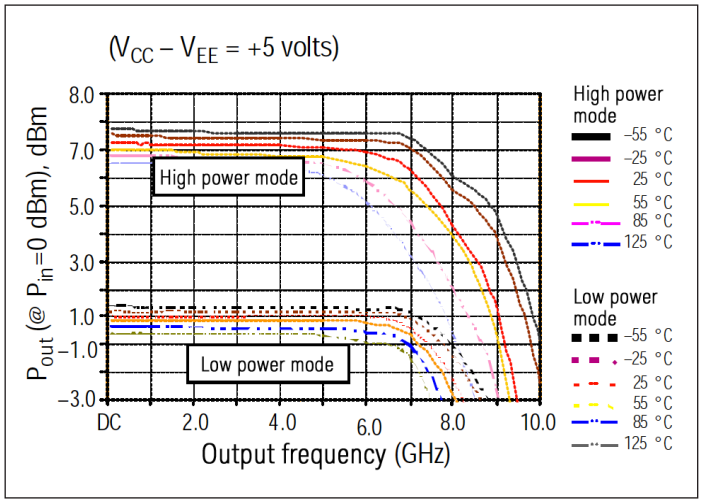


Figure 19. Typical pass–through output power vs. output frequency (over temperature)

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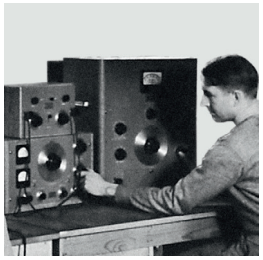

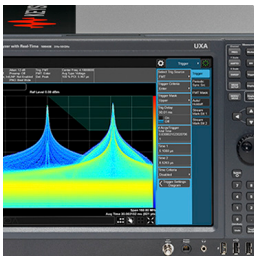

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The product described in this data sheet is RoHS Compliant and RoHS Process Compatible with a maximum temperature of 260 °C and a maximum of 3 temperature cycles.

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