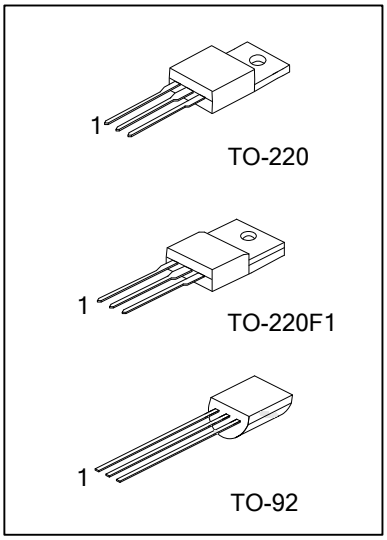
1.3A, 500V N-CHANNEL POWER MOSFET



■ DESCRIPTION

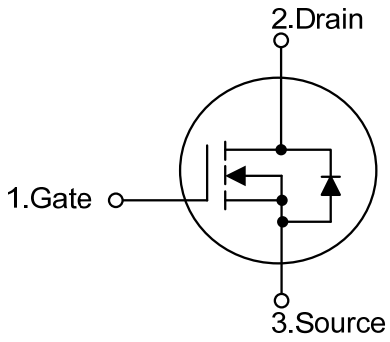
The UTC **1N50** is a N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

The UTC **1N50** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.

■ FEATURES

* $R_{DS(ON)}$=6.0Ω @ V_{GS}=10V
* High Switching Speed
* 100% Avalanche Tested

■ SYMBOL



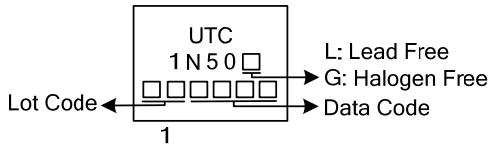
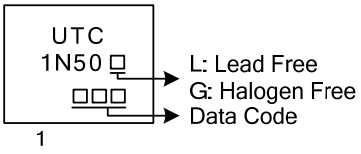
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
1N50L-TA3-T	1N50G-TA3-T	TO-220	G	D	S	Tube
1N50L-TF1-T	1N50G-TF1-T	TO-220F1	G	D	S	Tube
1N50L-92-B	1N50G-T92-B	TO-92	G	D	S	Tape Box
1N50L-92-K	1N50G-T92-K	TO-92	G	D	S	Bulk

Note: Pin Assignment: G: Gate D: Drain S: Source

1N50L-TA3-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube, B: Tape Box, K: Bulk (2) TA3: TO-220, TF1: TO-220F1, T92: TO-92 (3) L: Lead Free, G: Halogen Free and Lead Free

■ MARKING

TO-220 / TO-220F1	TO-92
	

■ ABSOLUTE MAXIMUM RATINGS (T_C=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	±30	V
Drain Current	Continuous (T_C=25°C)	I_D	1.3 (Note 2)	A
	Pulsed (Note 3)	I_{DM}	5 (Note 2)	A
Avalanche Current (Note 3)		I_{AR}	1.3	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	113	mJ
	Repetitive (Note 5)	E_{AR}	2.6	mJ
Power Dissipation	TO-220	P_D	40	W
	TO-220F1		20	W
	TO-92		1.56	W
Derate above 25°C	TO-220		0.32	W/°C
	TO-220F1		0.16	W/°C
	TO-92		0.0125	W/°C
Junction Temperature		T_J	+150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Drain current limited by maximum junction temperature
3. Repetitive Rating: Pulse width limited by maximum junction temperature
4. L = 120mH, I_{AS} = 1.3A, V_{DD} = 50V, R_G = 27Ω, Starting T_J = 25°C
5. I_{SD} ≤ 1.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

■ THERMAL DATA

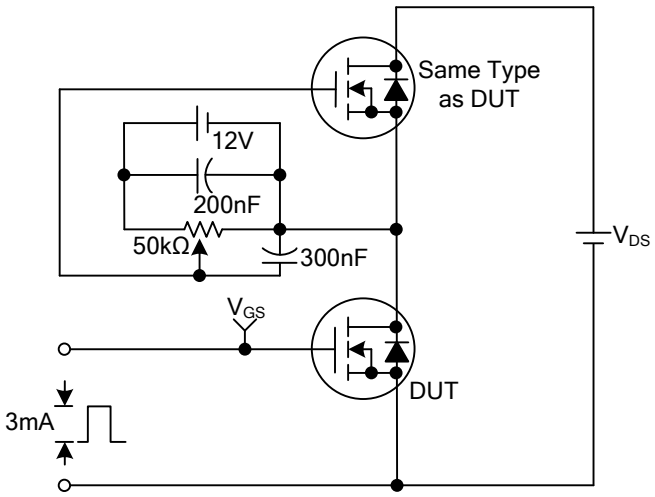
PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-220F1	θ_{JA}	62.5	°C/W
	TO-92		180	°C/W
Junction to Case	TO-220	θ_{JC}	3.13	°C/W
	TO-220F1		6.24	°C/W
	TO-92		80	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

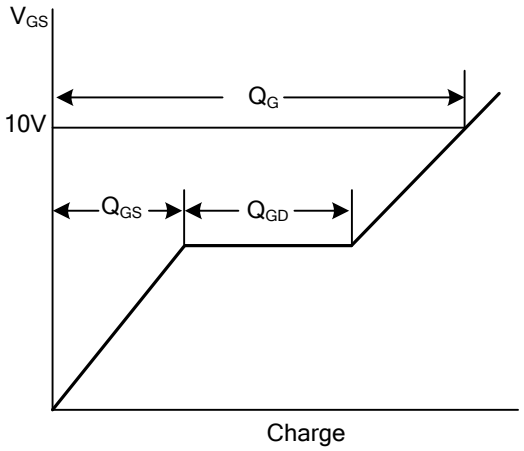
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV_{DSS}	I_D=250μA, V_{GS}=0V	500			V
Drain-Source Leakage Current		I_{DSS}	V_{DS}=500V, V_{GS}=0V			1	μA
Gate- Source Leakage Current	Forward	I_{GSS}	V_{GS}=+30V, V_{DS}=0V			+100	nA
	Reverse		V_{GS}=-30V, V_{DS}=0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static Drain-Source On-State Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=0.65A		4.3	6.0	Ω
DYNAMIC PARAMETERS							
Input Capacitance		C_{ISS}	V_{GS}=0V, V_{DS}=25V, f=1.0MHz		220	290	pF
Output Capacitance		C_{OSS}			30	35	pF
Reverse Transfer Capacitance		C_{RSS}			11	13	pF
SWITCHING PARAMETERS							
Turn-ON Delay Time		$t_{D(ON)}$	V_{DD}=30V, I_D=0.5A, R_G=25Ω (Note 1, 2)		44	50	ns
Rise Time		t_R			31	35	ns
Turn-OFF Delay Time		$t_{D(OFF)}$			58	90	ns
Fall-Time		t_F			22	40	ns
Total Gate Charge		Q_G	V_{GS}=10V, V_{DS}=50V, I_D=1.3A (Note 1, 2)		11	16	nC
Gate to Source Charge		Q_{GS}			3.64		nC
Gate to Drain Charge		Q_{GD}			2		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Body-Diode Continuous Current		I_S				1.3	A
Maximum Body-Diode Pulsed Current		I_{SM}				5	A
Drain-Source Diode Forward Voltage		V_{SD}	I_S=1.3A, V_{GS}=0V			1.15	V

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature

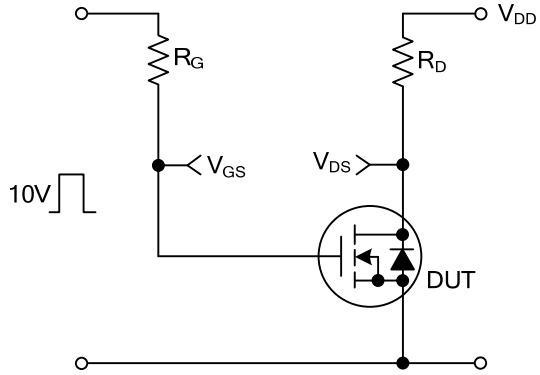
■ TEST CIRCUITS AND WAVEFORMS



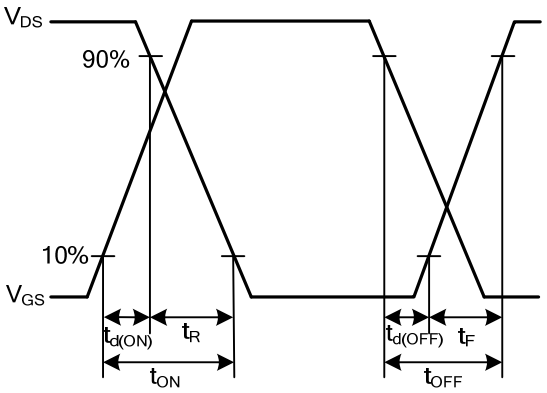
Gate Charge Test Circuit



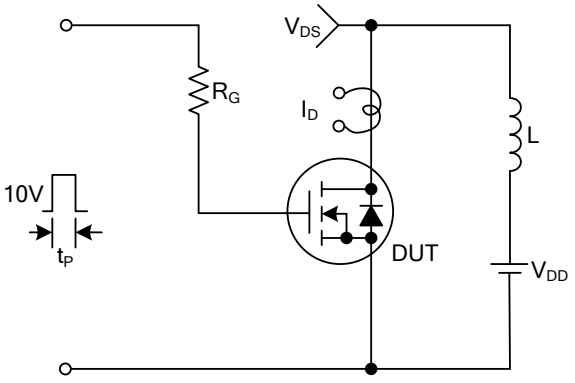
Gate Charge Waveforms



Resistive Switching Test Circuit

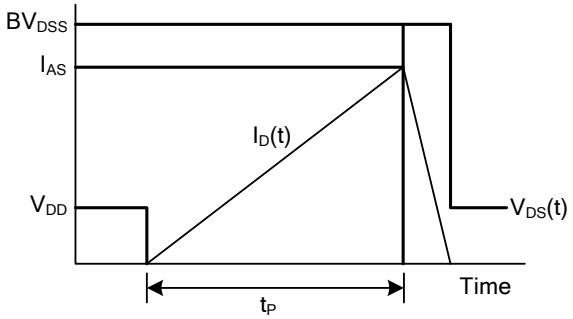


Resistive Switching Waveforms



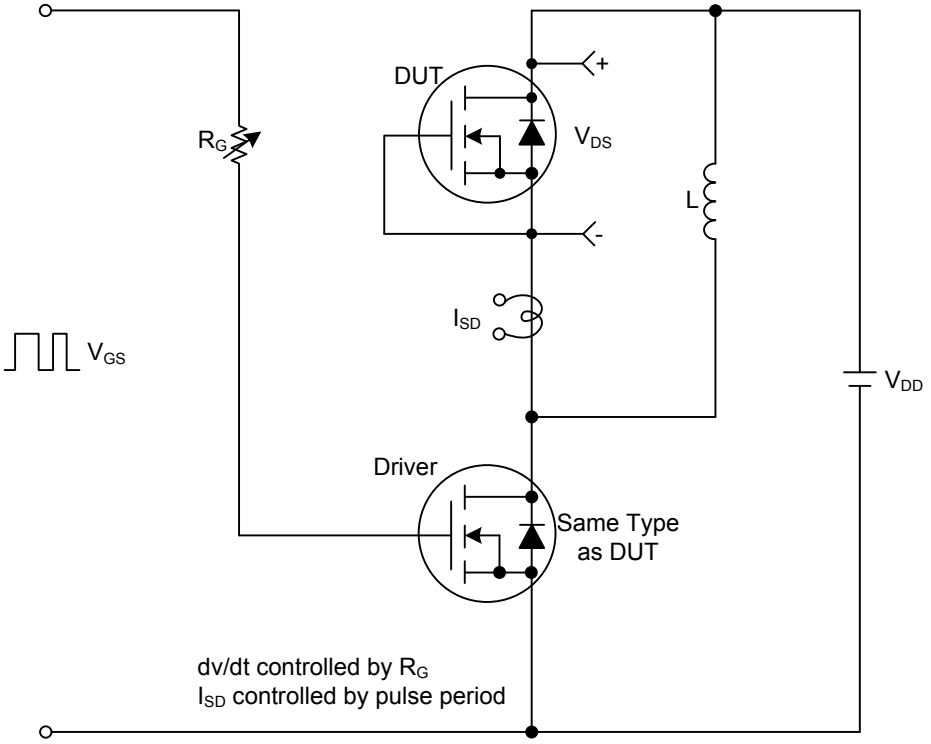
Unclamped Inductive Switching Test Circuit

$$E_{AS}=\frac{1}{2}LI_{AS}^{2}\frac{BV_{DSS}}{BV_{DSS}-V_{DD}}$$



Unclamped Inductive Switching Waveforms

■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms