



1N50A

Preliminary

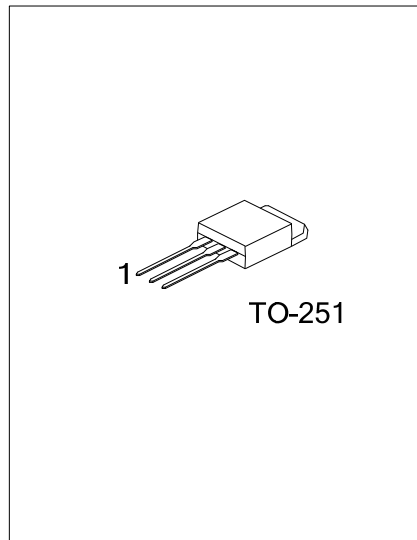
Power MOSFET

1.0A, 500V N-CHANNEL POWER MOSFET

DESCRIPTION

The UTC **1N50A** is an N-channel mode power MOSFET using UTC's advanced technology to provide customers with planar stripe and DMOS technology. This technology allows a minimum on-state resistance and superior switching performance. It also can withstand high energy pulse in the avalanche and commutation mode.

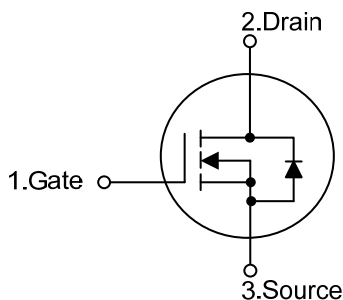
The UTC **1N50A** is generally applied in high efficiency switch mode power supplies, active power factor correction and electronic lamp ballasts based on half bridge topology.



FEATURES

- * $R_{DS(ON)} < 8.0\Omega$ @ $V_{GS}=10V, I_D=0.5A$
- * High Switching Speed
- * 100% Avalanche Tested

SYMBOL



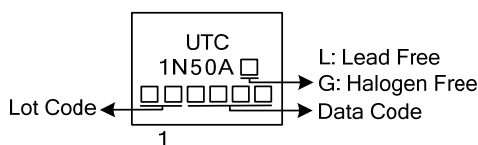
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
1N50AL-TM3-T	1N50AG-TM3-T	TO-251	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>1N50AL-TM3-T</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package 	<ul style="list-style-type: none"> (1) T: Tubel (2) TM3: TO-251 (3) L: Lead Free, G: Halogen Free and Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous ($T_C=25^\circ\text{C}$)	I_D	1 (Note 2)	A
	Pulsed (Note 3)	I_{DM}	4 (Note 2)	A
Avalanche Energy	Single Pulsed (Note 4)	E_{AS}	40	mJ
Power Dissipation		P_D	25	W
Derate above 25°C			0.2	W/ $^\circ\text{C}$
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55~+150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Drain current limited by maximum junction temperature
3. Repetitive Rating: Pulse width limited by maximum junction temperature
4. $L = 80\text{mH}$, $I_{AS} = 1\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 27\Omega$, Starting $T_J = 25^\circ\text{C}$
5. $I_{SD} \leq 1.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	5	$^\circ\text{C}/\text{W}$

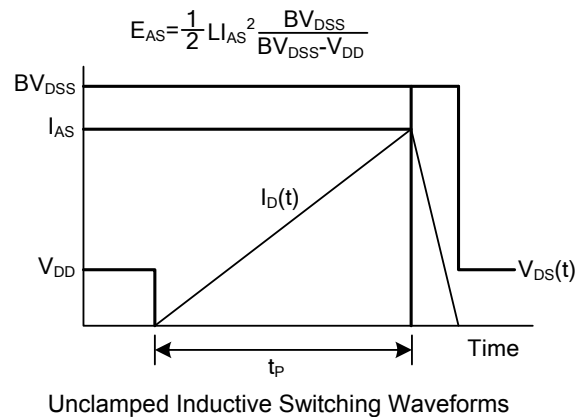
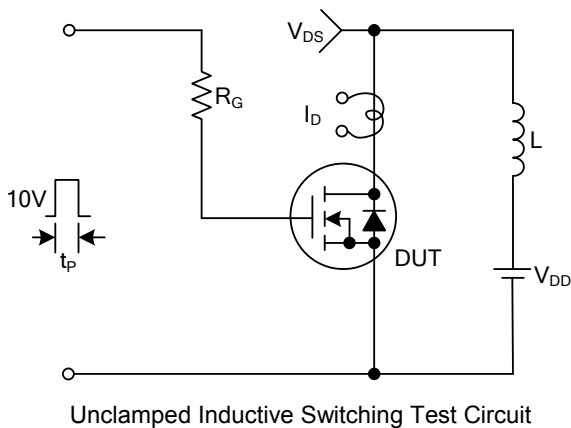
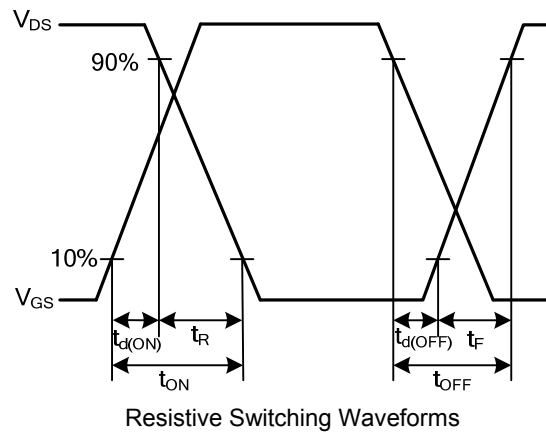
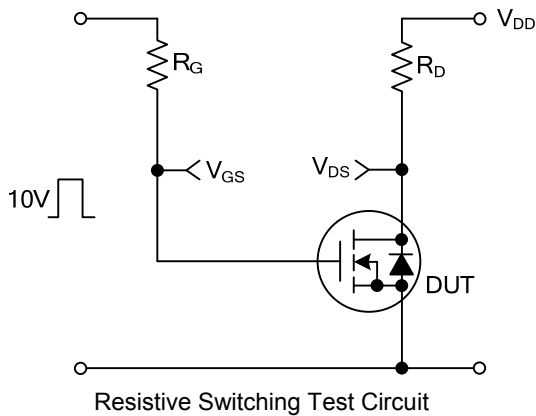
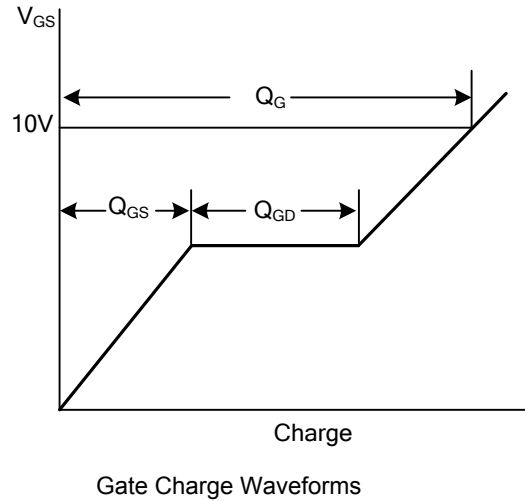
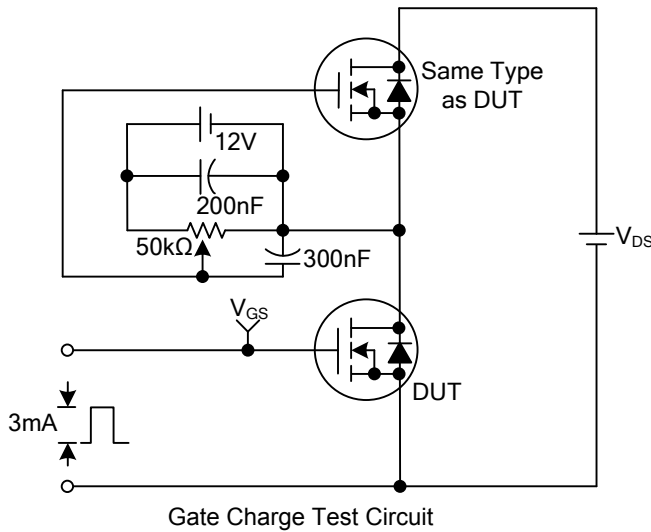
■ ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			1	μA
Gate- Source Leakage Current	I_{GSS}	Forward			+100	nA
		Reverse			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	3.0		5.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=0.5\text{A}$		6.8	8.0	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		125	290	pF
Output Capacitance	C_{OSS}			17	35	pF
Reverse Transfer Capacitance	C_{RSS}			15	20	pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=30\text{V}$, $I_D=0.5\text{A}$, $R_G=25\Omega$ (Note 1, 2)		32	40	ns
Rise Time	t_R			17	35	ns
Turn-OFF Delay Time	$t_{D(OFF)}$			54	70	ns
Fall-Time	t_F			18	32	ns
Total Gate Charge	Q_G	$V_{GS}=10\text{V}$, $V_{DS}=50\text{V}$, $I_D=1.3\text{A}$ (Note 1, 2)		9	15	nC
Gate to Source Charge	Q_{GS}			3		nC
Gate to Drain Charge	Q_{GD}			0.8		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				1	A
Maximum Body-Diode Pulsed Current	I_{SM}				4	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=1\text{A}$, $V_{GS}=0\text{V}$			1.15	V

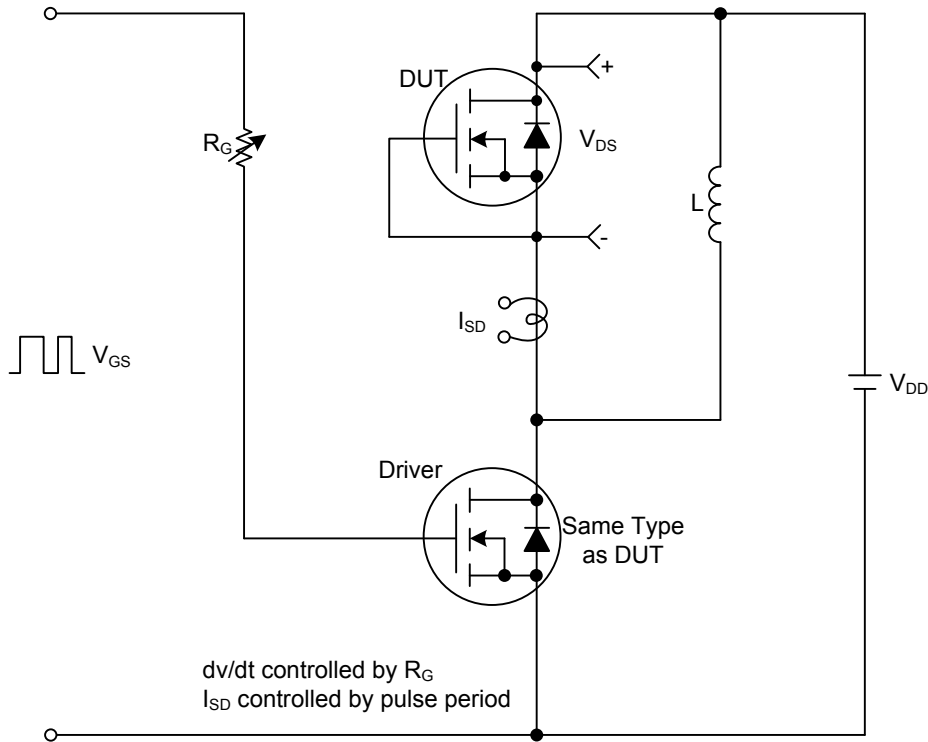
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

2. Essentially independent of operating temperature

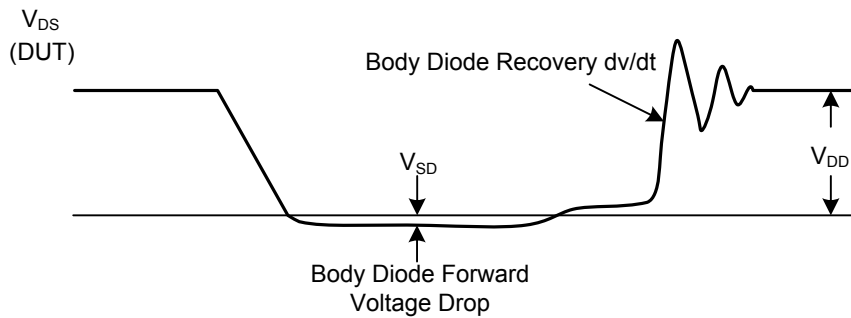
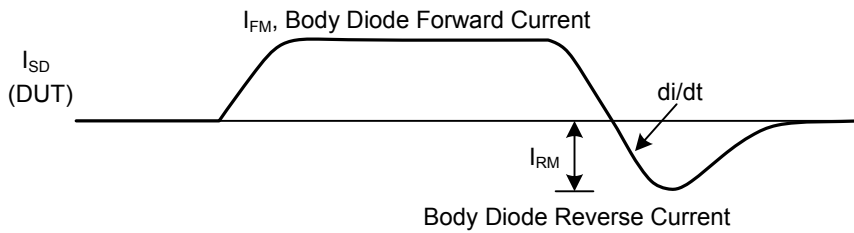
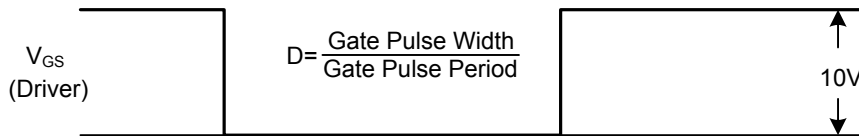
■ TEST CIRCUITS AND WAVEFORMS



■ TEST CIRCUITS AND WAVEFORMS(Cont.)



Peak Diode Recovery dv/dt Test Circuit & Waveforms



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