Silicon Tuning Diodes

1N5148
1N5148A

Designed for electronic tuning and harmonic–generation applications, and provide solid–state reliability to replace mechanical tuning methods.

- Guaranteed High–Frequency Q
- Guaranteed Wide Tuning Range
- Standard 10% Capacitance Tolerance
- Complete Typical Design Curves

6.8 – 47 pF EPICAP VOLTAGE–VARIABLE CAPACITANCE DIODES

CASE 51–02 (DO–204AA)

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	60	Volts
Forward Current	I_F	250	mAdc
RF Power Input(1)	P_{in}	5.0	Watts
Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 2.67	mW mW/°C
Device Dissipation @ T_C = 25°C Derate above 25°C	P_C	2.0 13.3	Watts mW/°C
Junction Temperature	T_J	+175	°C
Storage Temperature Range	T_{stg}	–65 to +200	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	$V_{(BR)R}$	60	70	—	Vdc
Reverse Voltage Leakage Current (V_R = 55 Vdc, T_A = 25°C) (V_R = 55 Vdc, T_A = 150°C)	I_R	— —	— —	0.02 20	μAdc
Series Inductance (f = 250 MHz, L ≈ 1/16″)	L_S	—	4.0	—	nH
Case Capacitance (f = 1.0 MHz, L ≈ 1/16″)	C_C	—	0.17	—	pF
Diode Capacitance Temperature Coefficient (V_R = 4.0 Vdc, f = 1.0 MHz)	TC_C	—	200	—	ppm/°C

1. The RF power input rating assumes that an adequate heatsink is provided.

Device	C_T, Diode Capacitance V_R = 4.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 4.0 Vdc, f = 50 MHz	α V_R = 4.0 Vdc, f = 1.0 MHz		TR, Tuning Ratio C_4/C_{60} f = 1.0 MHz	
	Min	Typ	Max	Min	Min	Typ	Min	Typ
1N5148	42.3	47	51.7	200	0.43	0.45	3.2	3.4
1N5148A	44.7	47	49.3	200	0.43	0.45	3.2	3.4

PARAMETER TEST METHODS

1. L_S, SERIES INDUCTANCE
L_S is measured on a shorted package at 250 MHz using an impedance bridge (Boonton Radio Model 250A RX Meter). L = lead length.

2. C_C, CASE CAPACITANCE
C_C is measured on an open package at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

3. C_T, DIODE CAPACITANCE
($C_T = C_C + C_J$). C_T is measured at 1.0 MHz using a capacitance bridge (Boonton Electronics Model 75A or equivalent).

4. TR, TUNING RATIO
TR is the ratio of C_T measured at 4.0 Vdc divided by C_T measured at 60 Vdc.

5. Q, FIGURE OF MERIT
Q is calculated by taking the G and C readings of an admittance bridge at the specified frequency and substituting in the following equations:

$$Q = \frac{2\pi fC}{G}$$

(Boonton Electronics Model 33AS8).

6. α, DIODE CAPACITANCE REVERSE VOLTAGE SLOPE
The diode capacitance, C_T (as measured at V_R = 4.0 Vdc, f = 1.0 MHz) is compared to C_T (as measured at V_R = 60 Vdc, f = 1.0 MHz) by the following equation which defines α.

$$\alpha = \frac{\log\ C_T(4) - \log\ C_T(60)}{\log\ 60 - \log\ 4}$$

Note that a C_T versus V_R law is assumed as shown in the following equation where C_C is included.

$$C_T = \frac{K}{V\alpha}$$

7. TC_C, DIODE CAPACITANCE TEMPERATURE COEFFICIENT
TC_C is guaranteed by comparing C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = –65°C with C_T at V_R = 4.0 Vdc, f = 1.0 MHz, T_A = +85°C in the following equation which defines TC_C:

$$TC_C = \left| \frac{C_T(+85°C) - C_T(-65°C)}{85 + 65} \right| \cdot \frac{10^6}{C_T(25°C)}$$

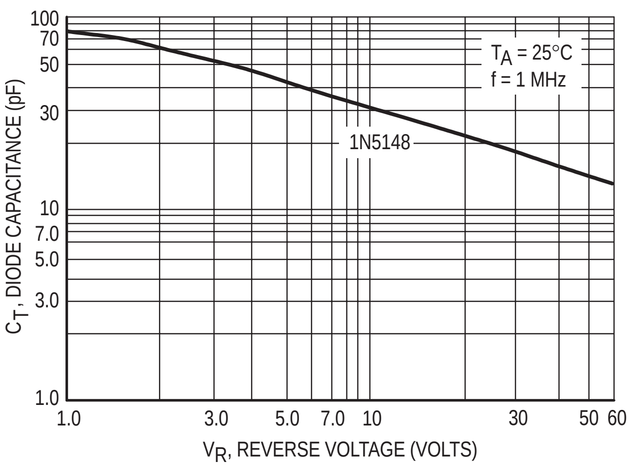

Figure 1. Diode Capacitance versus Reverse Voltage

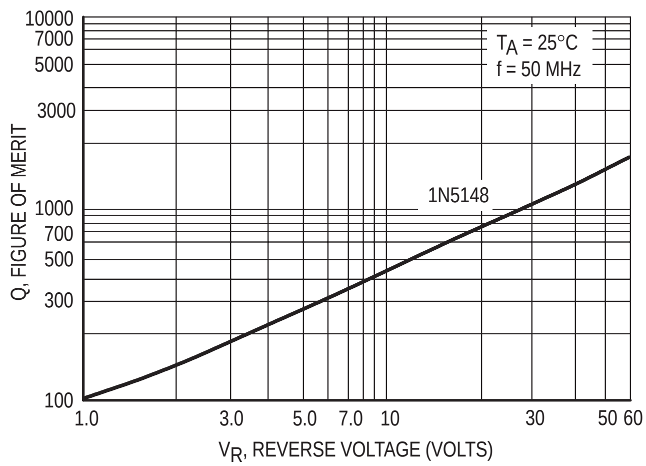

Figure 2. Figure of Merit versus Reverse Voltage

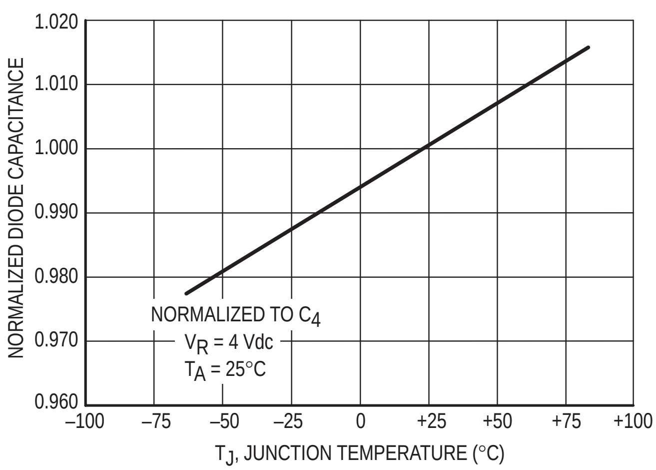

Figure 3. Normalized Diode Capacitance versus Junction Temperature

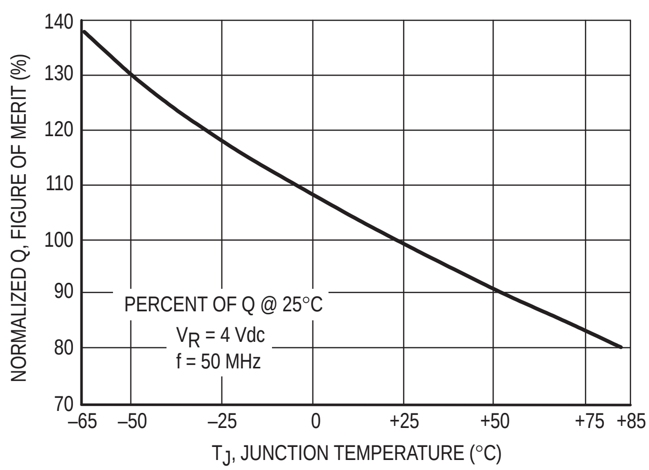

Figure 4. Normalized Figure of Merit versus Junction Temperature

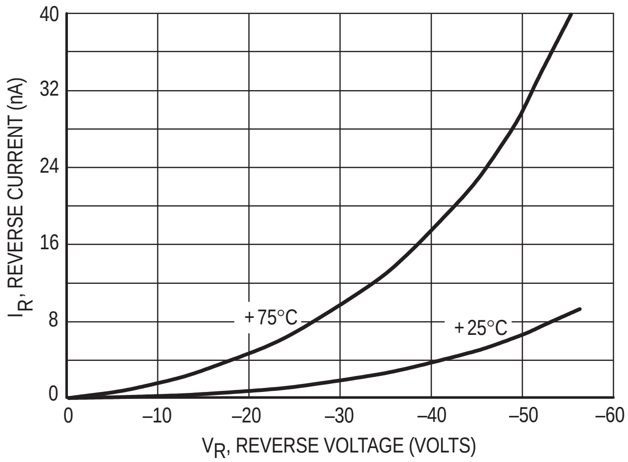

Figure 5. Reverse Current versus Reverse Bias Voltage

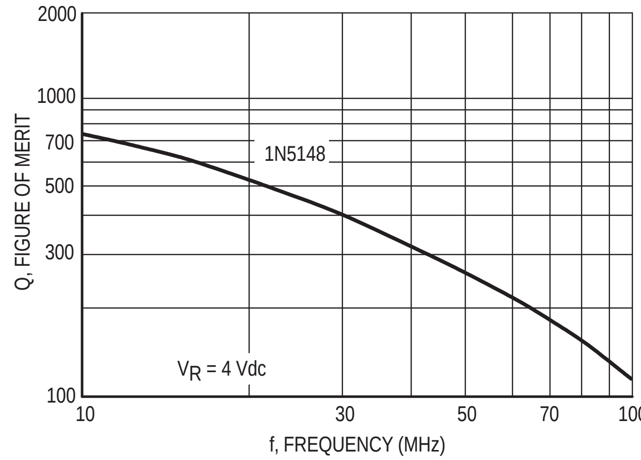

Figure 6. Figure of Merit versus Frequency