MOTOROLA

1N6095
1N6096
SD41

SWITCHMODE POWER RECTIFIERS

. using the Schottky Barrier principle with a platinum barrier metal These state-of-the-art devices have the following features.

- Guardring for Stress Protection
- Low Forward Voltage
- 150°C Operating Junction Temperature Capability
- Guaranteed Reverse Avalanche

SCHOTTKY BARRIER RECTIFIERS

25 and 30 AMPERES
30 to 45 VOLTS

CASE 245
(DO-4)

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MAXIMUM RATINGS

Rating	Symbol	1N6095*	1N6096*	SD41	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	30	40	45	Volts
Average Rectified Forward Current (Rated V_R)	I_O	25 T_C = 70°C	25 T_C = 70°C	30 T_C = 105°C	Amps
Case Temperature (Rated V_R)	T_C	105	105		°C
Nonrepetitive Peak Surge Current (Surge applied at rated load conditions halfwave, single phase, 60 Hz)	I_{FSM}	400	400	600	Amp
Peak Repetitive Reverse Surge Current (2.0 μs, 1.0 kHz) See Figure 10 (1)	I_{RRM}	2.0	2.0	2.0	Amps
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +125	-65 to +125	-55 to +150	°C
Peak Operating Junction Temperature (Forward Current Applied)	$T_{J(pk)}$	150	150	150	°C
Voltage Rate of Change (Rated V_R)	dv/dt	—	—	700	V/μs

THERMAL CHARACTERISTICS

Characteristic	Symbol	1N6095*	1N6096*	SD41	Unit
Maximum Thermal Resistance, Junction to Case	$R_{\theta JC}$	◄	2.0	►	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	1N6095*	1N6096*	SD41	Unit
Maximum Instantaneous Forward Voltage (2) (i_F = 30 Amp, T_C = 125°C) (i_F = 78.5 Amp, T_C = 70°C)	v_F	— 0.86	— 0.86	0.55	Volts
Maximum Instantaneous Reverse Current (2) (Rated dc Voltage, T_C = 125°C)	i_R	250	250	125	mA
Capacitance (100 kHz ≤ f ≤ 1.0 MHz)	C_t	6000 V_R = 1.0 V	6000 V_R = 1.0 V	2000 V_R = 5.0 V	pF

*Indicates JEDEC Registered Data
(1) Not JEDEC requirement, but a Motorola product capability
(2) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%

FIGURE 1 —MAXIMUM FORWARD VOLTAGE

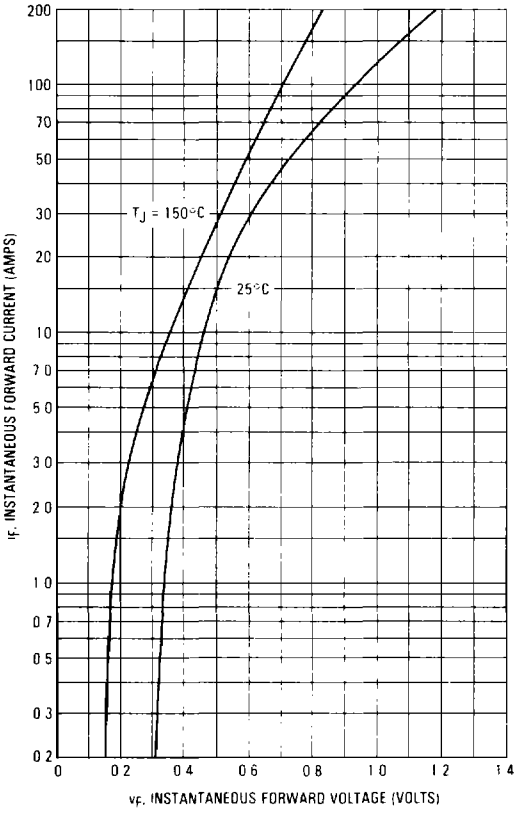

FIGURE 2 — MAXIMUM REVERSE CURRENT

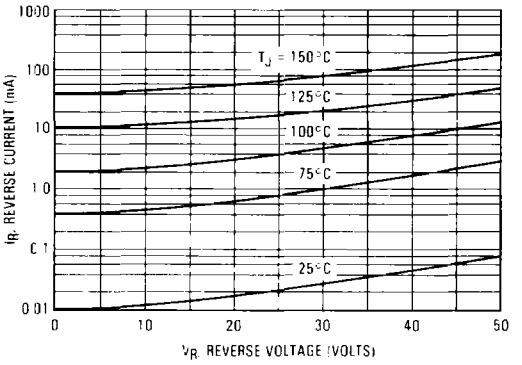

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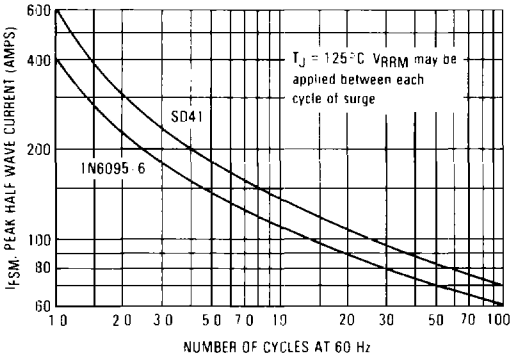
FIGURE 3 — MAXIMUM SURGE CAPABILITY



HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance (See Figure 4.)

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 per cent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficieny is not indicative of power loss; it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage

FIGURE 4 — CAPACITANCE

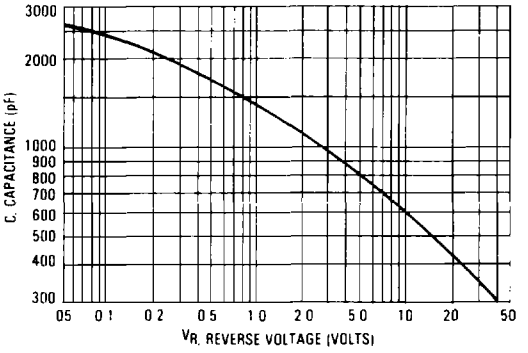


FIGURE 5 — SD41 CURRENT DERATING

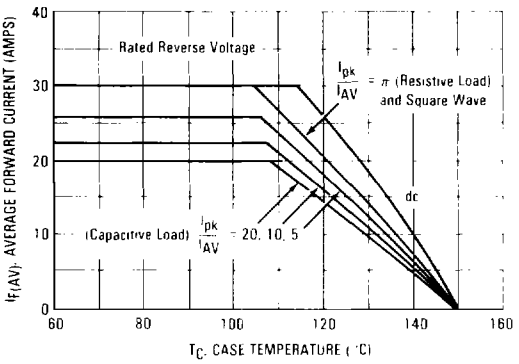


FIGURE 6 — 1N6095/6 CURRENT DERATING

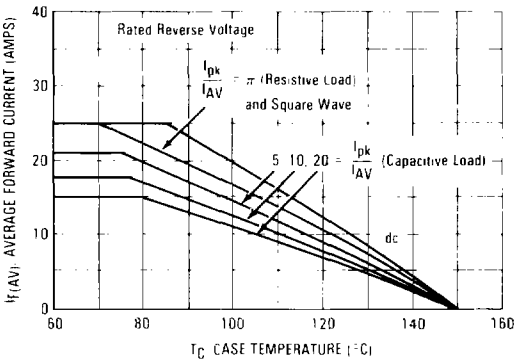


FIGURE 7 — FORWARD POWER DISSIPATION

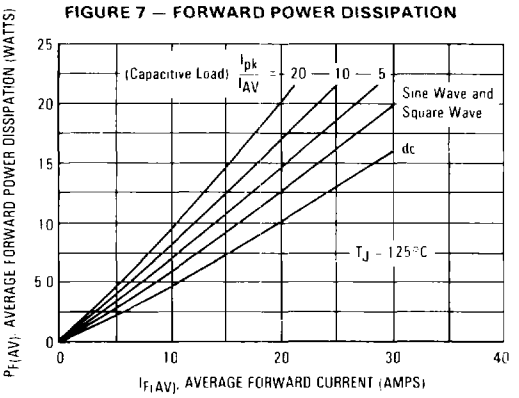


FIGURE 8 — THERMAL RESPONSE

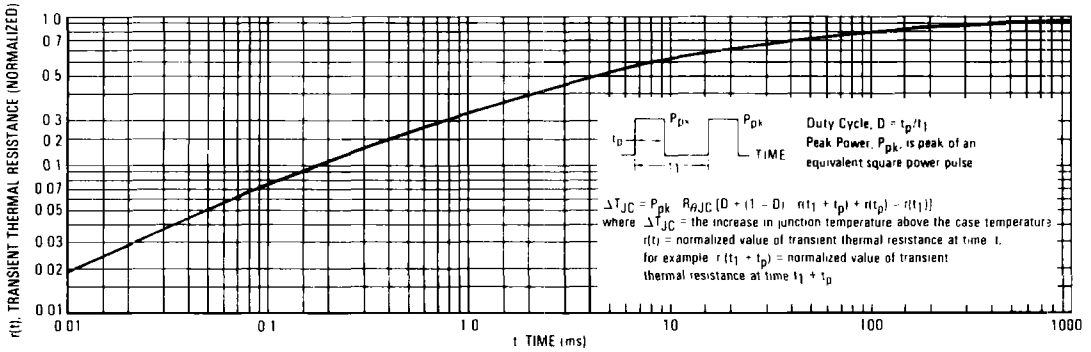
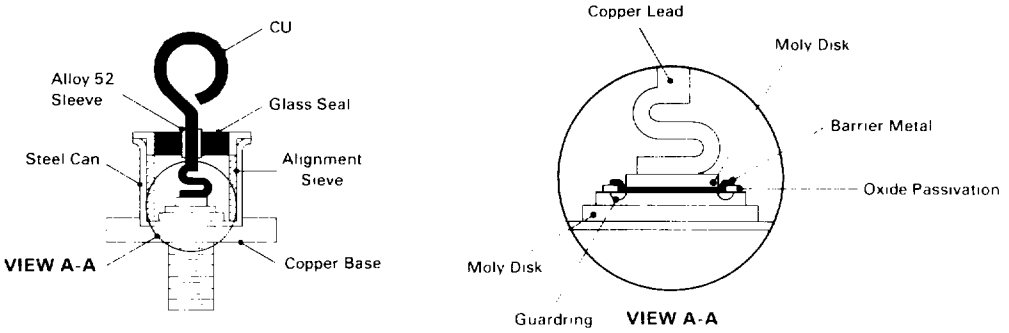


FIGURE 9 — SCHOTTKY RECTIFIER



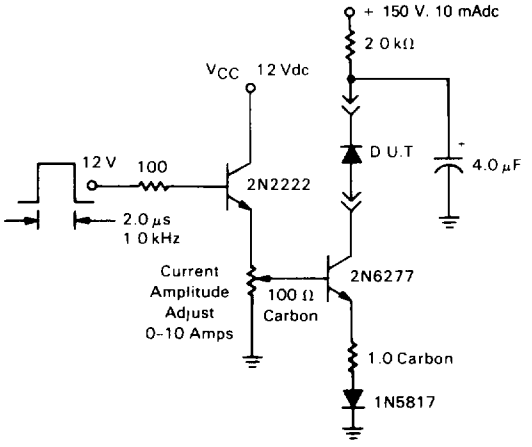
Motorola builds quality and reliability into its Schottky Rectifiers

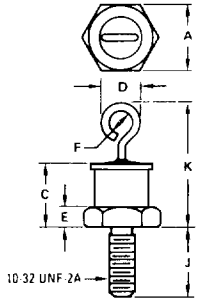
First is the chip, which has an interface metal between the platinum-barrier metal and nickel-gold ohmic-contact metal to eliminate any possible interaction with the barrier. The indicated guardring prevents dv/dt problems, so snubbers are not required. The guardring also operates like a zener to absorb over-voltage transients.

Second is the package. There are molybdenum disks which closely match the thermal coefficient of expansion of silicon on each side of the chip. The top copper lead is also stress-reliefed. These two features give the unit the capability of passing stringent thermal fatigue tests for 5,000 cycles. The top copper lead provides a low resistance to current and therefore does not contribute to device heating; a heat sink should be used when attaching wires.

Third is the redundant electrical testing. The device is tested before assembly in "sandwich" form with the chip between the moly disks. It is tested again after assembly. As part of the final electrical test, devices are 100% tested for dv/dt at 1,600 V/μs and reverse avalanche.

FIGURE 10 — TEST CIRCUIT FOR dv/dt AND REVERSE SURGE CURRENT





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.77	11.10	0.424	0.437
C	–	10.29	–	0.405
D	–	6.35	–	0.250
E	1.91	4.45	0.075	0.175
F	1.52	–	0.060	–
J	10.72	11.51	0.422	0.453
K	–	20.32	–	0.800

CASE 245
(DO-4)
Polarity: Cathode to Case