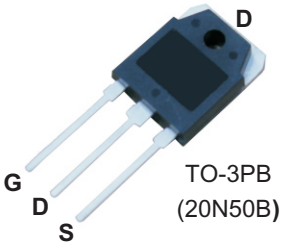
N-Channel Power MOSFET
(20A, 500Volts)

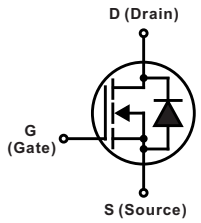
DESCRIPTION

The Nell 2**0N50** is a three-terminal silicon device with current conduction capability of 20A, fast switching speed, low on-state resistance, breakdown voltage rating of 500V, and max. threshold voltage of 5 volts.

They are designed for use in applications such as switched mode power supplies, DC to DC converters, motor control circuits, UPS and general purpose switching applications.



TO-3PB
(20N50B)



FEATURES

- $R_{DS(ON)}$ = 0.23Ω@V_{GS} = 10V
- Ultra low gate charge(60nC max.)
- Low reverse transfer capacitance (C_{RSS} = 27pF typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 150°C operation temperature

PRODUCT SUMMARY	
I_D (A)	20
V_{DSS} (V)	500
$R_{DS(ON)}$ (Ω)	0.23 @ V_{GS} = 10V
Q_G(nC) max.	60

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
V_{DSS}	Drain to Source voltage	T_J=25°C to 150°C	500	V
V_{DGR}	Drain to Gate voltage	R_{GS}=20KΩ	500	
V_{GS}	Gate to Source voltage		±30	
I_D	Continuous Drain Current	T_C=25°C	20	A
		T_C=100°C	12.4	
I_{DM}	Pulsed Drain current(Note 1)		80	
I_{AR}	Avalanche current(Note 1)		20	
E_{AR}	Repetitive avalanche energy(Note 1)	I_{AR}=20A, R_{GS}=50Ω, V_{GS}=10V	25	mJ
dv/dt	Peak diode recovery dv/dt(Note 2)		4.6	V /ns
P_D	Total power dissipation (Derating factor above 25°C)	T_C=25°C	280 (2.3)	W(W/°C)
T_J	Operation junction temperature		-55 to 150	°C
T_{STG}	Storage temperature		-55 to 150	
T_L	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf·in (N·m)

Note: 1.Repetitive rating: pulse width limited by junction temperature.
2.I_{SD} ≤ 20A, di/dt ≤ 200A/μs, V_{DD} ≤ $V_{(BR)DSS}$, starting T_J=25°C.

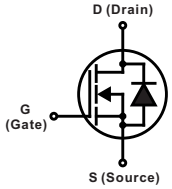
THERMAL RESISTANCE

SYMBOL	PARAMETER		Min.	Typ.	Max.	UNIT
$R_{th(j-c)}$	Thermal resistance, junction to case	TO-3P(B)			0.44	°C/W
$R_{th(c-s)}$	Thermal resistance, case to heatsink			0.5		
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-3P(B)			40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{(BR)DSS}$	Drain to source breakdown voltage	I_D = 250μA, V_{GS} = 0V	500			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	I_D = 250μA, referenced to 25°C		0.5		V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=500V, V_{GS}=0V, T_C = 25°C			25	μA
		V_{DS}=400V, V_{GS}=0V, T_C=150°C			250	
I_{GSS}	Gate to source forward leakage current	V_{GS} = 30V, V_{DS} = 0V			100	nA
	Gate to source reverse leakage current	V_{GS} = -30V, V_{DS} = 0V			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	I_D = 10A, V_{GS} = 10V		0.20	0.23	Ω
$V_{GS(TH)}$	Gate threshold voltage	V_{GS}=V_{DS}, I_D=250μA	3.0		5.0	V
g_{FS}	Forward transconductance	V_{DS}=40V, I_D=10A		24.6		S
C_{ISS}	Input capacitance	V_{DS} = 25V, V_{GS} = 0V, f =1MHz		2400	3120	pF
C_{OSS}	Output capacitance			355	465	
C_{RSS}	Reverse transfer capacitance			27		
$t_{d(ON)}$	Turn-on delay time	V_{DD} = 250V, V_{GS} = 10V, I_D = 20A R_{GS} = 25Ω(Note 1, 2)		95	200	ns
t_r	Rise time			375	760	
$t_{d(OFF)}$	Turn-off delay time			100	210	
t_f	Fall time			105	220	
Q_G	Total gate charge	V_{DD} = 400V, V_{GS} = 10V, I_D = 20A (Note 1, 2)		46	60	nC
Q_{GS}	Gate to source charge			15		
Q_{GD}	Gate to drain charge (Miller charge)			22		
E_{AS}	Single pulse avalanche energy(Note 3)	I_{AS}= 20A, L=5.0mH			1110	mJ

SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
V_{SD}	Diode forward voltage	I_{SD} = 20A, V_{GS} = 0V			1.4	V
Is (I_{SD})	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET			20	A
I_{SM}	Pulsed source current				80	
t_{rr}	Reverse recovery time	I_{SD} = 20A, V_{GS} = 0V, dI_F/dt = 100A/μs		500		ns
Q_{rr}	Reverse recovery charge			7.2		μC

Note: 1. Pulse test: Pulse width ≤ 300μs, duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

3. I_{AS}=20A, V_{DD}=50V, L=5.0mH, R_{GS}= 25Ω, starting T_J=25°C.

ORDERING INFORMATION SCHEME

20 N 50 B

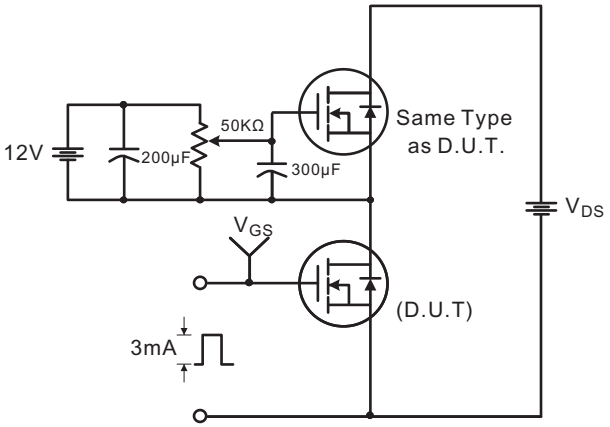
Current rating, I_D
20 = 20A

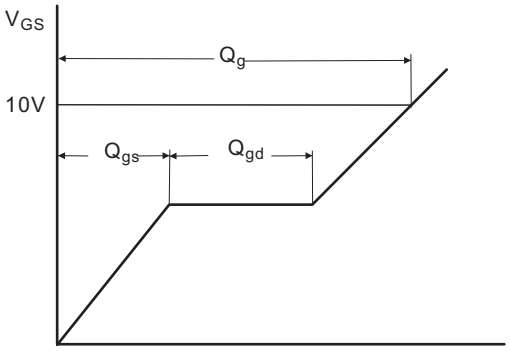
MOSFET series
N = N-Channel

Voltage rating, V_{DS}
50 = 500V

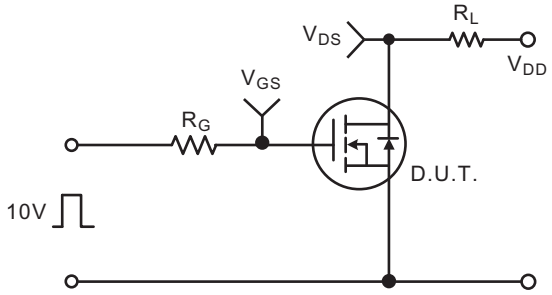
Package type
B = TO-3P(B)

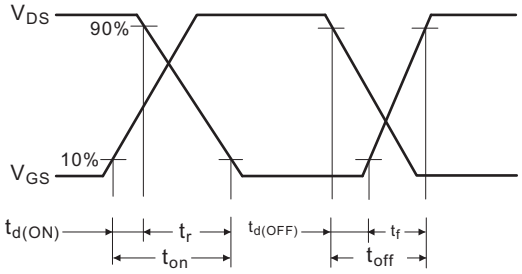
■ Gate charge test circuit & waveform



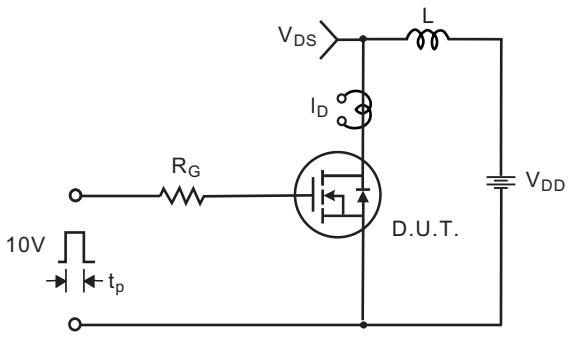


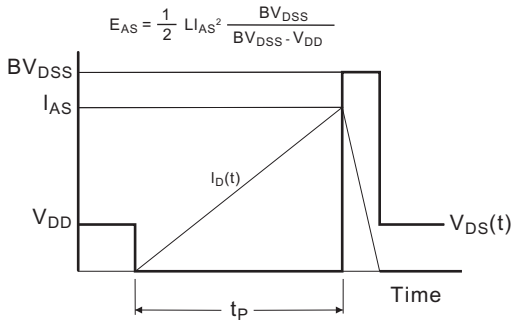
■ RESISTIVE SWITCHING TEST CIRCUIT & WAVEFORM



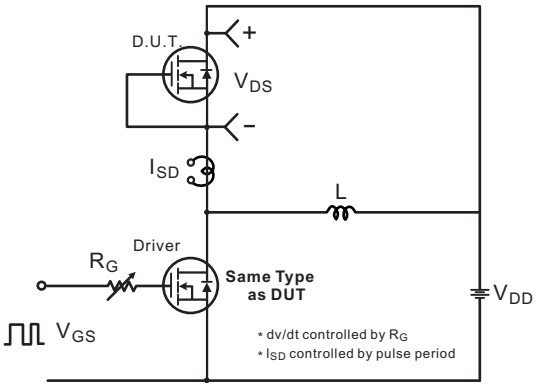


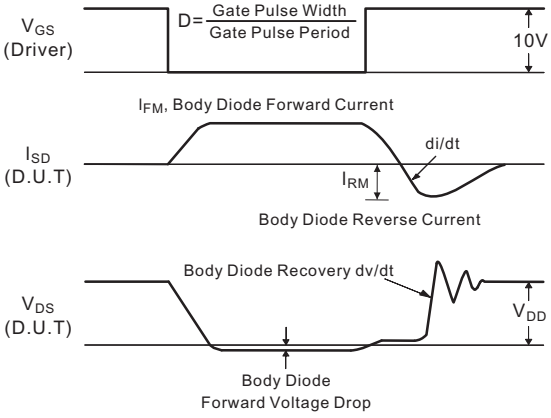
■ UNCLAMPED INDUCTIVE SWITCHING & WAVEFORMS





■ PEAK DIODE RECOVERY dv/dt TEST CIRCUIT & WAVEFORMS





■ TYPICAL CHARACTERISTICS

Fig.1 On-State characteristics

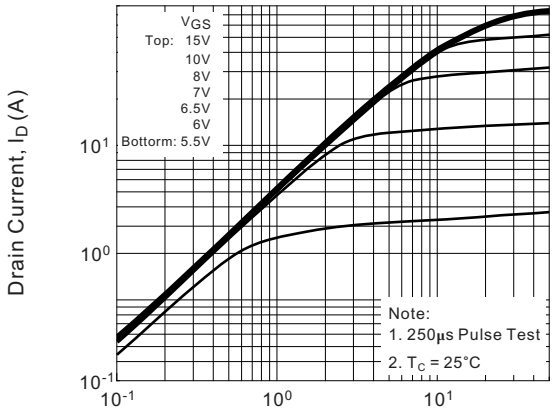


Fig.2 Transfer characteristics

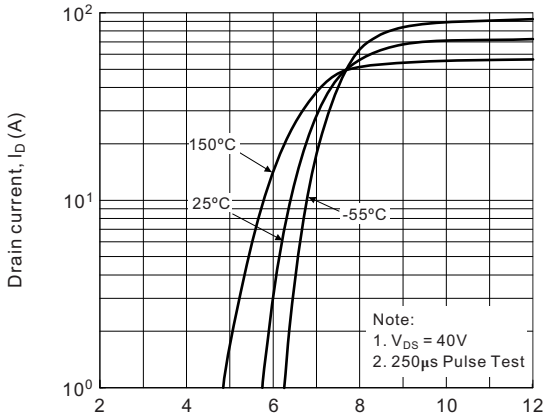


Fig.3 On-Resistance variation vs. drain current and gate voltage

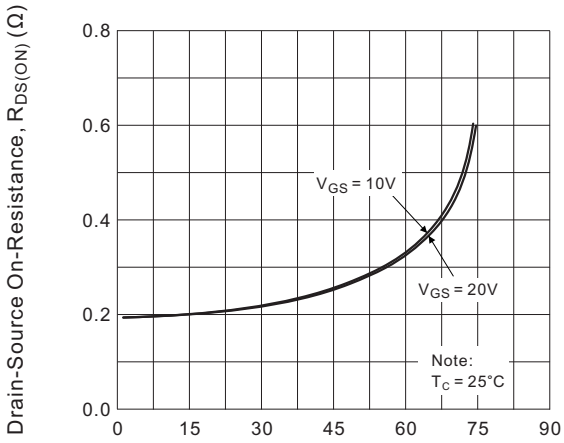


Fig.4 Body diode forward voltage variation vs. Source current and Temperatue

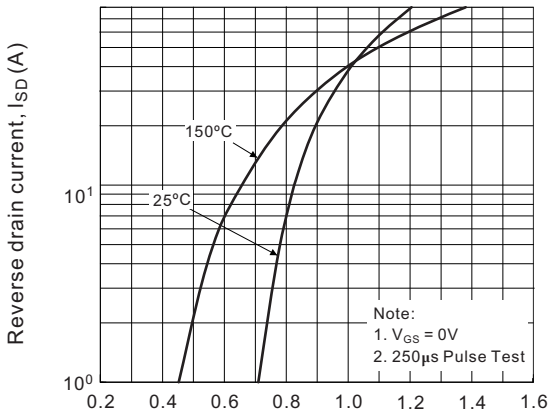


Fig.5 Capacitance characteristics

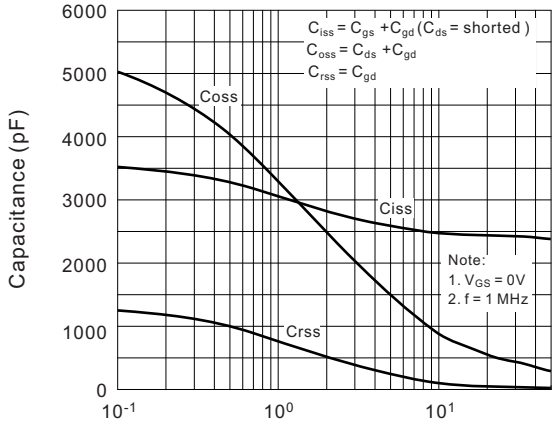


Fig.6 Gate charge characteristics

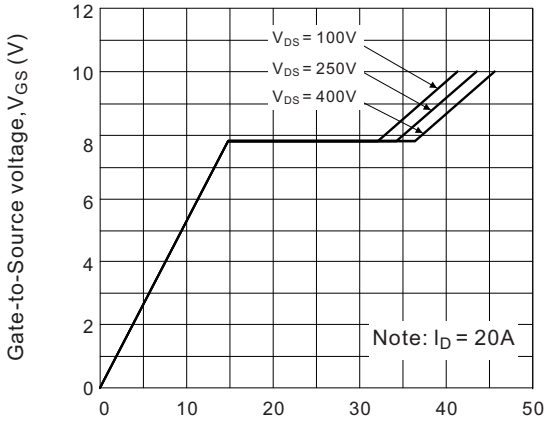


Fig.7 Breakdown voltage variation vs. Temperature

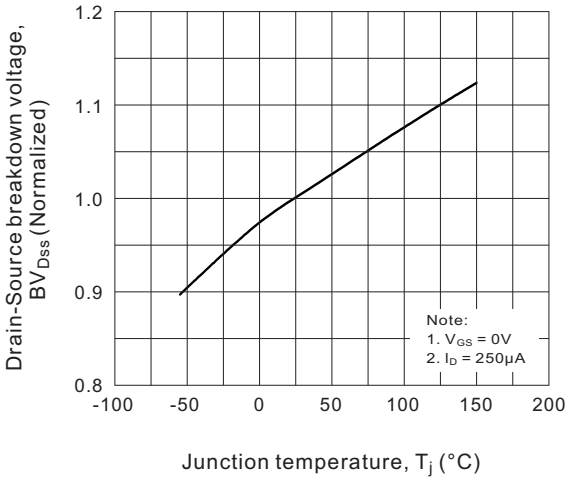


Fig.8 On-Resistance variation vs. Temperature

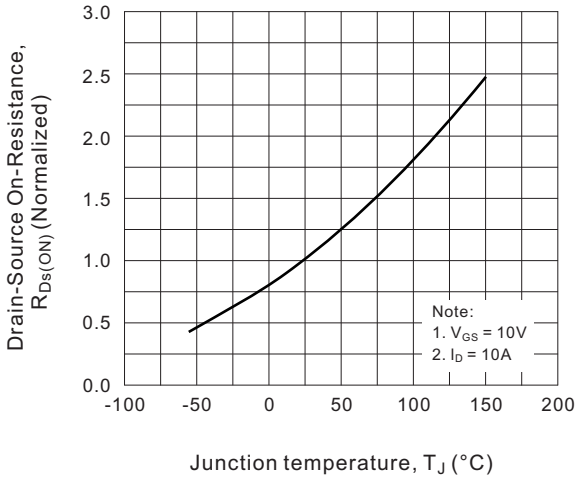


Fig.9 Maximum safe operating area

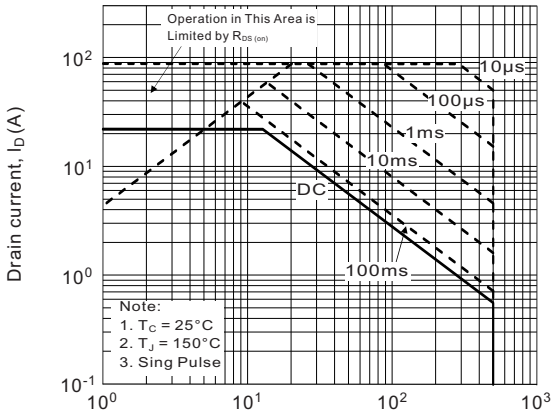


Fig.10 Maximum drain current vs. Case temperature

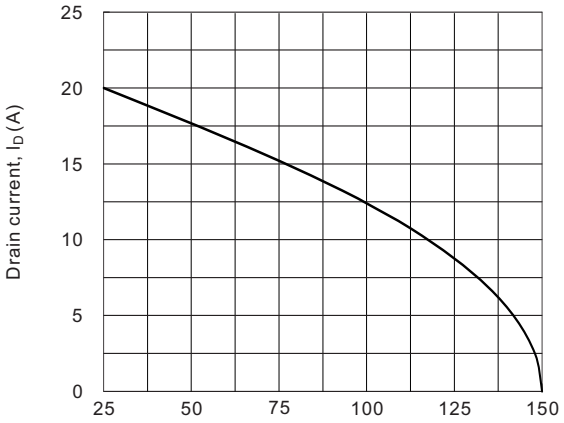
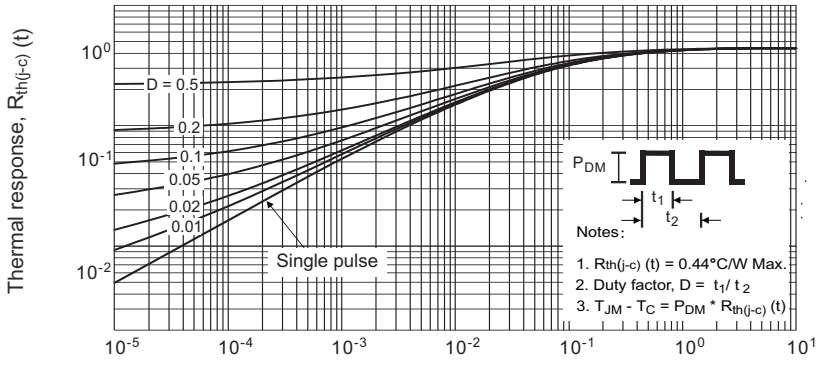
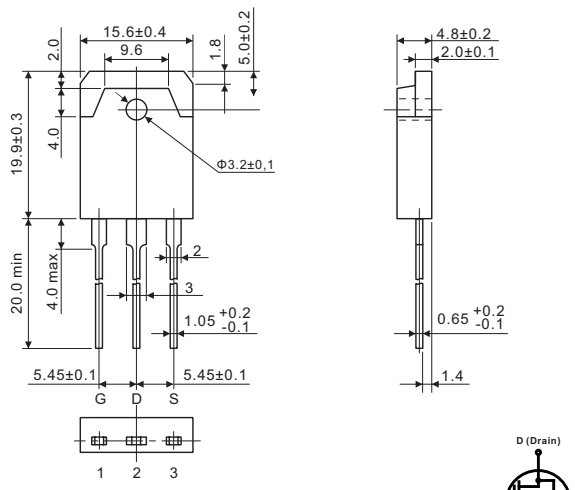


Fig.11 Transient thermal response curve



Case Style

TO-3PB



All dimensions in millimeters(inches)