21555 Non-Transparent PCI-to-PCI Bridge

Specification Update

December 2002

Notice: The 21555 may contain design defects or errors known as errata. Characterized errata that may cause the 21555's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278337-008

Contents

Revision History

Date	Version	Description
12/19/02	008	The following changes have been made to this document: • 21555 bridge steppings have changed to A3. Markings have been updated as well. See "Markings" on page 11. • Added related document to "Affected Documents/Related Documents" on page 7. • Status for Errata 1 and 2 are changed to Fixed. See "Errata" on page 9. • Specification change - 21555 bridge PCI compliancy now at Version 2.3. See "Specification Changes" on page 9. • Documentation changes - Data sheet and User Manual include 2.3 compliance information. See "Added Section 3.1.1 PCI Local Bus Compliance" on page 22. and "Change to Tables 61 and 62 in Section 16.5.2" on page 22.
6/12/02	007	Added Errata 2.
4/12/02	006	Added Errata 1.
6/11/01	005	Corrected PBGA package description from 2-layer to 4-layer within this document.
6/7/01	004	Documentation changes: (See page 9) • Replaced last row of Table 2-3. See Section 14 on Page 21. • Changed l_stat description in Section 11-5. See Section 15 on Page 22.
5/24/01	003	Documentation changes: (See page 8) • Added Markings Table on page 11. • Insert reference to 21554 for improved accuracy. See Section 3 on Page 16. • Remove misplaced sections from Chapter 4. See Section 4 on Page 17. • Remove unnecessary parenthetical phrase. See Section 5 on Page 19. • Change **p_clk** and **s_clk** signal description. See Section 6 on Page 19. • Remove incorrect sentence from Hot Swap input pin description. See Section 7 on Page 19. • Change or remove three (3) references to the 21554. See Section 8 on Page 19. • Update D7:D6 byte offset descriptions. See Section 9 on Page 20. • Remove three references to CLS=4. See Section 10 on Page 20. • Additional information about JTAG pin termination requirements. See Section 11 on Page 20. • Emphasize special handling of the JTAG **tms** signal for Hot insertion applications.See Section 12 on Page 20. • Changed Section 12.2.1 and JTAG description. See Section 13 on Page 21.
9/15/00	002	Added specification change to PBGA package dimensions for coplanarity maximum value.
2/21/00	001	This new Specification Update document contains: • One Specification Change that announces coplanarity value changes. Two Documentation changes that: • Correct the JTAG timing specifications. • Correct the coplanarity values in the datasheet document.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
21555 Non-Transparent PCI-to-PCI Bridge Advance Information Datasheet (specification)	278320
21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual	278321
21555AA/BA and 21555AB/BB Differences Application Note	278669

Nomenclature

Errata are design defects or errors. These may cause the 21555's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the **21555 Non-Transparent PCI-to-PCI Bridge** product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark)	
or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings		Page	Status	ERRATA
	A2	A3			
1.	X		12	Fixed	"21555AA/BA boundary Scan Implementation is not compliant with IEEE 1149.1"
2.	X		13	Fixed	"21555AA/BA I2O Circuitry Will Not Work Asynchronously"

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	A2	A3			
1	X	X	14	Doc change	PBGA Package Dimensions for coplanarity changed from maximum value 0.15 mm to maximum value 0.2 mm.
2		X	14	Doc change	PCI 2.3 Compliance

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	DOCUMENTATION CHANGES
1	278320-001	16	Datasheet "Section 3.4.6: JTAG Timing Specifications"
2	278320-001	16	Datasheet "Section 4.0, Table 16, 304-Point 4-Layer PBGA Package Dimensions"
3	278321-001	16	User's Manual: "Add a Specific Reference to 21554 to first Introduction Paragraph"
4	278321-001	17	User's Manual: "Remove Sections 4.2 through 4.2.4 to Section 2.3.4"
5	278321-001	19	User's Manual: "Remove unnecessary parenthetical phrase from ROM Interface Signal description"
6	278321-001	19	User's Manual: "Table 10-1 p_clk and s_clk descriptions need correction and updating"
7	278321-001	19	User's Manual:"Section 11.2.1, Hot Insertion Input Pin Description Change"
8	278321-001	19	User's Manual: "Remove or change 3 incorrect references to the 21554"
9	278321-001	20	User's Manual: "Section 16.1Byte Offset of D7:D6 needs updating"

Documentation Changes

10	278321-001	20	User's Manual: "Remove reference to CLS=4"
11	278321-001	20	User's Manual: "JTAG Action during Hot insertion"
12	278321-001	20	User's Manual: "Internal and External Signal Terminations"
13	278321-001	21	User's Manual: "Change to Initialization Section 12.2.1 and JTAG Description"
14	278321-001	21	User's Manual: "Change to Chapter 2, Table 2-3 p_req64_l description"
15	278321-001	22	User's Manual: "Change to Section 11.5 l_stat pin description"
16	278320-001	22	Data sheet: "Added Section 3.1.1 PCI Local Bus Compliance"
16	278321-001	22	User's Manual: "Change to Tables 61 and 62 in Section 16.5.2"

Identification Information

Markings

Package Markings	REV_ID Register Value[1]	Speed (MHz)	Stepping
Intel FW21555AA	02h	33	A2
Intel FW21555BA	02h	66	A2
Intel FW21555AB	03h	33	A3
Intel FW21555BB	03h	66	A3

1. Identified in a PCI system by reading the value in the REV_ID register.

Errata

1. 21555AA/BA boundary Scan Implementation is not compliant with IEEE 1149.1

Problem: There is a one cycle delay before valid BSDL data is pushed out to the pins. The problem is due to an incorrect inversion in the equation that generates the JTAG update.

Implication: The parallel output data from any bi-directional pins, purely output pins or control cells, will be driven out exactly one clock after the UPDATE state. This is in violation of the IEEE1149.1 Specification.

Workaround: Although the 21555 JTAG implementation is non-compliant, it may still be usable for test purposes if the following considerations are understood:

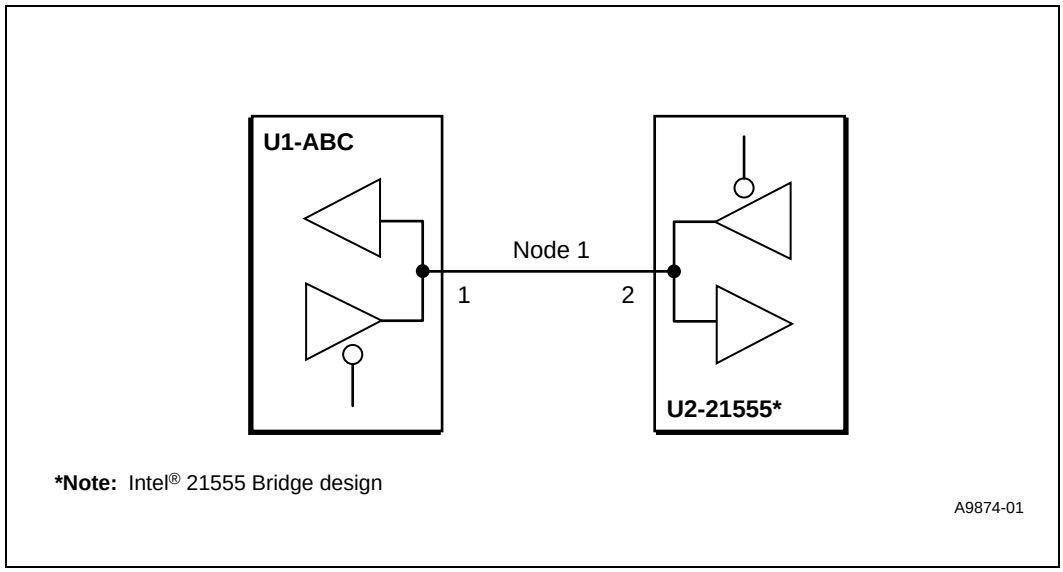
Workaround 1: In-Circuit testers should test for the parallel output data to be on the pins of the chip, at least one clock after the UPDATE state. Typically Automated Test Pattern Generator (ATPG) test vectors will test for this state upon exiting the UPDATE state. This test should be delayed one clock from the ATPG vectors. Also, In-Circuit testers should ensure that data is driven onto pins of the 21555, one clock after UPDATE, to avoid any potential of back driving a pin.

Workaround 2: Standalone boundary scan testers and In-Circuit testers performing chained boundary scan tests, should understand that the Parallel Output UPDATE data, being delayed by one clock, may cause bus contention and back driving during that one clock period, assuming the vectors change bus driving sources in one vector. This is because in chained boundary scan tests, all components execute TAP instructions in Parallel (or lock step), and vector generation algorithms optimize the number of vectors.

To understand the potential issue in detail, refer to the diagram below. Node 1 is a bi-directional node, with U1.1 and U2.2 connected as shown. Assuming that U1 is an IEEE1149.1 compliant device, that U2 is the 21555, and that the control cells of the 21555 were set during the vectors to enable the driver of U2.2 to drive to U1.1 (receiver). When switching drivers from U2 to U1, U2 should tri-state its driver prior to, or at the same time as, U1 enables its driver. Since the 21555 UPDATES its Parallel Outputs one clock late and the control cells which enable U2's drivers are Parallel Outputs which again updates one clock cycle late then U2.2, which will be driving at the same time U1.1 is driving. This contention will happen for one TCK cycle, until U2 UPDATES its parallel outputs. The period of this contention is dependent on the TCK frequency rate.

A remedy to the 21555's late UPDATE is to ensure the chained Boundary Scan tester's vectors do not switch bus driver directions in one vector. This means that one vector should disable U2's driver, and the next vector should enable U1's driver. ATPG vectors typically are not manually manageable in this way and this requirement may force an engineer's manual intervention. No single stepping of test clock through the TAP State Machine should be allowed with the 21555 in the boundary scan chain. The resulting contention would increase the potential back drive time, increasing the possibility of device damage.

Figure 1. Node Boundary



Status: Fixed.This behavior has been corrected in the 21555AB/BB Step A3 device.

2. 21555AA/BA I²O Circuitry Will Not Work Asynchronously

Problem: The I^2O circuitry does not function properly in asynchronous mode.

The root cause of this problem is the synchronization logic between the primary and secondary clock domains - they are incorrectly wired.

Implication: The I^2O circuitry will not function in asynchronous mode and can hang the system.

Workaround: There is no workaround for applications that require asynchronous operation of the I^2O circuitry. Although the 21555 I^2O circuitry is improperly implemented for asynchronous operation, the device will work properly in synchronous mode.

Status: Fixed. This behavior has been corrected in the 21555AB/BB Step A3 device.

Note: No changes were made to the BSDL file when correcting this problem.

Specification Changes

1. PBGA Package Dimensions for coplanarity changed from maximum value 0.15 mm to maximum value 0.2 mm.

Per PCN notification 961, the 304-point 4-layer PBGA package dimensions for symbol aaa, coplanarity, are changed from maximum value 0.15 mm to maximum value 0.2 mm.

2. PCI 2.3 Compliance

The PCI Special Interest Group ratified the PCI version 2.3 specification. To meet new requirements, an additional bit was added in the Command Register and an additional bit added in the Status Register of the 21555 bridge. The new register bits information is presented in the "Documentation Changes" section of this Specification Update.

Specification Clarifications

1. None for this revision of this specification update.

Documentation Changes

1. Section 3.4.6: JTAG Timing Specifications

Table 1 has been updated and now appears as follows:

Table 1. JTAG Timing Specifications

Symbol	Parameter	Minimum	Maximum	Unit
T_{jr}	tck frequency	0	5	MHz
T_{jp}	tck period	200	∞	ns
T_{ght}	tck high time	100	—	ns
T_{glt}	tck low time	100	—	ns
T_{jrt}	tck rise time[1]	—	10	ns
T_{gft}	tck fall time[2]	—	10	ns
T_{js}	tdi, tms setup time to tck rising edge	10	—	ns
T_{jh}	tdi, tms hold time from tck rising edge	25	—	ns
T_{jd}	tdo valid delay from tck falling edge[3]	—	30	ns
T_{jfd}	tdo float delay from tck falling edge	—	30	ns

1. Measured between 0.8 V and 2.0 V.
2. Measured between 2.0 V and 0.8 V.
3. C_1=50 pF.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information Datasheet (278320).*

2. Section 4.0, Table 16, 304-Point 4-Layer PBGA Package Dimensions

Issue: The maximum value for symbol aaa, dimension coplanarity, has been changed from 0.15 mm to a value of 0.2 mm.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information Datasheet (278320).*

3. Add a Specific Reference to 21554 to first Introduction Paragraph

Issue: Refer to Chapter 1, Page 1-1, first paragraph, third sentence, first clause: change:
"A related peripheral device, " to say "The 21554, a related peripheral device, has a 64-bit primary interface,".
The entire paragraph should appear as follows: "Intel's 21555 is a PCI peripheral device that performs PCI bridging functions for embedded and intelligent I/O applications. The 21555 has a 64-bit primary interface, a 64-bit secondary interface, and 66-MHz capability. The 21554 a related PCI peripheral device, has a 64-bit primary interface, a 64-bit secondary interface, and 33-MHz capability."

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

4. Remove Sections 4.2 through 4.2.4 to Section 2.3.4

Issue: Remove these sections:

4.2 64-Bit Operation

The 21555 provides 64-bit extension support on the primary and secondary interfaces. Both 64-bit and 32-bit operation are supported on both interfaces.

This section describes how to use the 64-bit extensions. It describes the conditions under which a transaction can be treated as a 64-bit transaction and includes information about how the transaction is forwarded.

4.2.1 Address Phase of 64-Bit Transactions

When a transaction using the primary bus 64-bit extension is a single address cycle (SAC)—that is, the address falls below the 4GB boundary, and the upper 32 bits of the address are assumed to be zero—**AD<63:32>** and **C/BE#<7:4>** are not defined but are driven to valid logic level during the address phase.

When the transaction is a dual address cycle (DAC), that is, the address falls above the 4GB boundary and the upper 32 bits of the address are non-zero, signals **AD<63:32>** contain the upper 32 bits of the address for both address phases. Signals **C/BE#<7:4>** contain the memory bus command during both address phases. A 64-bit target then has the opportunity to decode the entire 64-bit address and bus command after the first address phase. A 32-bit target needs both address phases to decode the full address and bus command.

4.2.2 Data Phase of 64-Bit Transactions

During memory write transactions, when the 21555 has driven **REQ64#** to indicate it is initiating a 64-bit transfer, the 21555 drives the following during the data phase:

- The low 32 bits of data on **AD<31:0>**
- The low four byte enable bits on **C/BE#<3:0>**
- The high 32 bits of data on **AD<63:32>**
- The high four byte enable bits on **C/BE#<7:4>**

When the 21555 detects **ACK64#** asserted by the target at the same time that it detects **DEVSEL#** asserted, every data phase then consists of 64 bits and eight byte enable bits.

For write transactions, when the 21555 does not detect **ACK64#** asserted at the same time that it detects **DEVSEL#** asserted, the 21555 redirects the write data that it has on the **AD<63:32>** bus to **AD<31:0>** during the second data phase. Similarly, the upper four byte enable bits are redirected to **C/BE#<3:0>** during the second data phase. All data phases then consist of 32 bits.

For 64-bit memory write transactions that end at an odd Dword boundary, the 21555 drives the byte enable bits to 1 during the last data phase. Signals **AD<63:32>** are then unpredictable but are driven to a valid logic level.

For read transactions, when the 21555 has asserted **REQ64#,** it drives 8 bits of byte enables on **C/BE#<7:0>**. Since the only read transactions that use the 64-bit extension are prefetchable memory read transactions, the byte enable bits are always zero. Therefore, no special redirection is needed based on the target's assertion or lack of assertion of **ACK64#**. When the target asserts **ACK64#** at the same time that it asserts **DEVSEL#**, all read data transfers then consist of 64 bits and the target drives **PAR64**, which covers **AD<63:32>** and **C/BE#<7:4>**. When the target does not assert **ACK64#** when it asserts **DEVSEL#**, all data phases then consist of 32 bits.

4.2.3 64-Bit Transactions Received by the 21555

When the 21555 is the target of a transaction and the 21555 detects **REQ64#** asserted during a memory transaction to be forwarded across the bridge, the 21555 either asserts **ACK64#** at the same time that it asserts **DEVSEL#** to indicate its ability to perform 64-bit data transfers. Under certain circumstances, the 21555 does not use the 64-bit extension as a target and therefore does not assert **ACK64#**.

The 21555 does not assert **ACK64#** when any of the following is true:

- Signal **REQ64#** was not asserted by the initiator.
- The 21555 is responding to a non-prefetchable memory read transaction.
- The 21555 is responding to an I/O transaction.
- The 21555 is responding to a configuration transaction.
- Only 1 Dword of data was read from the target.

When the 21555 is the target of a 64-bit memory write transaction, it is able to accept 64 bits of data during each data phase.

When the 21555 is the target of a 64-bit prefetchable memory read transaction, it supplies 64 bits of read data during each data phase and drives **PAR64** corresponding to **AD<63:32>** and **C/BE#<7:4>**, for each data phase. When an odd number of Dwords was read from the target and the 21555 has asserted **ACK64#** when returning read data to the initiator, the 21555 disconnects before the last odd Dword is returned. The 21555 may have read an odd number of Dwords because of either a target disconnect or a master latency timer expiration during 32-bit data transfers on the opposite interface.

4.2.4 64-Bit Extension Support During Reset

When the 21555 supports a 64-bit interface on its primary bus, it samples **p_req64_l** while **p_rst_l** is asserted to determine whether the PCI 64-bit extension signals are connected on the board. When **p_req64_l** is high, the 64-bit extension signals are not connected and the 21555 drives the 64-bit extension outputs to have valid logic levels on the inputs. The 21555 treats all transactions on the primary interface as 32-bit transactions. When **p_req64_l** is low, the 64-bit signals are connected to pull-up resistors on the board and the 21555 does not perform any input biasing. In this case, the 21555 can treat memory write and prefetchable memory read transactions as 64-bit transactions on the primary interface, as previously described in this section.

The 21555 always asserts **s_req64_l** low during **s_rst_l** assertion to indicate that the 64-bit extension is supported on the secondary bus. Individual pull-up resistors must always be supplied for **s_ad<63:32>**, **s_cbe_l<7:4>**, and **s_par6**4.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

5. Remove unnecessary parenthetical phrase from ROM Interface Signal description

Issue: Refer to Section 6.1, Table 6-1, Page 6-2. Under pr_ad[6], remove from the last sentence: "(if implemented)."

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

6. Table 10-1 p_clk and s_clk descriptions need correction and updating

Issue: Refer to Table 10-1, pages 10-1 and 10-2, the last sentences in the **p_clk** and **s_clk** Signal Name descriptions. The sentences are inaccurate. The paragraphs below contain the corrected sentences.

p_clk	I	Primary interface PCI CLK. This signal provides timing for all transactions on the primary PCI bus. All primary PCI inputs are sampled on the rising edge of **p_clk**, and all primary PCI outputs are driven from the rising edge of **p_clk**. The 21555 operates in a frequency range from 0 MHz to 66 MHz in synchronous mode. In asynchronous mode the 21555 supports a clocking ratio (defined p_clk : s_clk or s_clk : p_clk) of a maximum ratio 2.5 : 1 with the upper frequency limit for either clock input being 66MHz.

s_clk	I	Secondary interface PCI CLK. This signal provides timing for all transactions on the secondary PCI bus. All secondary PCI inputs are sampled on the rising edge of **s_clk**, and all secondary PCI outputs are driven from the rising edge of **s_clk**. The 21555 operates in a frequency range from 0 MHz to 66 MHz in synchronous mode. In asynchronous mode the 21555 supports a clocking ratio (defined p_clk : s_clk or s_clk : p_clk) of a maximum ratio 2.5 : 1 with the upper frequency limit for either clock input being 66MHz

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

7. Section 11.2.1, Hot Insertion Input Pin Description Change

Issue: Refer to section 11.2.1, on page 11-3, Last paragraph. Remove the last sentence That paragraph should appear as follows:
"The 21555 is selected to be the secondary bus central function when it detects **pr_ad[6]** low when **s_rst_l** is asserted. When the 21555 detects this condition, it immediately drives **s_ad**, **s_cbe_l**, and **s_par** low and tristates secondary bus control signals for the duration of secondary bus reset. When the 21555 implements a 64-bit secondary interface, it also asserts **s_req64_l**, but tristates all other secondary bus 64-bit extension signals."

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

8. Remove or change 3 incorrect references to the 21554

Issue: The following three entries that refer to the 21554 were modified:

- Page 9-3, Table 9-3, Row Labeled "Downstream Delayed Read", Change "21554" to "21555".
- Page 9-4, Table 9-3, Row Labeled "Upstream Delayed Read", Change "21554" to "21555".
- Section 11.3, Page 11-4, End of Step 3, Remove "(21554 only.)".

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

9. Section 16.1Byte Offset of D7:D6 needs updating

Issue: Refer to Section 16.1, Table 16-1, on page 16-4, the D7:D6 Byte Offset Register Name and Reset Value row. Add the following information to the Register Name and Reset Value (Hex) columns.

D5	Secondary SERR# Disable	00	Y	Y	Y
D7:D6	Mode Settings Configuration Register	Determined by Parallel ROM Strapping Options	—	N	Y
DB:D8	Reset Control	0000	—	Primary	Y

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321).*

10. Remove reference to CLS=4

Issue: Remove the following lines:
Section 2.3.1.4, Page 2-14 delete "A full cache line threshold is used for CLS=4".
Section 2.4.2.2, Table 2-25, Page 2-36. Delete two sentences: "When CLS=4 a full cache line threshold is used.".

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual (278321)*

11. JTAG Action during Hot insertion

Issue: Change Table 12-1 row 3 to be as follows:

tms	I	The JTAG test mode select pin, **tms** causes state transitions in the Test Access Port (TAP) controller. The **tms** signal is pulled high by a weak pull-up resistor internal to the device. If this pin is low while **t_rst_l** is low the device can enter an unsupported mode. Other devices that are not on early power and are connected to the JTAG Scan Chain, pull **tms** low during Hot Insertion causing the 21555 to enter the unsupported mode. During the Hot Insertion isolate this signal from other JTAG devices on the circuit board or JTAG scan chain.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

12. Internal and External Signal Terminations

Issue: Change Table 12-1 rows 1 and 4 to be as follows:

tck	I	JTAG boundary-scan clock. Signal **tck** is the JTAG logic control clock. This pin has an internal weak pull-down resistor.
trst_l	I	JTAG TAP reset and disable. When low, JTAG is disabled and the TAP controller is asynchronously forced into the reset state, which in turn asynchronously initializes other test logic. An unterminated **trst_l** is pulled high by a weak pull-up resistor internal to the device. The TAP controller must be reset before the JTAG circuits can function. For normal JTAG TAP port operation, this signal must be high. Prior to normal 21555 operation, this signal must be strobed low or pulled low with a 1kΩ resistor.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

13. Change to Initialization Section 12.2.1 and JTAG Description

Issue: Change to second paragraph. Also made a change to normal operation description note for JTAG below Figure 12-1. The section now appears as follows:

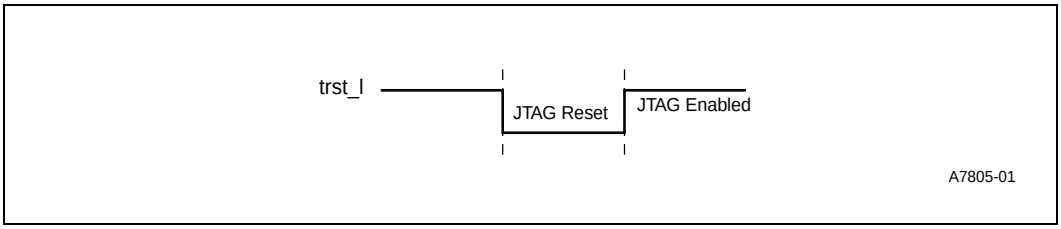
12.2.1 Initialization

The test access port controller and the instruction register output latches are initialized and JTAG is disabled while the **trst_l** input is asserted low (see Figure 12-1). While signal **trst_l** is low, the test access port controller enters the test-logic reset state. This results in the instruction register being reset which holds the bypass register instruction. During test-logic reset state, all JTAG test logic is disabled, and the device performs normal functions. The test access port controller leaves this state only after **trst_l** (low) goes high and an appropriate JTAG test operation sequence is sent on the tms and tck pins.

For the 21555 to operate properly, the JTAG logic must be reset. The controller resets:

- Asynchronously with the assertion of **trst_l** .
- Synchronously after five **tck** clock cycles, with **tms** held high.

Figure 12-1. Signal trst_l States



Note: Prior to normal 21555 operation, this signal must be strobed low or pulled low with a 1kΩ resistor.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

14. Change to Chapter 2, Table 2-3 p_req64_l description

Issue: The last row of Table 2-3 now appears as follows:

p_req64_l	STS	Primary PCI interface request 64-bit transfer. Signal p_req64_l is asserted by the initiator to indicate that the initiator is requesting 64-bit data transfer. Signal p_req64_l has the same timing as p_frame_l. When deasserting, p_req64_l is driven to a deasserted state for one clock cycle and is then sustained by an external pull-up resistor. The 21555 samples p_req64_l during primary reset to enable the 64-bit extension signals. If p_req64_l is sampled high during primary reset, the primary 64-bit extension is disabled and assumed not connected. The 21555 then drives p_ad[63:32], p_cbe_l[7:4], and p_par64 to valid logic levels. ***Note:*** Refer to the ROM Interface signal pr_ad[1] description in Chapter 6, Table 6-1 for information on primary bus 64-bit extension operation upon deassertion of r_rst_in_l.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

15. Change to Section 11.5 l_stat pin description

Issue: Last bullet changed and last note removed. The last bullet now appears as follows:

•Support bi-directional pin, l_stat. This signal functions as both a micro-switch sensor input and a LED control output. 2 ms of debounce is built into the 21555 l_stat pin.

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*

16. Added Section 3.1.1 PCI Local Bus Compliance

Issue: Added Section 3.1.1 that includes new bit information to meet *PCI Local Bus Specification 2.3* requirements. The new section appears as follows:

3.1.1 Added Bits for PCI Local Bus Specification 2.3 Compliance

Two bits were added to the 21555 bridge to meet *PCI Local Bus Specification 2.3* requirements: Bit 10 in the Command Registers and Bit 3 in the Status Registers. The A3 Stepping of the bridge now includes these new features.

Note: For a description of the added bits, please refer to the *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User's Manual.*

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Datasheet (278320).*

17. Change to Tables 61 and 62 in Section 16.5.2

Issue: Two bits were added to the 21555 bridge to meet *PCI Local Bus Specification 2.3* requirements. As a result, Bit 10 information was added to Table 61 in Section 16.5.2 in the Command Registers and Bit 3 information was added to Table 62 in Section 16.5.2 in the Status Registers. The A3 Stepping of the bridge now includes these new features. The new information appears in the tables as follows:

Table 61. Primary and Secondary Command Registers

Offsets	Primary Command	Secondary Command
Primary byte	05:04h	45:44h
Secondary byte	45:44h	05:04h

Bit	Name	R/W	Description
10[1]	Interrupt Disable Bit	R/W	This bit disables the 21555 from asserting p_inta_l / s_inta_l. • When 0, enables the 21555 to assert its p_inta_l / s_inta_l signal. • When 1, disables the 21555 ability to assert the p_inta_l / s_inta_l signal. This bit's state after RST# is 0.

1. Bit not used and does not apply to Step A2 of product

Table 62. Primary and Secondary Status Registers

Offsets	Primary Status	Secondary Status
Primary byte	07:06h	47:46h
Secondary byte	47:46h	07:06h

Bit	Name	R/W	Description
3[1]	Interrupt Status Bit	R	This bit reflects the state of the interrupt in the 21555 bridge. • Only when the Interrupt Disable Bit in the command register is set to 0 and the appropriate interrupt status bit set to 1 will the p_inta_l/s_inta_l signals be asserted. • Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.

1. Bit not used and does not apply to Step A2 of product

Affected Docs: *21555 Non-Transparent PCI-to-PCI Bridge Advance Information User Manual (278321).*