3.3 VOLT ZERO DELAY CLOCK MULTIPLIER 2308B

Description

The 2308B is a high-speed phase-lock loop (PLL) clock multiplier. It is designed to address high-speed clock distribution and multiplication applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

The 2308B has two banks of four outputs each that are controlled via two select addresses. By proper selection of input addresses, both banks can be put in tri-state mode. In test mode, the PLL is turned off, and the input clock directly drives the outputs for system testing purposes. In the absence of an input clock, the 2308B enters power down, and the outputs are tri-stated. In this mode, the device will draw less than 25µA.

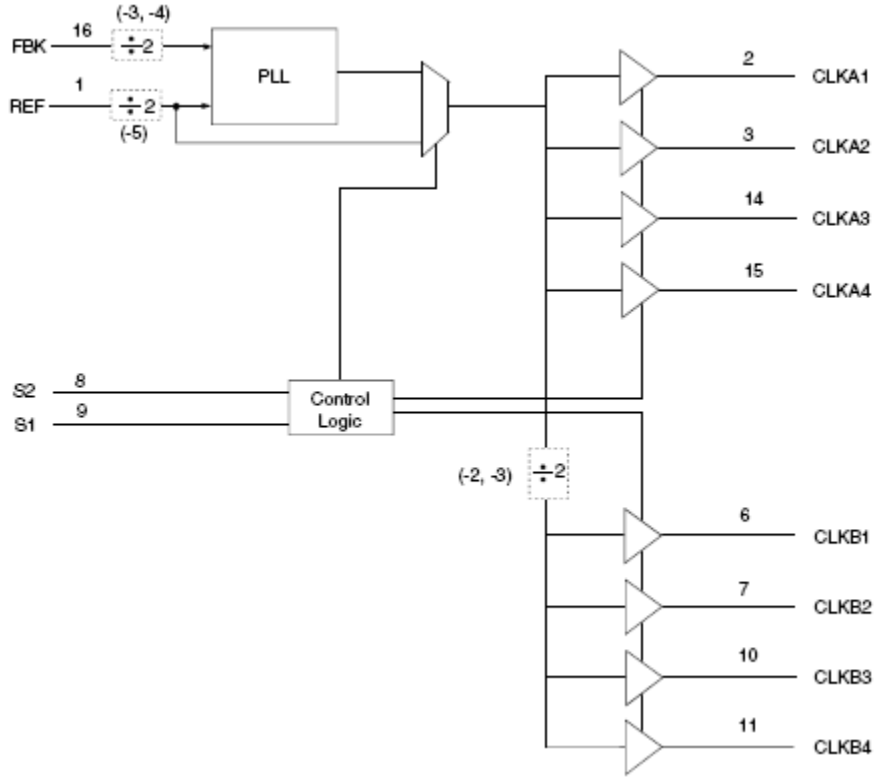
The 2308B is available in six unique configurations for both prescaling and multiplication of the Input REF Clock. (see Available Options for 2308B table.)

The PLL is closed externally to provide more flexibility by allowing the user to control the delay between the input clock and the outputs.

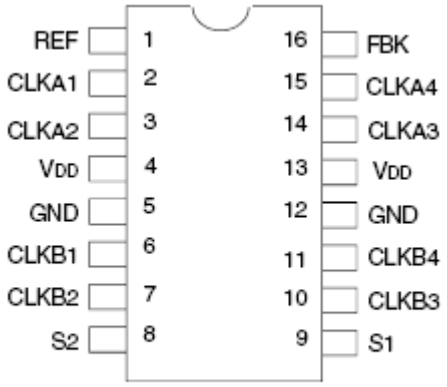
Features

- Phase-Lock Loop Clock Distribution for Applications ranging from 10MHz to 133MHz operating frequency
- Distributes one clock input to two banks of four outputs
- Separate output enable for each output bank
- External feedback (FBK) pin is used to synchronize the outputs to the clock input
- Output Skew < 200 ps
- Low jitter < 200 ps cycle-to-cycle
- 1x, 2x, 4x output options (see Available Options for 2308B table)
- No external RC network required
- Operates at 3.3 V V_{DD}
- Available in 16-SOIC and 16-TSSOP packages
- Available in commercial and industrial temperature ranges

Block Diagram



Pin Assignment



SOIC/ TSSOP

Applications

- SDRAM
- Telecom
- Datacom
- PC Motherboards/Workstations
- Critical Path Delay Designs

Function Table[1] Select Input Decoding

S2	S1	CLKA	CLKB	Output Source	PLL Shut Down
L	L	Tri-state	Tri-state	PLL	Y
L	H	Driven	Tri-state	PLL	N
H	L	Driven	Driven	REF	Y
H	H	Driven	Driven	PLL	N

Note 1: H = HIGH voltage level; L = LOW voltage level

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	REF[1]	Input Reference Clock, 5 Volt Tolerant Input.
2	CLKA1[2]	Clock Output for Bank A.
3	CLKA2[2]	Clock Output for Bank A.
4	VDD	3.3 V Supply.
5	GND	Ground.
6	CLKB1[2]	Clock Output for Bank B.
7	CLKB2[2]	Clock Output for Bank B.
8	S2[3]	Select Input, Bit 2.
9	S1[3]	Select Input, Bit 1.
10	CLKB3[2]	Clock Output for Bank B.
11	CLKB4[2]	Clock Output for Bank B.
12	GND	Ground.
13	VDD	3.3 V Supply.
14	CLKA3[2]	Clock Output for Bank A.
15	CLKA4[2]	Clock Output for Bank A.
16	FBK	PLL Feedback Input.

Notes:
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-up on these inputs.

Available Options for 2308B

Device	Feedback From	Bank A Frequency	Bank B Frequency
2308B-1	Bank A or Bank B	Reference	Reference
2308B-1H	Bank A or Bank B	Reference	Reference
2308B-2	Bank A	Reference	Reference/2
2308B-2	Bank B	2 x Reference	Reference
2308B-2H	Bank A	Reference	Reference/2
2308B-2H	Bank B	2 x Reference	Reference
2308B-3	Bank A	2 x Reference	Reference or $\overline{\text{Reference}}$[1]
2308B-3	Bank B	4 x Reference	2 x Reference
2308B-4	Bank A or Bank B	2 x Reference	2 x Reference
2308B-5H	Bank A or Bank B	Reference/2	Reference/2

Note 1: Output phase is indeterminant (0° or 180° from input clock).

Absolute Maximum Ratings[1]

Symbol	Rating	Max.	Unit
V_{DD}	Supply Voltage Range	-0.5 V to +4.6	V
V_I[2]	Input Voltage Range (REF)	-0.5 V to +5.5	V
V_I	Input Voltage Range (except REF)	-0.5 to V_{DD} + 0.5	V
I_{IK} (V_I < 0)	Input Clamp Current	-50	mA
I_{OK} (V_O < 0 or V_O > VDD)	Terminal Voltage with Respect to GND (inputs V_{IH} 2.5, V_{IL} 2.5)	±50	mA
I_O (V_O = 0 to VDD)	Continuous Output Current	±50	mA
V_{DD} or GND	Continuous Current	±100	mA
T_A = 55 °C (in still air only)[3]	Maximum Power Dissipation	0.7	W
T_{STG}	Storage Temperature Range	-65 to +150	°C
Operating Temperature	Commercial range	0 to +70	°C
Operating Temperature	Industrial range	-40 to +85	°C

Notes:

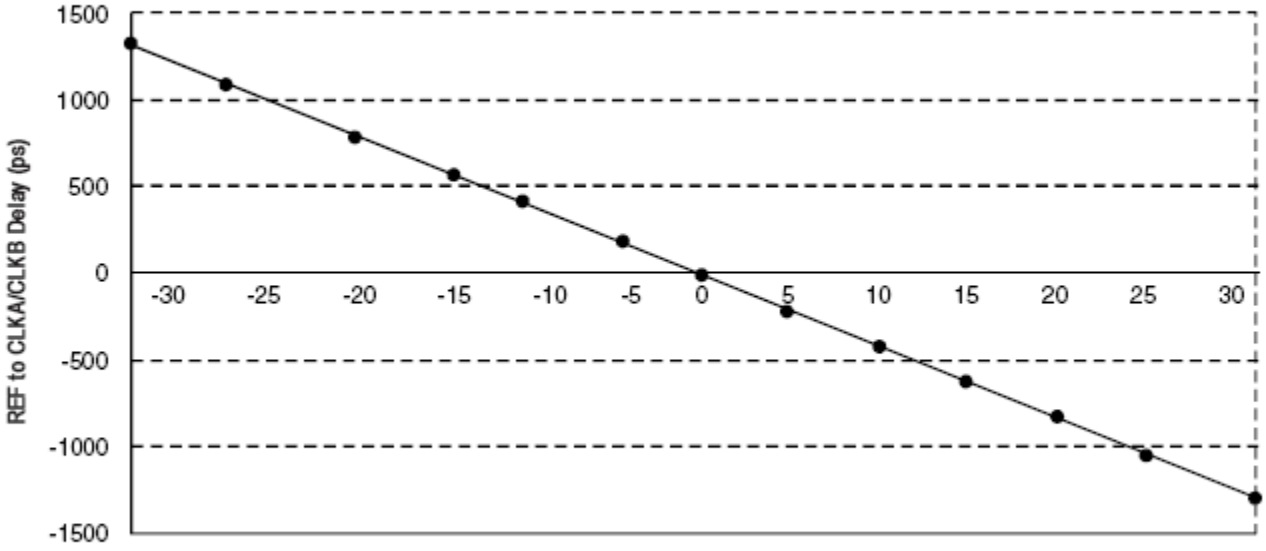
1. Stresses above the ratings listed below can cause permanent damage to the 2308B. These ratings, which are standard values for commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Zero Delay and Skew Control

To close the feedback loop of the 2308B, the FBK pin can be driven from any of the eight available output pins. The output driving the FBK pin will be driving a total load of 7pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the Output Load Difference Chart to calculate loading differences between the feedback output and remaining outputs. Ensure the outputs are loaded equally, for zero output-output skew.

REF TO CLKA/CLKB DELAY vs. OUTPUT LOAD DIFFERENCE BETWEEN FBK PIN AND CLKA/CLKB PINS



OUTPUT LOAD DIFFERENCE BETWEEN FBK PIN AND CLKA/CLKB PINS (pF)

Operating Conditions–Commercial

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{DD}	Supply Voltage		3	3.6	V
T_A	Operating Temperature (Ambient Temperature)		0	70	°C
C_L	Load Capacitance below 100 MHz		–	30	pF
	Load Capacitance from 100 MHz to 133 MHz		–	15	pF
C_{IN}	Input Capacitance[1]		–	7	pF

Note 1: Applies to both REF and FBK.

DC Electrical Characteristics–Commercial

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Input High Voltage Level	V_{IH}			2			V
Input Low Voltage Level	V_{IL}					0.8	V
Input Low Current	I_{IL}	V_{IN} = 0V				50	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}				100	µA
Output High Voltage	V_{OH}	I_{OH} = -8 mA (-1, -2, -3, -4) I_{OH} = -12 mA (-1H, -2H, -5H)		2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA (-1, -2, -3, -4) I_{OL} = 12 mA (-1H, -2H, -5H)				0.4	V
Power Down Current	I_{DD_PD}	REF = 0MHz (S2 = S1 = H)				12	µA
Supply Current	I_{DD}	Unloaded Outputs Select Inputs at V_{DD} or GND	100 MHz CLKA (-1, -2, -3, -4)			45	mA
			100 MHz CLKA (-1H, -2H, -5H)			70	
			66 MHz CLKA (-1, -2, -3, -4)			32	
			66 MHz CLKA (-1H, -2H, -5H)			50	
			33 MHz CLKA (-1, -2, -3, -4)			18	
			33 MHz CLKA (-1H, -2H, -5H)			30	

Switching Characteristics–Commercial

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	t_1	30 pF Load, all devices	10		100	MHz
Output Frequency	t_1	20 pF Load, -1H, -2H, -5H Devices[1]	10		133.3	MHz
Output Frequency	t_1	15pF Load, -1, -2, -3, -4 devices	10		133.3	MHz
Duty Cycle = t2 ÷ t1 (-1, -2, -3, -4, -1H, -2H, -5H)		Measured at 1.4V, FOUT = 66.66MHz, 30pF Load	40	50	60	%
Duty Cycle = t2 ÷ t1 (-1, -2, -3, -4, -1H, -2H, -5H)		Measured at 1.4V, FOUT = 50MHz, 15pF Load	45	50	55	%
Rise Time (-1, -2, -3, -4)	t_3	Measured between 0.8V and 2V, 30pF Load			2.2	ns
Rise Time (-1, -2, -3, -4)	t_3	Measured between 0.8V and 2V, 15pF Load			1.5	ns
Rise Time (-1H, -2H, -5H)	t_3	Measured between 0.8V and 2V, 30pF Load			1.5	ns
Fall Time (-1, -2, -3, -4)	t_4	Measured between 0.8V and 2V, 30pF Load			2.2	ns
Fall Time (-1, -2, -3, -4)	t_4	Measured between 0.8V and 2V, 15pF Load			1.5	ns
Fall Time (-1H, -5H)	t_4	Measured between 0.8V and 2V, 30pF Load			1.25	ns
Output to Output Skew on same Bank (-1, -2, -3, -4)	t_5	All outputs equally loaded			200	ps
Output to Output Skew (-1H, -2H, -5H)		All outputs equally loaded			200	ps
Output Bank A to Output Bank B (-1, -4, -2H, -5H)		All outputs equally loaded			200	ps
Output Bank A to Output Bank B Skew (-2, -3)		All outputs equally loaded			400	ps
Delay, REF Rising Edge to FBK Rising Edge	t_6	Measured at VDD/2			±250	ps
Device to Device Skew	t_7	Measured at VDD/2 on the FBK pins of devices			700	ps
Output Slew Rate	t_8	Measured between 0.8V and 2V on -1H, -2H, -5H device using Test Circuit 2	1			V/ns
Cycle to Cycle Jitter (-1, -1H, -4, -5H)	t_J	Measured at 66.67MHz, loaded outputs, 15pF Load			200	ps
		Measured at 66.67MHz, loaded outputs, 30pF Load			200	
		Measured at 133.3MHz, loaded outputs, 15pF Load			100	
Cycle to Cycle Jitter (-2, -2H, -3)	t_J	Measured at 66.67MHz, loaded outputs, 30pF Load			400	ps
		Measured at 66.67MHz, loaded outputs, 15pF Load			400	
PLL Lock Time	t_{LOCK}	Stable Power Supply, valid clocks presented on REF and FBK pins			1	ms

Note 1: 2308B-5H has maximum input frequency of 133.33MHz and maximum output of 66.67MHz.

Operating Conditions–Industrial

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{DD}	Supply Voltage		3	3.6	V
T_A	Operating Temperature (Ambient Temperature)		-40	+85	°C
C_L	Load Capacitance below 100MHz		–	30	pF
	Load Capacitance from 100MHz to 133MHz		–	15	pF
C_{IN}	Input Capacitance[1]		–	7	pF

Note 1: Applies to both REF and FBK.

DC Electrical Characteristics–Industrial

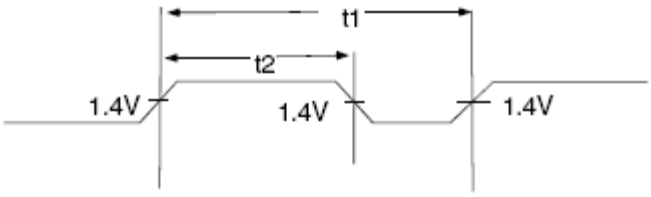
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Input High Voltage Level	V_{IH}			2			V
Input Low Voltage Level	V_{IL}					0.8	V
Input Low Current	I_{IL}	V_{IN} = 0V				50	µA
Input High Current	I_{IH}	V_{IN} = V_{DD}				100	µA
Output High Voltage	V_{OH}	I_{OH} = -8 mA (-1, -2, -3, -4) I_{OH} = -12 mA (-1H, -2H, -5H)		2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA (-1, -2, -3, -4) I_{OL} = 12 mA (-1H, -2H, -5H)				0.4	V
Power Down Current	I_{DD_PD}	REF = 0MHz (S2 = S1 = H)				25	µA
Supply Current	I_{DD}	Unloaded Outputs Select Inputs at V_{DD} or GND	100 MHz CLKA (-1, -2, -3, -4)			45	mA
			100 MHz CLKA (-1H, -2H, -5H)			70	
			66 MHz CLKA (-1, -2, -3, -4)			32	
			66 MHz CLKA (-1H, -2H, -5H)			50	
			33 MHz CLKA (-1, -2, -3, -4)			18	
			33 MHz CLKA (-1H, -2H, -5H)			30	

Switching Characteristics–Industrial

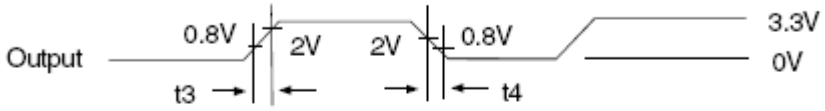
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Frequency	t_1	30 pF Load, all devices	10		100	MHz
Output Frequency	t_1	20 pF Load, -1H, -2H, -5H Devices[1]	10		133.3	MHz
Output Frequency	t_1	15pF Load, -1, -2, -3, -4 devices	10		133.3	MHz
Duty Cycle = t2 ÷ t1 (-1, -2, -3, -4, -1H, -2H, -5H)		Measured at 1.4V, FOUT = 66.66 MHz, 30 pF Load	40	50	60	%
Duty Cycle = t2 ÷ t1 (-1, -2, -3, -4, -1H, -2H, -5H)		Measured at 1.4V, FOUT = 50 MHz, 15 pF Load	45	50	55	%
Rise Time (-1, -2, -3, -4)	t_3	Measured between 0.8V and 2V, 30pF Load			2.2	ns
Rise Time (-1, -2, -3, -4)	t_3	Measured between 0.8V and 2V, 15pF Load			1.5	ns
Rise Time (-1H, -2H, -5H)	t_3	Measured between 0.8V and 2V, 30pF Load			1.5	ns
Fall Time (-1, -2, -3, -4)	t_4	Measured between 0.8V and 2V, 30pF Load			2.2	ns
Fall Time (-1, -2, -3, -4)	t_4	Measured between 0.8V and 2V, 15pF Load			1.5	ns
Fall Time (-1H, -5H)	t_4	Measured between 0.8V and 2V, 30pF Load			1.25	ns
Output to Output Skew on same Bank (-1, -2, -3, -4)	t_5	All outputs equally loaded			200	ps
Output to Output Skew (-1H, -2H, -5H)		All outputs equally loaded			200	ps
Output Bank A to Output Bank B (-1, -4, -2H, -5H)		All outputs equally loaded			200	ps
Output Bank A to Output Bank B Skew (-2, -3)		All outputs equally loaded			400	ps
Delay, REF Rising Edge to FBK Rising Edge	t_6	Measured at VDD/2			±250	ps
Device to Device Skew	t_7	Measured at VDD/2 on the FBK pins of devices			700	ps
Output Slew Rate	t_8	Measured between 0.8V and 2V on -1H, -2H, -5H device using Test Circuit 2	1			V/ns
Cycle to Cycle Jitter (-1, -1H, -4, -5H)	t_J	Measured at 66.67MHz, loaded outputs, 15pF Load			200	ps
		Measured at 66.67MHz, loaded outputs, 30pF Load			200	
		Measured at 133.3MHz, loaded outputs, 15pF Load			100	
Cycle to Cycle Jitter (-2, -2H, -3)	t_J	Measured at 66.67MHz, loaded outputs, 30pF Load			400	ps
		Measured at 66.67MHz, loaded outputs, 15pF Load			400	
PLL Lock Time	t_{LOCK}	Stable Power Supply, valid clocks presented on REF and FBK pins			1	ms

Note 1: 2308B-5H has maximum input frequency of 133.33 MHz and maximum output of 66.67 MHz.

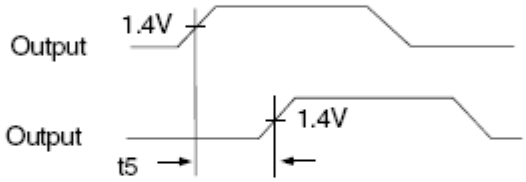
Switching Waveforms



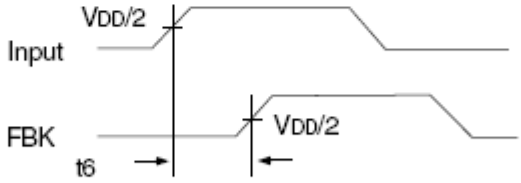
Duty Cycle Timing



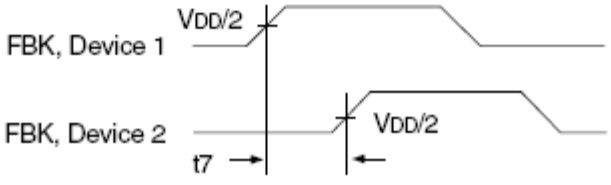
All Outputs Rise/Fall Time



Output to Output Skew

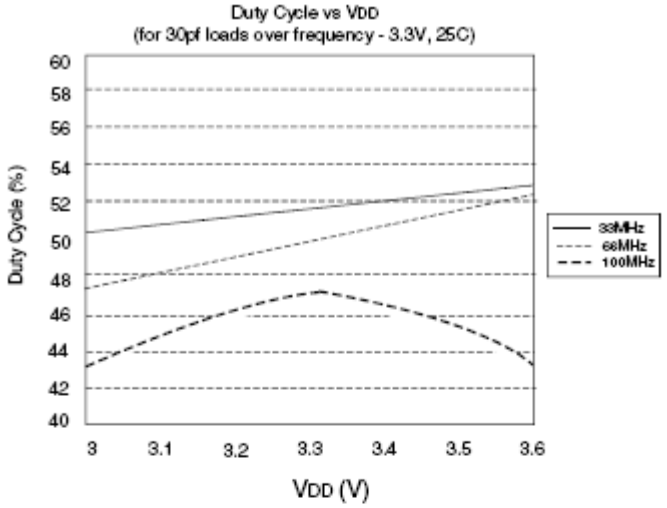


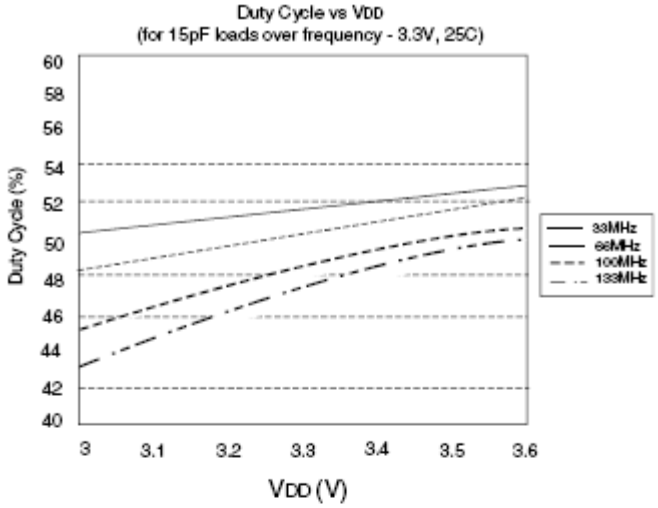
Input to Output Propagation Delay

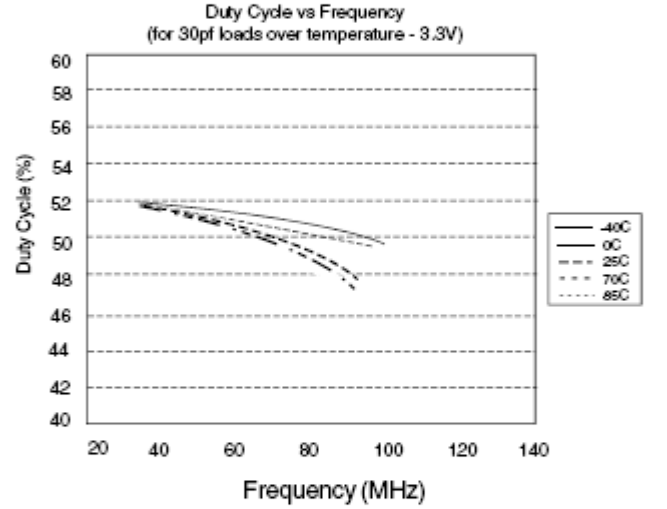


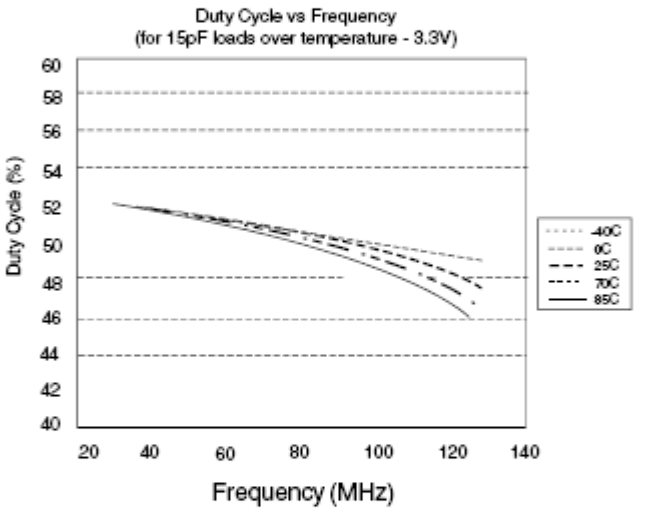
Device to Device Skew

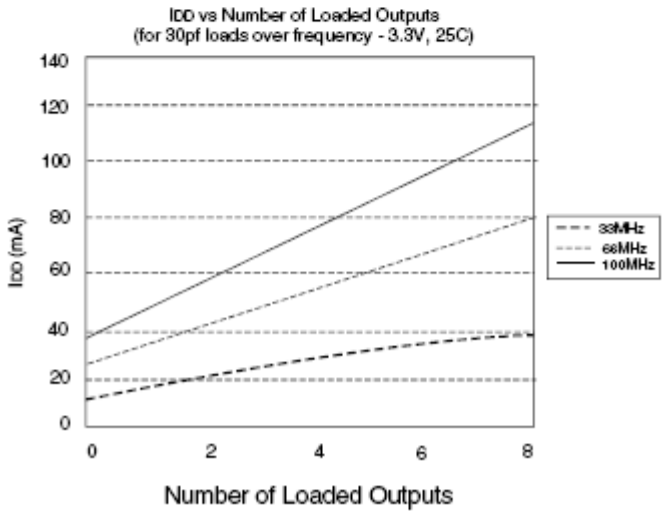
Typical Duty Cycle[1] and I_{DD} Trends[2] for 2308B-1, 2, 3, and 4

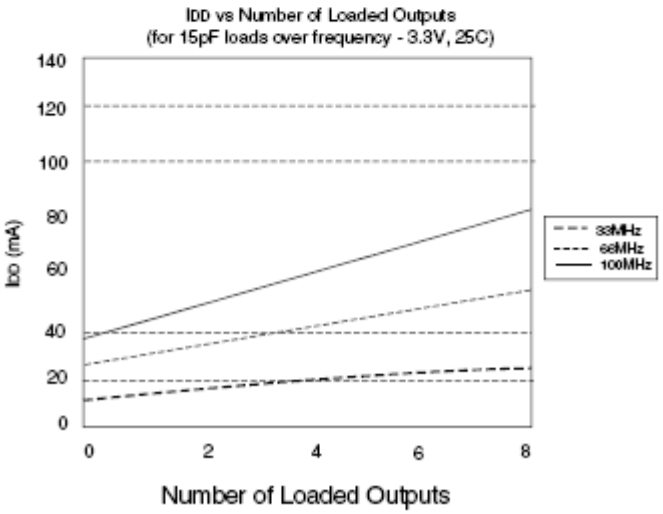








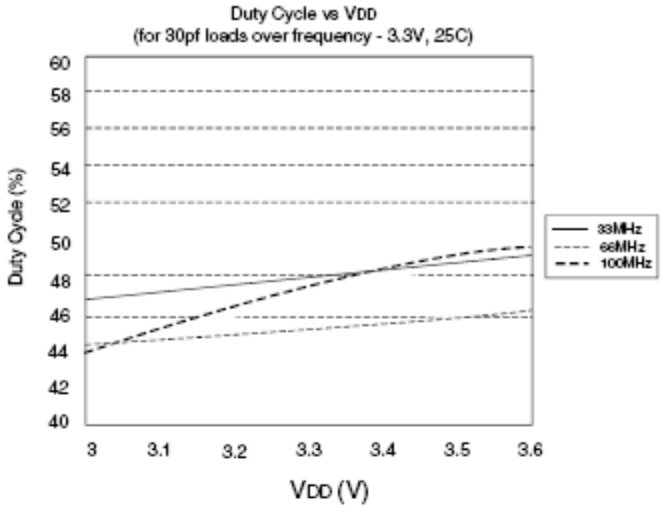


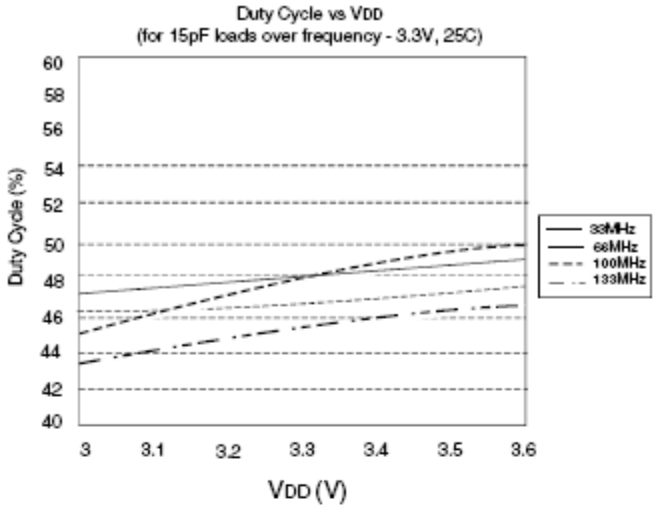


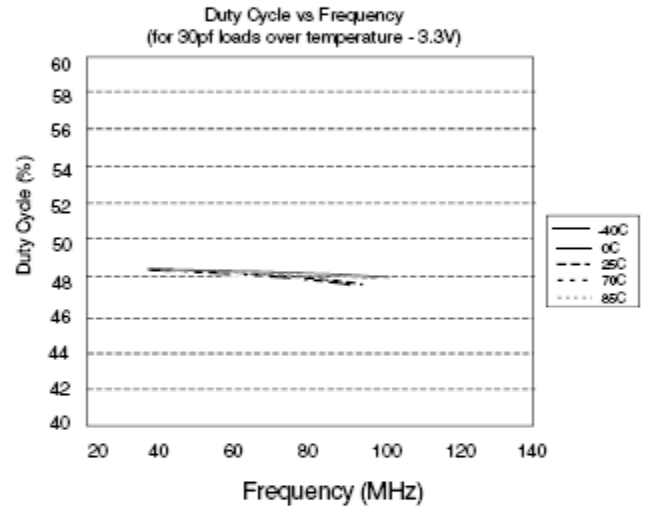
NOTES:

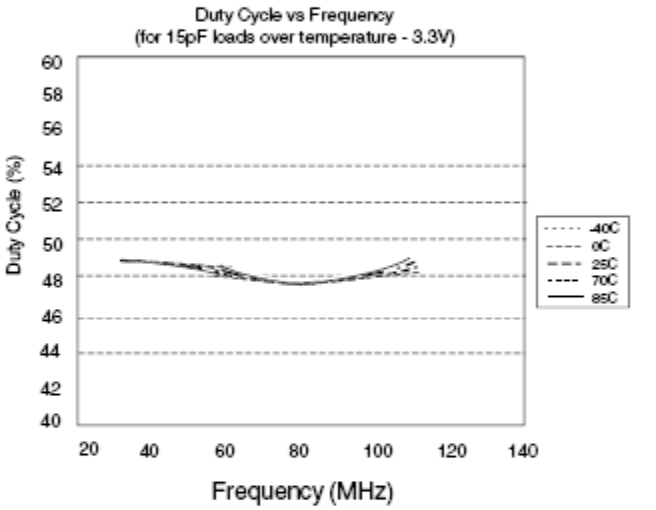
1. Duty Cycle is taken from typical chip measured at 1.4V.
2. IDD data is calculated from IDD = ICORE + nCVf, where ICORE is the Unloaded Current (n = Number of Outputs; C = Capacitance Load per Output (F); V = Voltage Supply(V); f = Frequency (Hz).

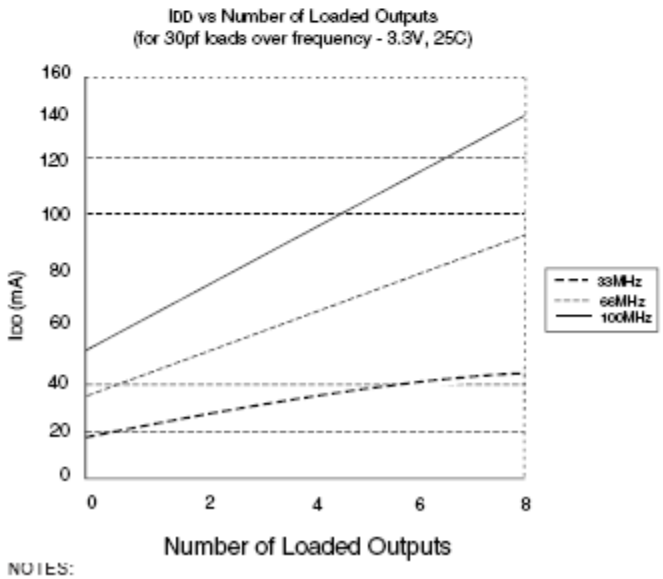
Typical Duty Cycle[1] and I_{DD} Trends[2] for 2308B-1H, 2H, and 5H

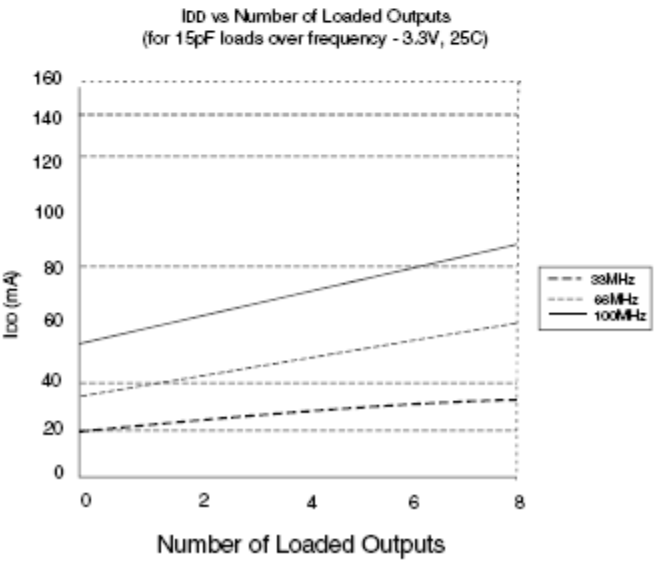










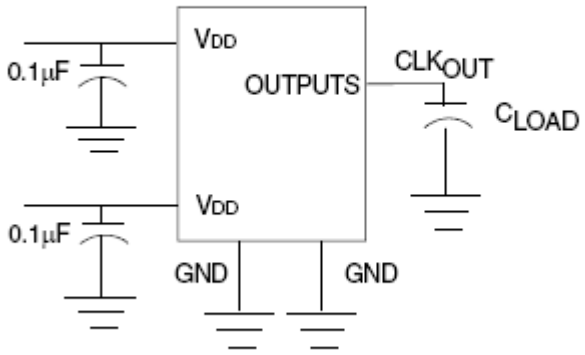


NOTES:

1. Duty Cycle is taken from typical chip measured at 1.4V.
2. IDD data is calculated from IDD = ICORE + nCVf, where ICORE is the Unloaded Current (n = Number of Outputs; C = Capacitance Load per Output (F); V = Voltage Supply(V); f = Frequency (Hz).

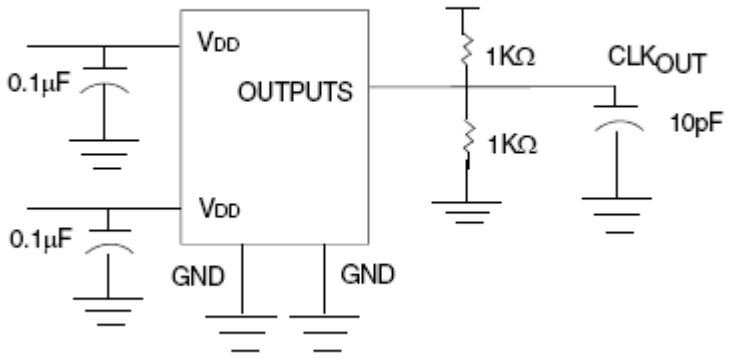
Test Circuits

TEST CIRCUIT 1



Test Circuit for all Parameters Except t8

TEST CIRCUIT 2



Test Circuit for t8, Output Slew Rate On -1H, -2H, and -5H Device

Thermal Characteristics 16-TSSOP

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		78		°C/W
	θ_{JA}	1 m/s air flow		70		°C/W
	θ_{JA}	3 m/s air flow		68		°C/W
Thermal Resistance Junction to Case	θ_{JC}			37		°C/W

Thermal Characteristics 16-SOIC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
2308B-1DC	Tubes	16-SOIC	0 to +70°C
2308B-1DCI	Tubes	16-SOIC	-40 to +85°C
2308B-1DCG	Tubes	16-SOIC	0 to +70°C
2308B-1DCGI	Tubes	16-SOIC	-40 to +85°C
2308B-1DC8	Tape and Reel	16-SOIC	0 to +70°C
2308B-1DCI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-1DCG8	Tape and Reel	16-SOIC	0 to +70°C
2308B-1DCGI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-1HDC	Tubes	16-SOIC	0 to +70°C
2308B-1HDCI	Tubes	16-SOIC	-40 to +85°C
2308B-1HDCG	Tubes	16-SOIC	0 to +70°C
2308B-1HDCGI	Tubes	16-SOIC	-40 to +85°C
2308B-1HDC8	Tape and Reel	16-SOIC	0 to +70°C
2308B-1HDCI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-1HDCG8	Tape and Reel	16-SOIC	0 to +70°C
2308B-1HDCGI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-1HPG	Tubes	16-TSSOP	0 to +70°C
2308B-1HPGI	Tubes	16-TSSOP	-40 to +85°C
2308B-1HPGG	Tubes	16-TSSOP	0 to +70°C
2308B-1HPGGI	Tubes	16-TSSOP	-40 to +85°C
2308B-1HPG8	Tape and Reel	16-TSSOP	0 to +70°C
2308B-1HPGI8	Tape and Reel	16-TSSOP	-40 to +85°C
2308B-1HPGG8	Tape and Reel	16-TSSOP	0 to +70°C
2308B-1HPGGI8	Tape and Reel	16-TSSOP	-40 to +85°C
2308B-2DC	Tubes	16-SOIC	0 to +70°C
2308B-2DCI	Tubes	16-SOIC	-40 to +85°C
2308B-2DCG	Tubes	16-SOIC	0 to +70°C
2308B-2DCGI	Tubes	16-SOIC	-40 to +85°C
2308B-2DC8	Tape and Reel	16-SOIC	0 to +70°C
2308B-2DCI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-2DCG8	Tape and Reel	16-SOIC	0 to +70°C
2308B-2DCGI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-3DCG	Tubes	16-SOIC	0 to +70°C
2308B-3DCGI	Tubes	16-SOIC	-40 to +85°C
2308B-3DCG8	Tape and Reel	16-SOIC	0 to +70°C
2308B-3DCGI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-4DC	Tubes	16-SOIC	0 to +70°C
2308B-4DCI	Tubes	16-SOIC	-40 to +85°C
2308B-4DCG	Tubes	16-SOIC	0 to +70°C
2308B-4DCGI	Tubes	16-SOIC	-40 to +85°C
2308B-4DC8	Tape and Reel	16-SOIC	0 to +70°C
2308B-4DCI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-4DCG8	Tape and Reel	16-SOIC	0 to +70°C

Part / Order Number	Shipping Packaging	Package	Temperature
2308B-4DCGI8	Tape and Reel	16-SOIC	-40 to +85°C
2308B-5HPG	Tubes	16-TSSOP	0 to +70°C
2308B-5HPGI	Tubes	16-TSSOP	-40 to +85°C
2308B-5HPGG	Tubes	16-TSSOP	0 to +70°C
2308B-5HPGGI	Tubes	16-TSSOP	-40 to +85°C
2308B-5HPG8	Tape and Reel	16-TSSOP	0 to +70°C
2308B-5HPGI8	Tape and Reel	16-TSSOP	-40 to +85°C
2308B-5HPGG8	Tape and Reel	16-TSSOP	0 to +70°C
2308B-5HPGGI8	Tape and Reel	16-TSSOP	-40 to +85°C

The 2308B-1, -2, -3, and -4 are Zero Delay Clock Buffers with Standard Drive.
The 2308B-1H, -2H, and -5H are Zero Delay Clock Buffers with High Drive.
Parts ordered with a "G" after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

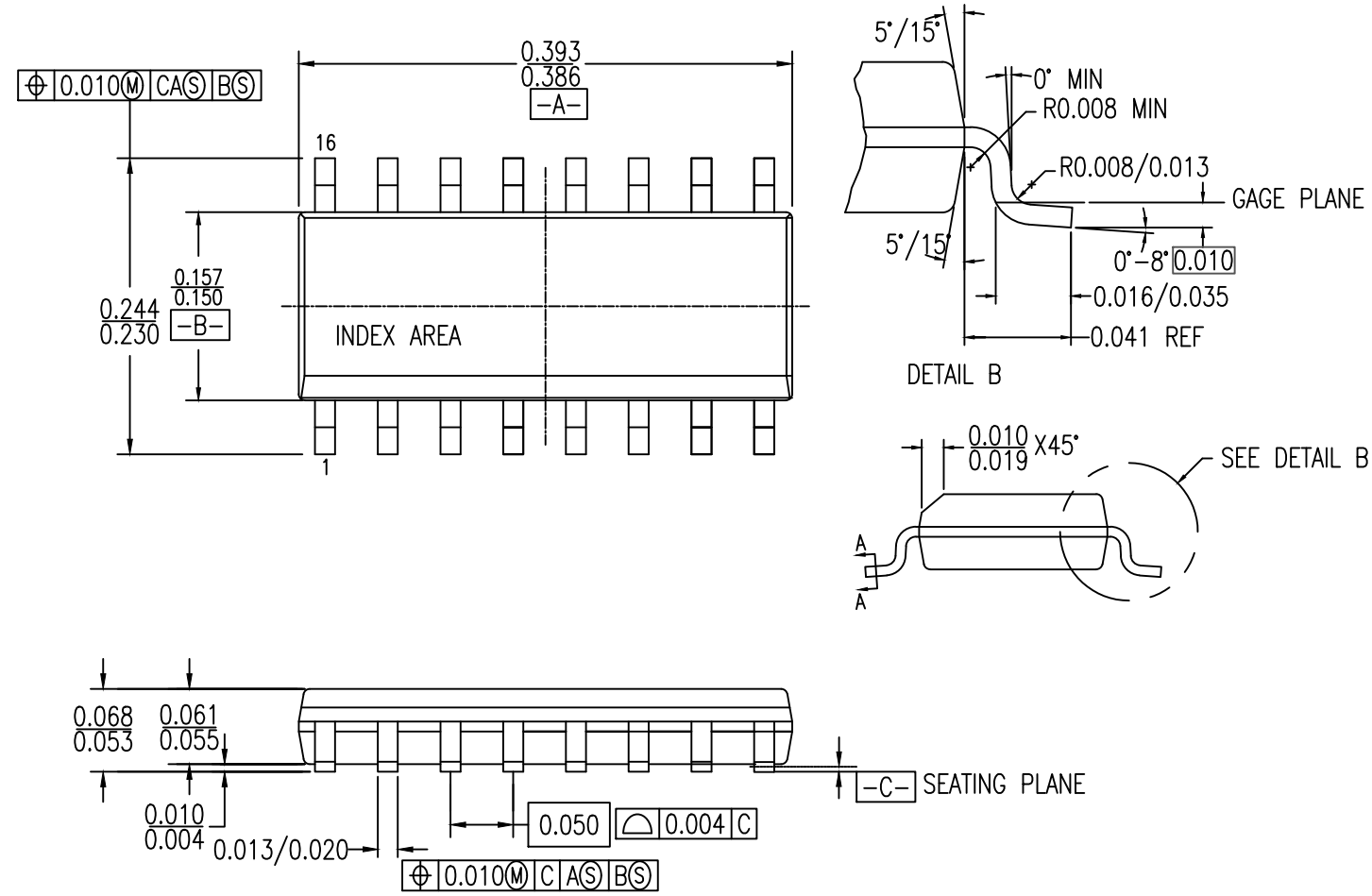
Revision History

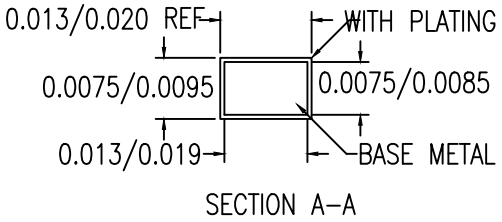
Date	Description of Change
May 21, 2021	• Removed all IDT prefixes. • Rebranded to Renesas. • Updated Package Outline Drawings section. • Updated Ordering Information table.
March 5, 2009	Updated part ordering to include 2308B-3DCG and -3DCGI.
November 3, 2008	Initial release.

16-SOIC Package Outline Drawing

0.150" Body Width, 0.050" Pitch

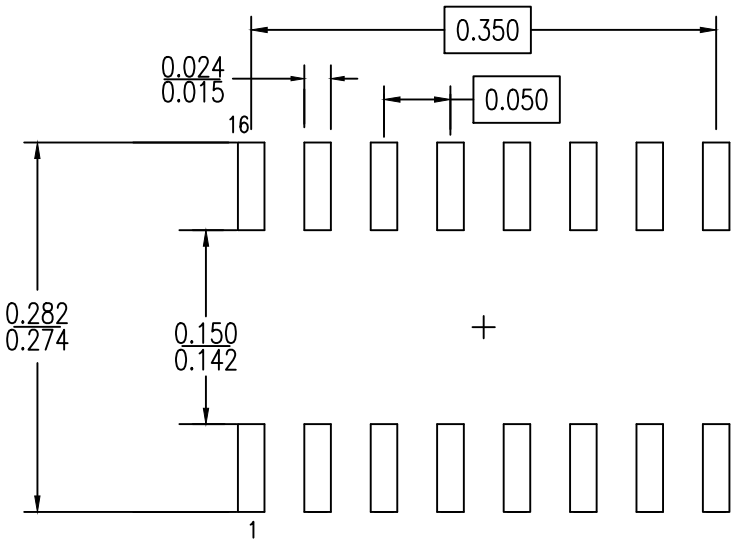
DCG16D1, PSC-4774-01, Rev 00, Page 1





NOTES:

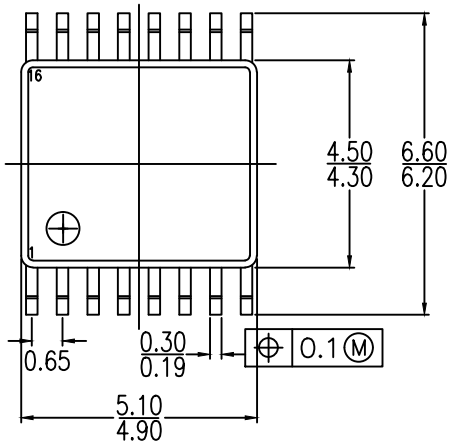
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN INCHES

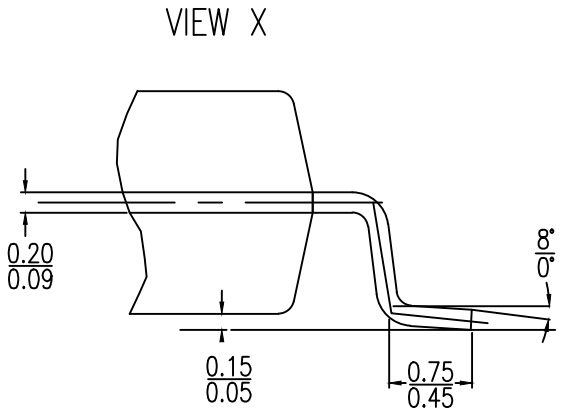


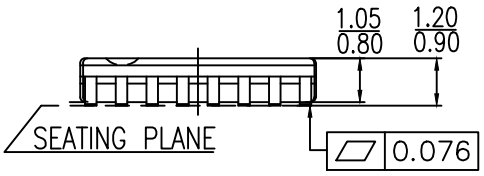
RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN INCHES

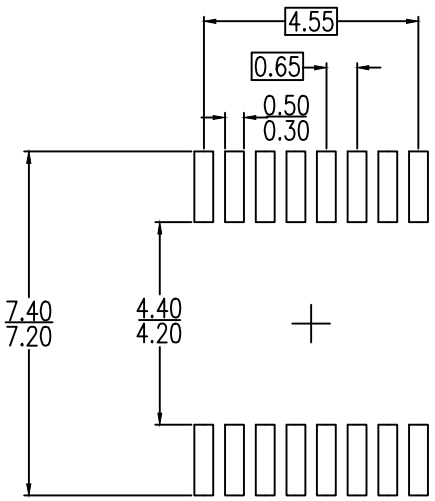
Package Revision History		
Date Created	Rev No.	Description
July 27, 2018	Rev 00	Initial Release







NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS



LAND PATTERN DIMENSIONS

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
Jan 26, 2018	Rev 00	Revised from PSC-4056-02 PGG16

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.