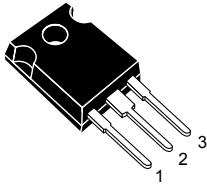
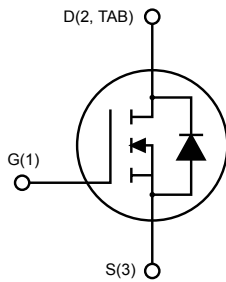


N-channel 600 V, 0.150 Ω typ., 19.5 A, FDmesh II Power MOSFET in a TO-247 package



TO-247



AM01475v1_noZen



Features

Order code	V_{DS} @ T_J max	$R_{DS(on)}$ max.	I_D
STW23NM60ND	650 V	0.180 Ω	19.5 A

- Fast-recovery body diode
- Low gate charge and input capacitance
- Low on-resistance $R_{DS(on)}$
- 100% avalanche tested
- High dv/dt ruggedness

Applications

- Switching applications

Description

This FDmesh II Power MOSFET with fast-recovery body diode is produced using MDmesh II technology. Utilizing a new strip-layout vertical structure, this device features low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.

Product status link

[STW23NM60ND](#)

Product summary

Order code	STW23NM60ND
Marking	23NM60ND
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	19.5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11.7	
$I_{DM}^{(1)}$	Drain current (pulsed)	78	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	9	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	700	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		

1. Pulse width is limited by safe operating area.

2. $I_{SD} \leq 19.5\text{ A}$, $di/dt \leq 600\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
$dv/dt^{(1)}$	Drain-source voltage slope	$V_{DD} = 480\text{ V}$, $I_D = 19.5\text{ A}$, $V_{GS} = 10\text{ V}$		30		V/ns
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(2)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.150	0.180	Ω

1. Characteristic value at turn off on inductive load.
2. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	2100	-	pF
C_{oss}	Output capacitance		-	80	-	pF
C_{rss}	Reverse transfer capacitance		-	10	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	310	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$, Gate DC Bias = 0 V, Test signal level = 20 mV, open drain	-	4	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 19.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$	-	69	-	nC
Q_{gs}	Gate-source charge	(see Figure 13. Test circuit for gate charge behavior)	-	13	-	nC
Q_{gd}	Gate-drain charge		-	35	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 10\text{ A}$,	-	21	-	ns
t_r	Rise time	$R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	19	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	92	-	ns
t_f	Fall time		-	42	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		19.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		78	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 19.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$,	-	190		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	1.2		μC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	13		A
t_{rr}	Reverse recovery time	$I_{SD} = 19.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$,	-	270		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	2.0		μC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	15		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

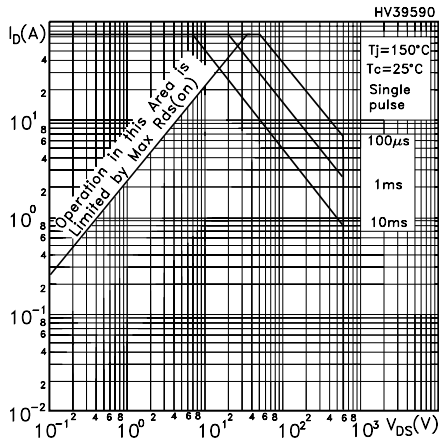


Figure 2. Thermal impedance

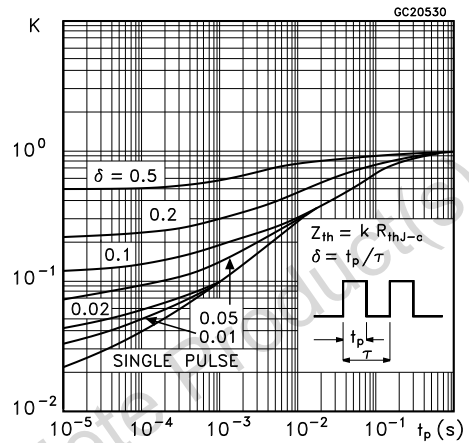


Figure 3. Output characteristics

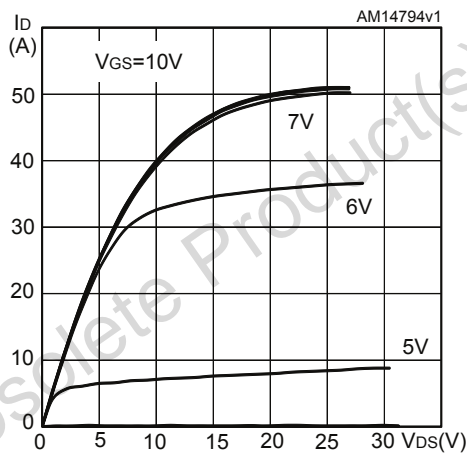


Figure 4. Transfer characteristics

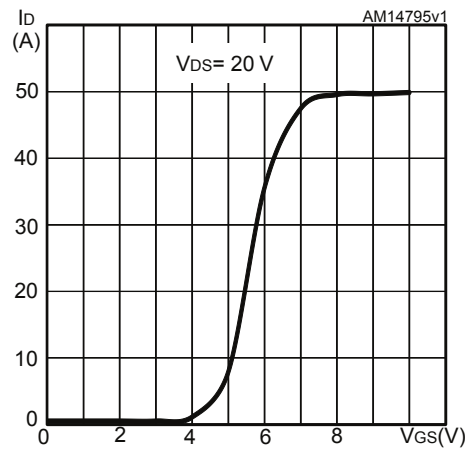


Figure 5. Static drain-source on resistance

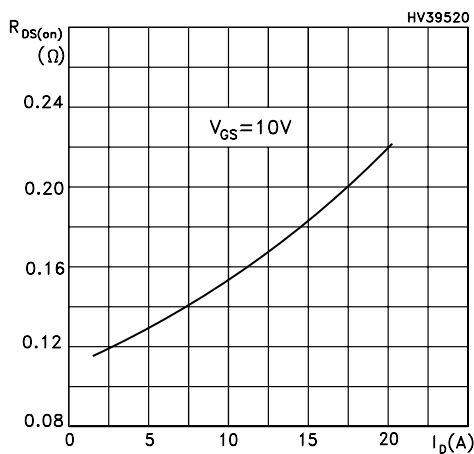


Figure 6. Gate charge vs gate-source voltage

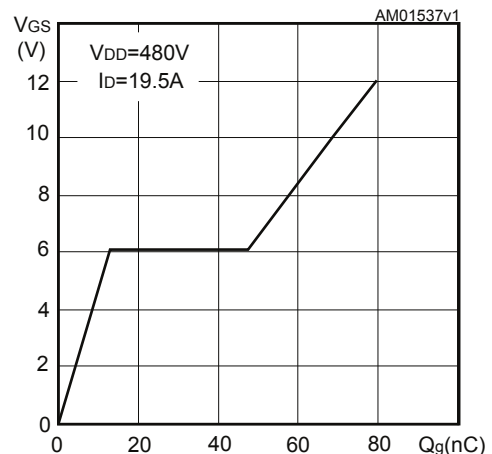


Figure 7. Capacitance variations

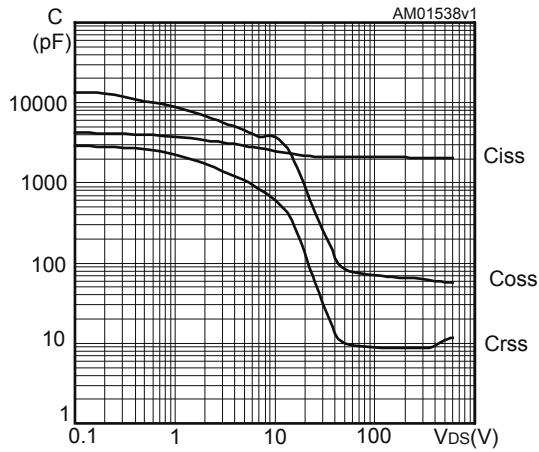


Figure 8. Normalized gate threshold voltage vs temperature

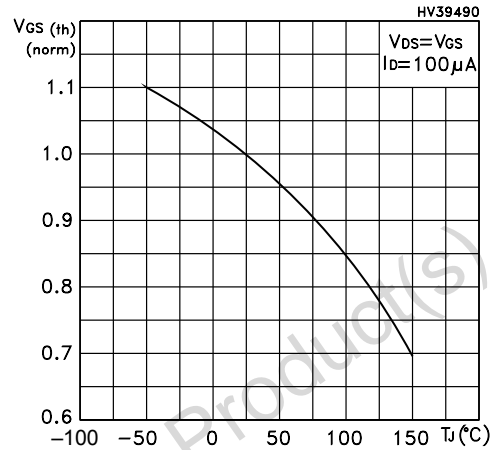


Figure 9. Normalized on resistance vs temperature

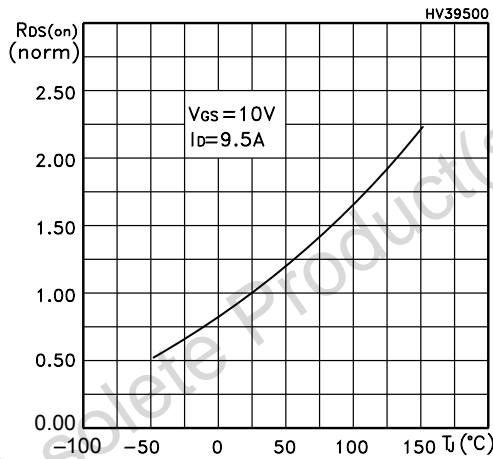


Figure 10. Source-drain diode forward characteristics

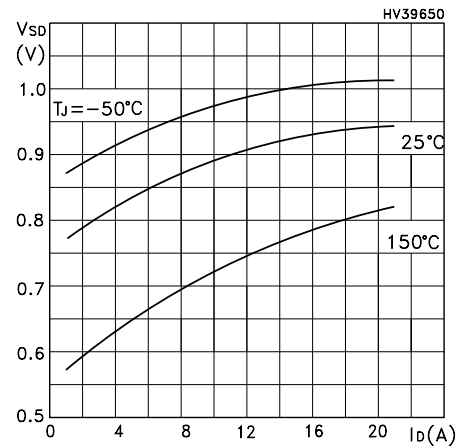
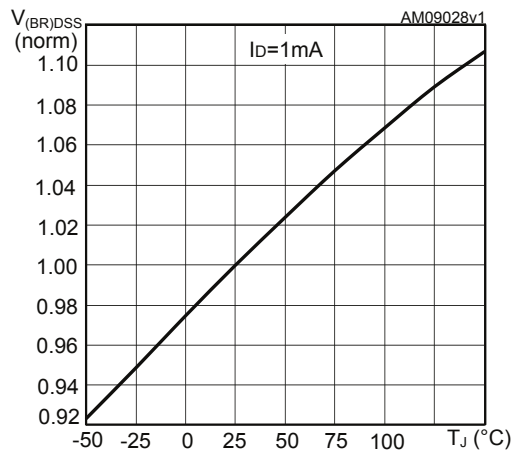
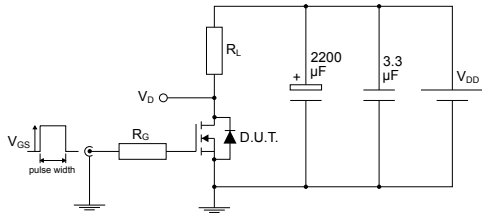


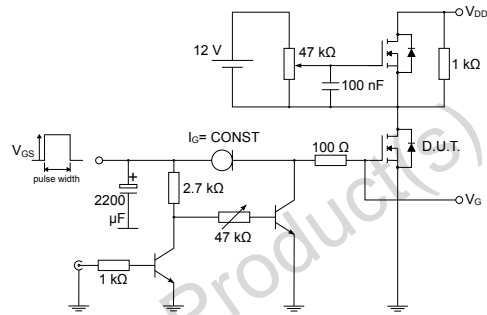
Figure 11. Normalized breakdown voltage vs temperature



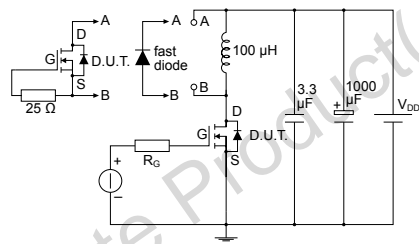
3 Test circuits

Figure 12. Test circuit for resistive load switching times


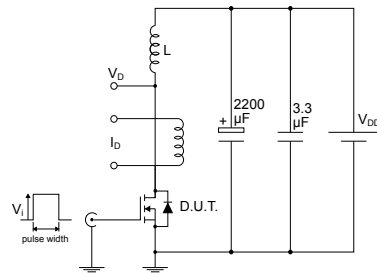
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Figure 13. Test circuit for gate charge behavior


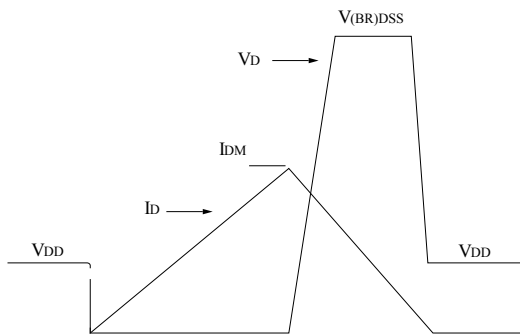
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Figure 14. Test circuit for inductive load switching and diode recovery times


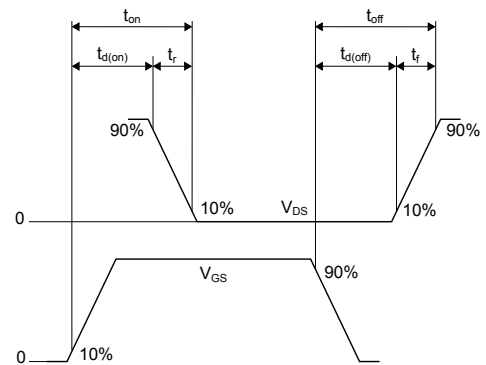
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Figure 15. Unclamped inductive load test circuit


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Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform


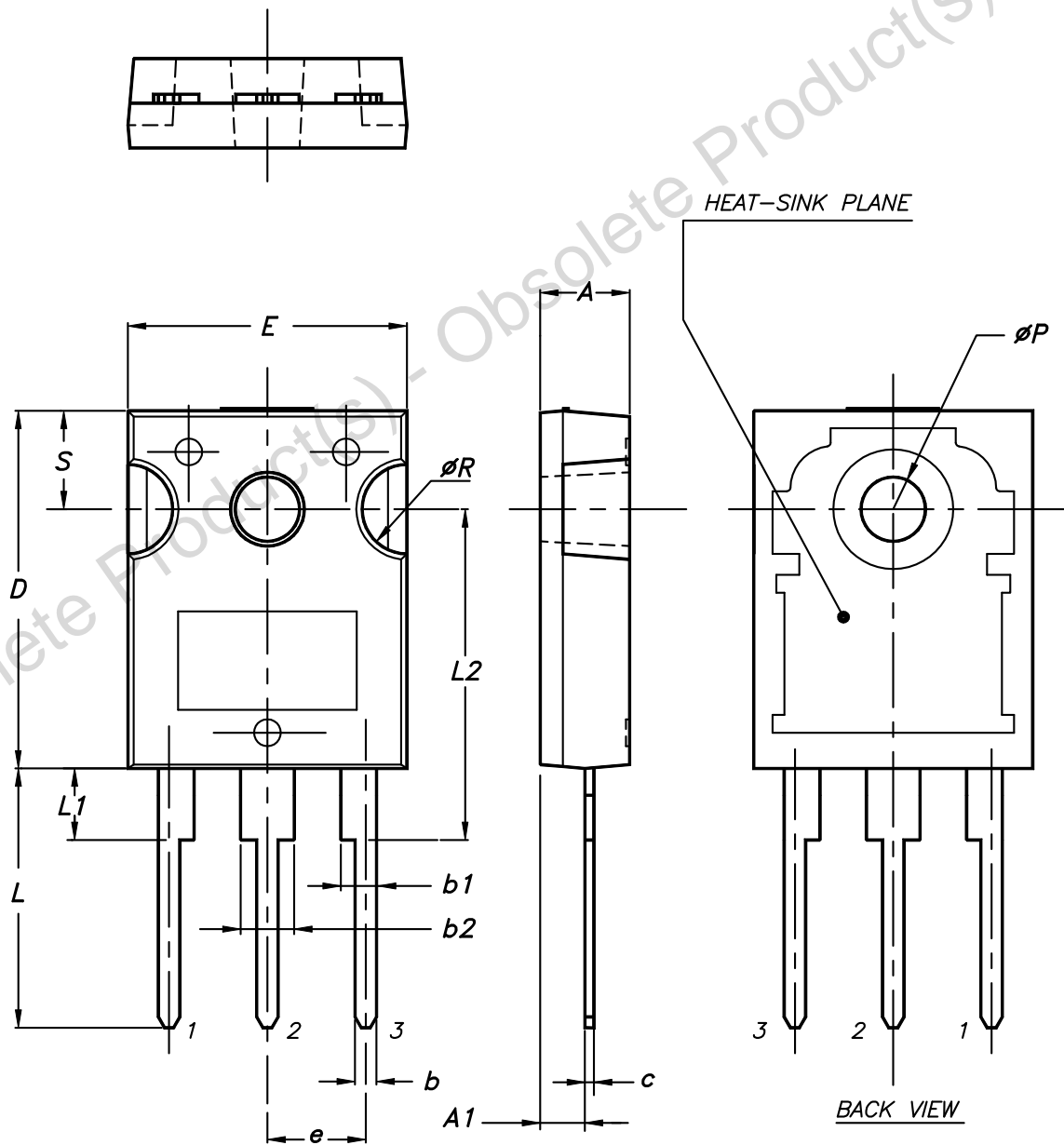
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 18. TO-247 package outline



0075325_9

Table 7. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 8. Document revision history

Date	Revision	Changes
13-Jan-2020	1	First release. Part number previously included in datasheet DS5681.

Obsolete Product(s) - Obsolete Product(s)

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	7
4	Package information	8
4.1	TO-247 package information	8
	Revision history	10

Obsolete Product(s) - Obsolete Product(s)

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