



Not recommended for new designs –
Please use 24LC01SC or 24LC02SC.

24C01SC/24C02SC

1K/2K 5.0V I²C™ Serial EEPROMs for Smart Cards

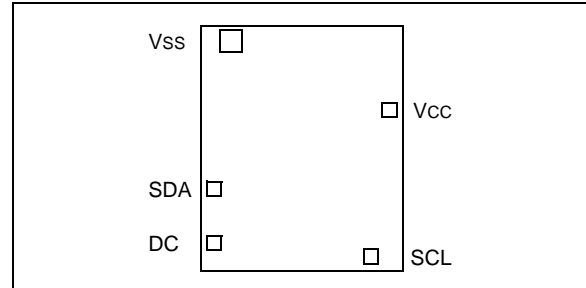
Features:

- ISO Standard 7816 pad locations
- Low-power CMOS technology
 - 1 mA active current typical
 - 10 μ A standby current typical at 5.5V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- 100 kHz and 400 kHz compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- ESD protection > 4 kV
- 1,000,000 E/W cycles ensured
- Data retention > 200 years
- Available for extended temperature ranges
 - Commercial (C): 0°C to +70°C

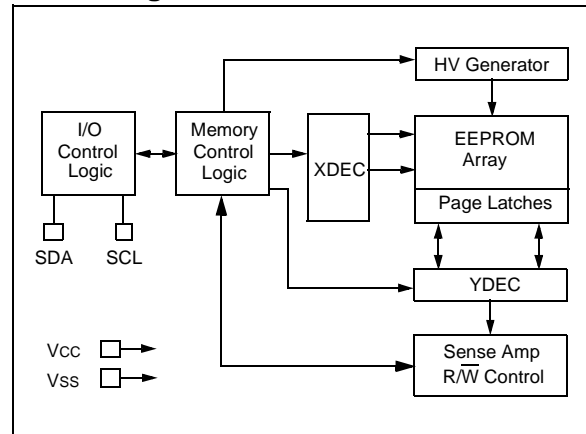
Description:

The Microchip Technology Inc. 24C01SC and 24C02SC are 1K-bit and 2K-bit Electrically Erasable PROMs with bondpad positions optimized for smart card applications. The devices are organized as a single block of 128 x 8-bit or 256 x 8-bit memory with a two-wire serial interface. The 24C01SC and 24C02SC also have page-write capability for up to 8 bytes of data.

Die Layout



Block Diagram



I²C is a trademark of Philips Corporation.

24C01SC/24C02SC

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

| | |
|---|---------------------------------|
| V _{CC} | 7.0V |
| All inputs and outputs w.r.t. V _{SS} | -0.6V to V _{CC} + 1.0V |
| Storage temperature | -65°C to +150°C |
| Ambient temperature with power applied..... | -40°C to +125°C |
| ESD protection on all pads | ≥4 kV |

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

| DC CHARACTERISTICS | V _{CC} = +4.5V to +5.5V Commercial (C): T _A = 0°C to +70°C | | | | |
|--------------------------------------|--|---------------------|--------------------|-------|---|
| Parameter | Symbol | Min. | Max. | Units | Conditions |
| SCL and SDA pads: | | | | | |
| High level input voltage | V _{IH} | .7 V _{CC} | — | — | (Note 1) I _{OL} = 3.0 mA, V _{CC} = 4.5V |
| Low level input voltage | V _{IL} | — | .3 V _{CC} | V | |
| Hysteresis of Schmidt Trigger inputs | V _{HYS} | .05 V _{CC} | — | V | |
| Low level output voltage | V _{OL} | — | .40 | V | |
| Input leakage current (SCL) | I _{LI} | -10 | 10 | μA | V _{IN} = .1V to 5.5V |
| Output leakage current (SDA) | I _{LO} | -10 | 10 | μA | V _{OUT} = .1V to 5.5V |
| Pin capacitance (all inputs/outputs) | C _{IN} , C _{OUT} | — | 10 | pF | V _{CC} = 5.0V (Note 1) T _A = 25°C, F _{CLK} = 1 MHz |
| Operating current | I _{CC} Write | — | 3 | mA | V _{CC} = 5.5V |
| | I _{CC} Read | — | 1 | mA | V _{CC} = 5.5V, SCL = 400 KHz |
| Standby current | I _{CCS} | — | 100 | μA | V _{CC} = 5.5V, SDA = SCL = V _{CC} |

Note 1: This parameter is periodically sampled and not 100% tested.

FIGURE 1-1: BUS TIMING START/STOP

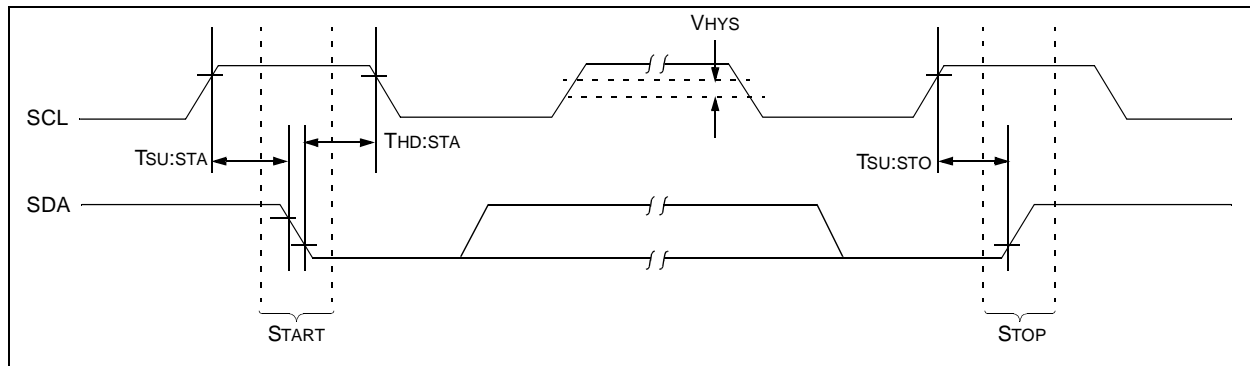


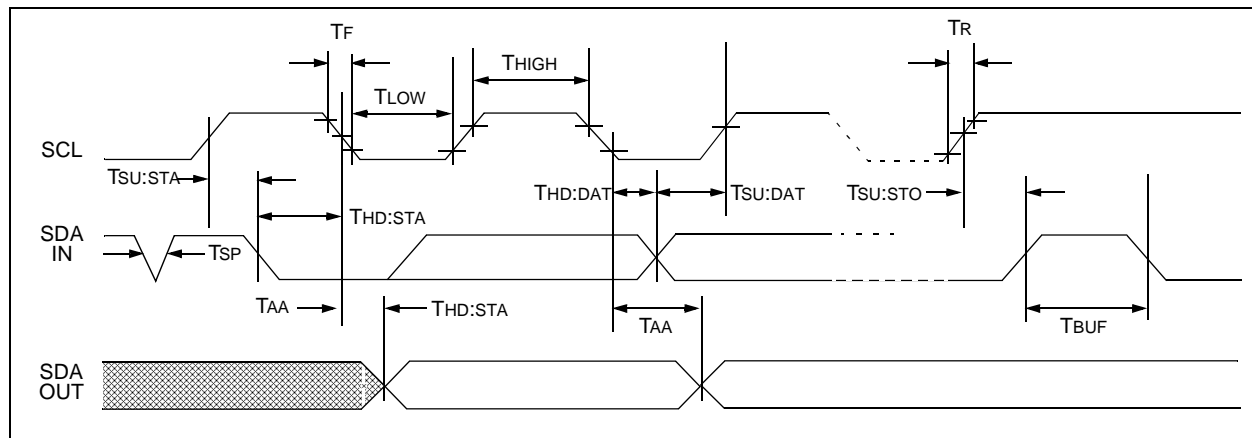
TABLE 1-2: AC CHARACTERISTICS

| Parameter | Symbol | Min. | Max. | Units | Remarks |
|---|---------|-------------|------|--------|---|
| Clock frequency | FCLK | — | 400 | kHz | |
| Clock high time | THIGH | 600 | — | ns | |
| Clock low time | TLOW | 1300 | — | ns | |
| SDA and SCL rise time | TR | — | 300 | ns | (Note 1) |
| SDA and SCL fall time | TF | — | 300 | ns | (Note 1) |
| Start condition hold time | THD:STA | 600 | — | ns | After this period the first clock pulse is generated |
| Start condition setup time | TSU:STA | 600 | — | ns | Only relevant for repeated Start condition |
| Data input hold time | THD:DAT | 0 | — | ns | (Note 2) |
| Data input setup time | TSU:DAT | 100 | — | ns | |
| Stop condition setup time | TSU:STO | 600 | — | ns | |
| Output valid from clock | TAA | — | 900 | ns | (Note 2) |
| Bus free time | TBUF | 1300 | — | ns | Time the bus must be free before a new transmission can start |
| Output fall time from VIH minimum to VIL maximum | TOF | 20 + 0.1 CB | 250 | ns | (Note 1) , CB = 100 pF |
| Input filter spike suppression (SDA and SCL pins) | TSP | — | 50 | ns | (Note 3) |
| Write cycle time | TWR | — | 10 | ms | Byte or Page mode |
| Endurance | — | 1M | — | cycles | 25°C, Vcc = 5V, Block mode (Note 4) |

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

- 2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
- 3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.
- 4:** This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

FIGURE 1-2: BUS TIMING DATA



24C01SC/24C02SC

2.0 FUNCTIONAL DESCRIPTION

The 24C01SC/02SC supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the Start and Stop conditions, while the 24C01SC/02SC works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain high.

3.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

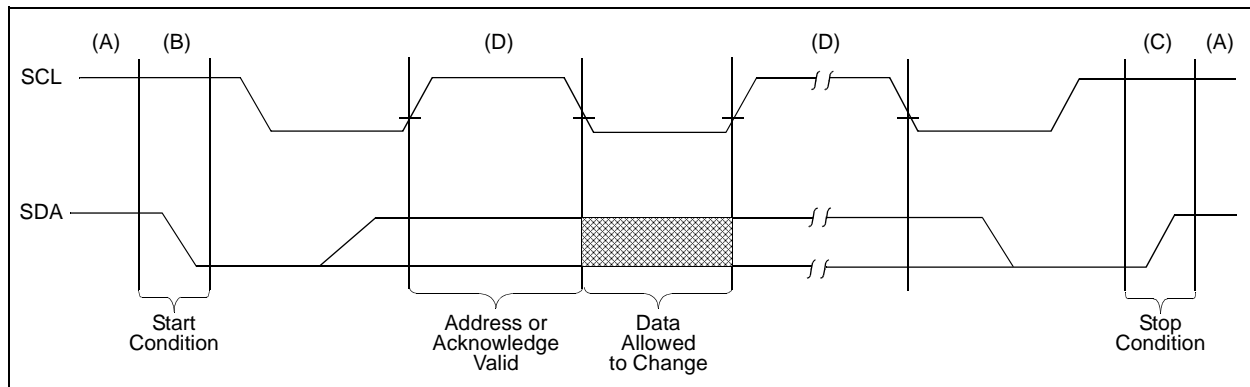
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note: The 24C01SC/02SC does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Slave Address

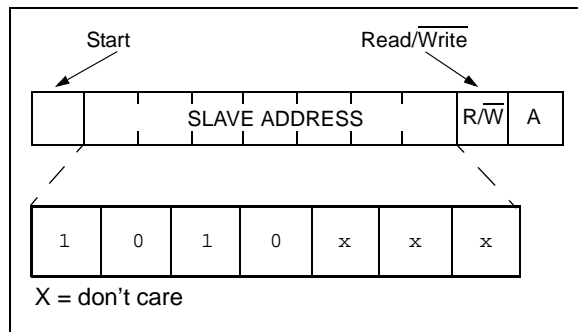
After generating a Start condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24C01SC/02SC, followed by three “don't care” bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24C01SC/02SC (Figure 3-2).

The 24C01SC/02SC monitors the bus for its corresponding slave address all the time. It generates an Acknowledge bit if the slave address was true, and it is not in a programming mode.

| Operation | Control Code | Chip Select | R/W |
|-----------|--------------|-------------|-----|
| Read | 1010 | xxx | 1 |
| Write | 1010 | xxx | 0 |

FIGURE 3-2: CONTROL BYTE ALLOCATION



4.0 WRITE OPERATION

4.1 Byte Write

Following the Start signal from the master, the device code (4 bits), the “don't care” bits (3 bits), and the R/W bit, which is a logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C01SC/02SC. After receiving another Acknowledge signal from the 24C01SC/02SC, the master device will transmit the data word to be written into the addressed memory location. The 24C01SC/02SC acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and during this time the 24C01SC/02SC will not generate Acknowledge signals (Figure 4-1).

4.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the 24C01SC/02SC in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to eight data bytes to the 24C01SC/02SC, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a Stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received an internal write cycle will begin (Figure 4-2).

Note: Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and end at addresses that are integer multiples of [page size - 1]. If a page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

24C01SC/24C02SC

FIGURE 4-1: BYTE WRITE

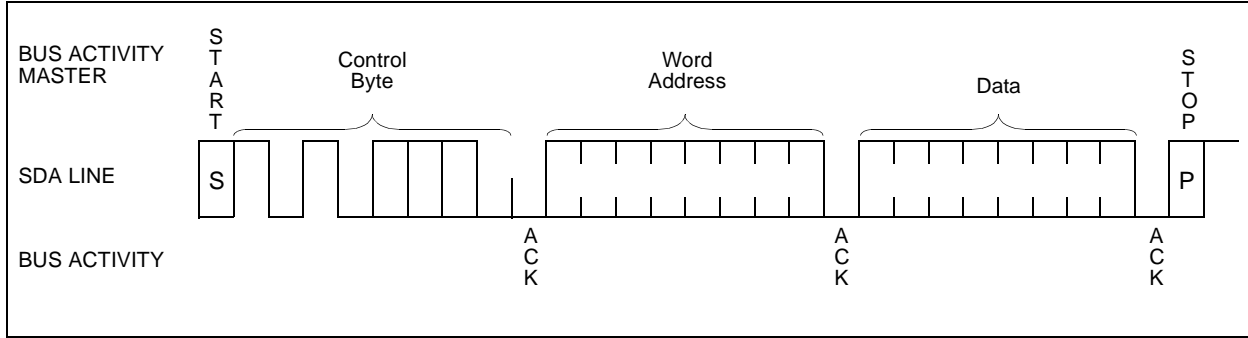
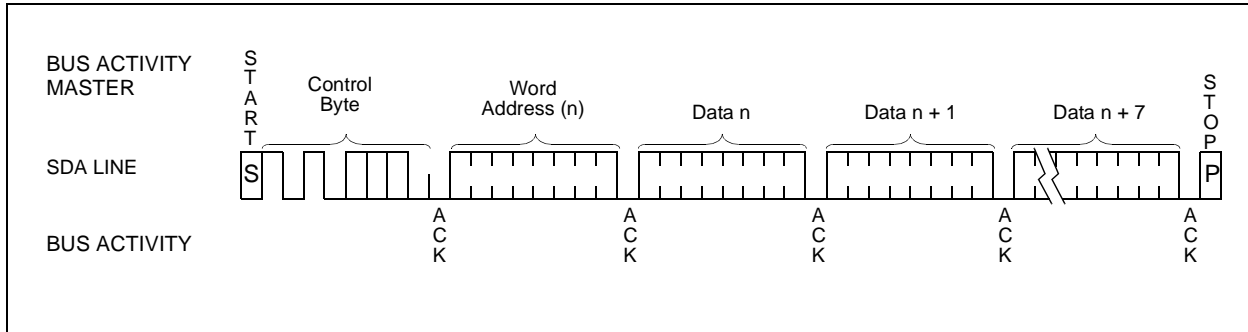


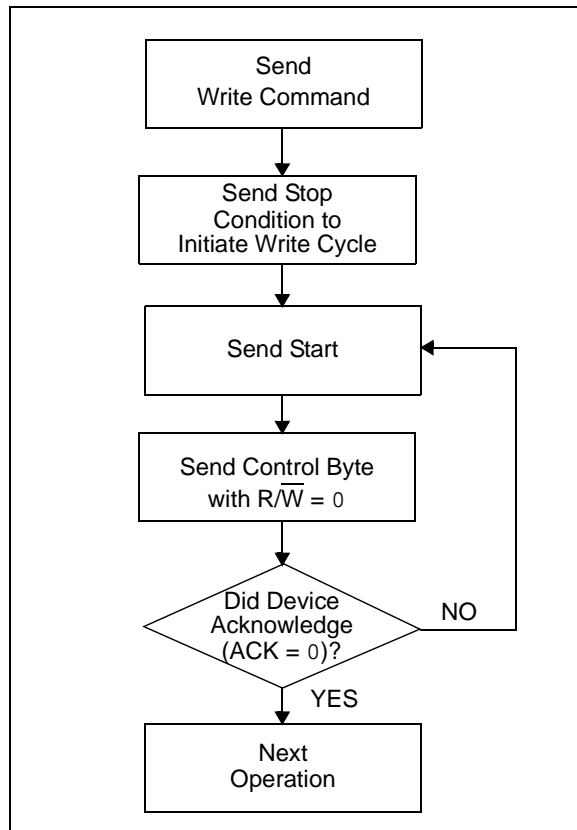
FIGURE 4-2: PAGE WRITE



5.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then NO ACK will be returned. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next Read or Write command. See Figure 5-1 for flow diagram.

FIGURE 5-1: ACKNOWLEDGE POLLING FLOW



6.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/\overline{W} bit of the slave address is set to one. There are three basic types of read operations: current address read, random read and sequential read.

6.1 Current Address Read

The 24C01SC/02SC contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n , the next current address read operation would access data from address $n + 1$. Upon receipt of the slave address with R/\overline{W} bit set to one, the 24C01SC/02SC issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24C01SC/02SC discontinues transmission (Figure 6-1).

6.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C01SC/02SC as part of a write operation. After the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then, the master issues the control byte again but with the R/\overline{W} bit set to a one. The 24C01SC/02SC will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the 24C01SC/02SC discontinues transmission (Figure 6-2).

6.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C01SC/02SC transmits the first data byte, the master issues an acknowledge as opposed to a Stop condition in a random read. This directs the 24C01SC/02SC to transmit the next sequentially addressed 8-bit word (Figure 6-3).

To provide sequential reads the 24C01SC/02SC contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

24C01SC/24C02SC

6.4 Noise Protection

The 24C01SC/02SC employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

FIGURE 6-1: CURRENT ADDRESS READ

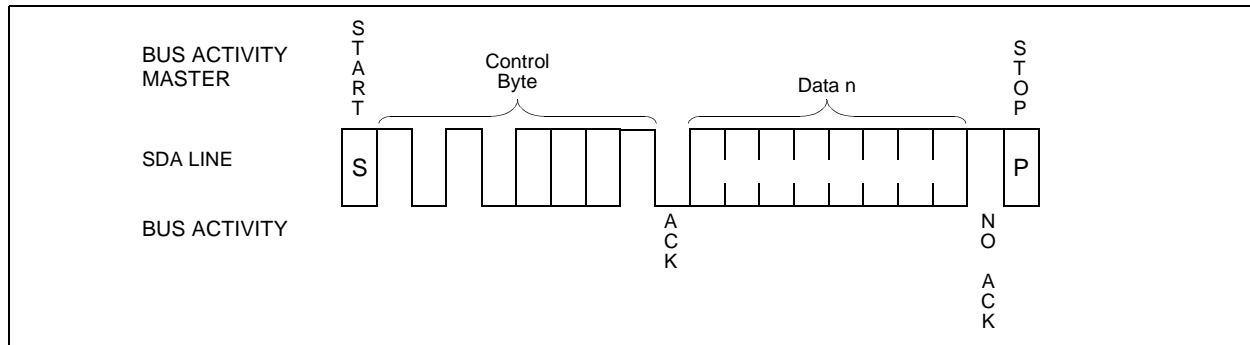


FIGURE 6-2: RANDOM READ

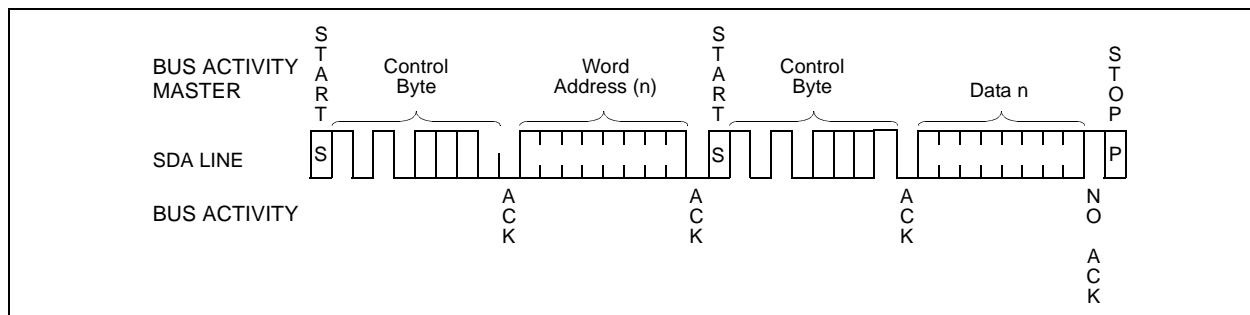
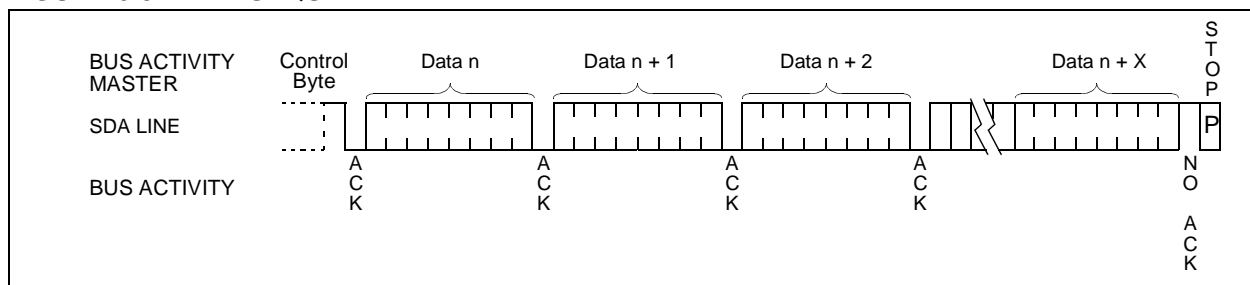


FIGURE 6-3: SEQUENTIAL READ



7.0 PAD DESCRIPTIONS

TABLE 7-1: PAD FUNCTION TABLE

| Name | Function |
|------|----------------------------|
| Vss | Ground |
| SDA | Serial Address/Data I/O |
| SCL | Serial Clock |
| Vcc | +4.5V to 5.5V Power Supply |
| DC | Don't connect |

7.1 SDA Serial Address/Data Input/Output

This is a bidirectional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to Vcc (typical 10K $\frac{3}{4}$ for 100 kHz, 2 K $\frac{3}{4}$ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

7.2 SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

7.3 DC Don't Connect

This pad is used for test purposes and should not be bonded out. It is pulled down to Vss through an internal resistor.

8.0 DIE CHARACTERISTICS

Figure 8-1 shows the die layout of the 24C01SC/02SC, including bondpad positions. Table 8-1 shows the actual coordinates of the bondpad midpoints with respect to the center of the die.

FIGURE 8-1: DIE LAYOUT

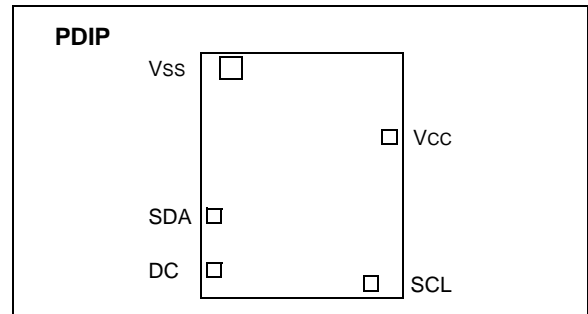


TABLE 8-1: BOND PAD COORDINATES

| Pad Name | Pad Midpoint, X dir. | Pad Midpoint, Y dir. |
|----------|----------------------|----------------------|
| Vss | -495.000 | 749.130 |
| SDA | -605.875 | -271.875 |
| SCL | 479.875 | -746.625 |
| Vcc | 605.875 | -261.375 |

- Note 1:** Dimensions are in microns.
Note 2: Center of die is at the 0,0 point.

24C01SC/24C02SC

APPENDIX A: REVISION HISTORY

Revision E

Added note to page 1 header (Not recommended for new designs).

Added On-line Support page.

Updated document format.

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape® or Microsoft® Internet Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

<ftp://ftp.microchip.com>

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

042003

24C01SC/24C02SC

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager
RE: Reader Response
Total Pages Sent _____

From: Name _____
Company _____
Address _____
City / State / ZIP / Country _____
Telephone: (_____) _____ - _____ FAX: (_____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: 24C01SC/24C02SC

Literature Number: DS21170E

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>X</u> | <u>/XX</u> | <u>XXX</u> |
|-------------------|--|------------|------------|
| Device | Temperature Range | Package | Pattern |
| Device | 24C01SC: 1K I ² C ISO Smart Card Die 24C02SC: 2K I ² C ISO Smart Card Die | | |
| Temperature Range | Blank = 0°C to +70°C | | |
| Package | S = Die in Wafer Pak W = Wafer WF = Sawed Wafer on Frame | | |
| Die Thickness | Blank = 11 mils 08 = 8 mils Other die thicknesses available, please consult factory. | | |

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

24C01SC/24C02SC

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rfPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rfPICDEM, Select Mode, Smart Serial, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2004, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==**

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: www.microchip.com

Atlanta

3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888
Fax: 949-263-1338

San Jose

1300 Terra Bella Avenue
Mountain View, CA 94043
Tel: 650-215-1444
Fax: 650-961-0286

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia

Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Unit 706B
Wan Tai Bei Hai Bldg.
No. 6 Chaoyangmen Bei Str.
Beijing, 100027, China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu

Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou

Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai

Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde

Room 401, Hongjian Building, No. 2
Fengxiangnan Road, Ronggui Town, Shunde
District, Foshan City, Guangdong 528303, China
Tel: 86-757-28395507 Fax: 86-757-28395571

China - Qingdao

Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India

Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessy Road
Bangalore, 560 025, India
Tel: 91-80-22290061 Fax: 91-80-22290062

Japan

Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea

168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or
82-2-558-5934

Singapore

200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan

Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria

Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France

Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - Ier Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany

Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy

Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands

Waegenburghtplein 4
NL-5152 JR, Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom

505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

05/28/04