# 24C02C

## 2-Kbit 5.0V I²C Serial EEPROM

### Features

- Single-Supply with Operation from 4.5V to 5.5V
- Low-Power CMOS Technology:
  - Read current: 1 mA, maximum
  - Standby current: 5 µA, maximum
- Two-Wire Serial Interface, I²C Compatible
- Cascadable up to Eight Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz and 400 kHz Clock Compatibility
- Fast Page or Byte Write Time: 1 ms, typical
- Self-Timed Erase/Write Cycle
- 16-Byte Page Write Buffer
- Hardware Write-Protect for Upper Half of the Array (80h-FFh)
- High Reliability:
  - More than one million erase/write cycles
  - Data retention >200 years
  - ESD protection >4,000V
- Factory Programming Available
- RoHS Compliant
- Temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C

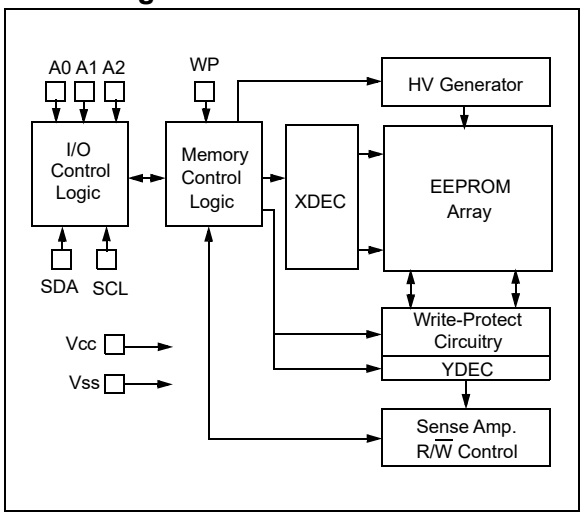
### Packages

8-Lead DFN, 8-Lead MSOP, 8-Lead PDIP,
8-Lead SOIC, 8-Lead TDFN and 8-Lead TSSOP

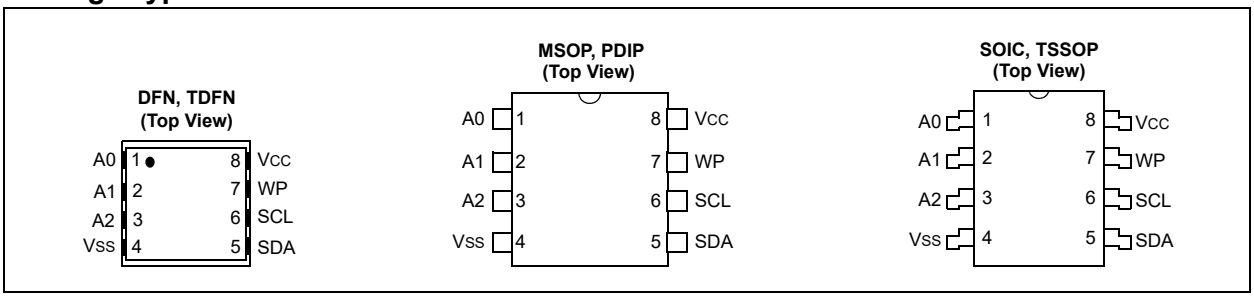
### Description

The Microchip Technology Inc. 24C02C is a 2-Kbit Serial Electrically Erasable PROM (EEPROM) with a voltage range of 4.5V to 5.5V. The device is organized as a single block of 256 x 8-bit memory with a two-wire serial interface. Low-current design permits operation with maximum standby and active currents of only 5 µA and 1 mA, respectively. The device has a page write capability for up to 16 bytes of data and has fast write cycle times of only 1 ms for both byte and page writes. Functional address lines allow the connection of up to eight 24C02C devices on the same bus for up to 16 Kbits of contiguous EEPROM memory.

### Block Diagram




### Package Types



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings(†)

VCC.....7.0V

All inputs and outputs w.r.t. VSS ..... -0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied .....-40°C to +125°C

ESD protection on all pins .....≥4 kV

**† NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: DC CHARACTERISTICS**

| **DC CHARACTERISTICS** | | | **Electrical Characteristics:**<br>**Industrial (I): VCC = +4.5V to 5.5V TA = -40°C to +85°C**<br>**Extended (E): VCC = +4.5V to 5.5V TA = -40°C to +125°C** | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics** | **Min.** | **Max.** | **Units** | **Conditions** |
| D1 | VIH | High-Level Input Voltage | 0.7 VCC | — | V | |
| D2 | VIL | Low-Level Input Voltage | — | 0.3 VCC | V | |
| D3 | VHYS | Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins) | 0.05 VCC | — | V | **Note 1** |
| D4 | VOL | Low-Level Output Voltage | — | 0.40 | V | IOL = 3.0 mA @ VCC = 4.5V |
| D5 | ILI | Input Leakage Current | — | ±1 | µA | VIN = VSS or VCC, WP = VSS |
| D6 | ILO | Output Leakage Current | — | ±1 | µA | VOUT = VSS or VCC |
| D7 | CIN, COUT | Pin Capacitance (all inputs/outputs) | — | 10 | pF | VCC = 5.0V (**Note 1**)<br>TA = +25°C, f = 1 MHz |
| D8 | ICCREAD | Operating Current | — | 1 | mA | VCC = 5.5V, SCL = 400 kHz |
| D9 | ICCWRITE | | — | 3 | mA | VCC = 5.5V |
| D10 | ICCS | Standby Current | — | 5 | µA | VCC = 5.5V, SCL = SDA = VCC<br>WP = VSS |

**Note 1:** This parameter is periodically sampled and not 100% tested.

**TABLE 1-2: AC CHARACTERISTICS**

| AC CHARACTERISTICS | | | Electrical Characteristics:<br>Industrial (I): VCC = +4.5V to 5.5V TA = -40°C to +85°C<br>Extended (E): VCC = +4.5V to 5.5V TA = -40°C to +125°C | | | |
|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic** | **Min.** | **Max.** | **Units** | **Conditions** |
| 1 | FCLK | Clock Frequency | — | 100 | kHz | |
| | | | — | 400 | kHz | I-temp. |
| 2 | THIGH | Clock High Time | 4000 | — | ns | |
| | | | 600 | — | ns | I-temp. |
| 3 | TLOW | Clock Low Time | 4700 | — | ns | |
| | | | 1300 | — | ns | I-temp. |
| 4 | TR | SDA and SCL Rise Time | — | 1000 | ns | **Note 1** |
| | | | — | 300 | ns | I-temp. (**Note 1**) |
| 5 | TF | SDA and SCL Fall Time | — | 300 | ns | I-temp. (**Note 1**) |
| 6 | THD:STA | Start Condition Hold Time | 4000 | — | ns | |
| | | | 600 | — | ns | I-temp. |
| 7 | TSU:STA | Start Condition Setup Time | 4700 | — | ns | |
| | | | 600 | — | ns | I-temp. |
| 8 | THD:DAT | Data Input Hold Time | 0 | — | ns | **Note 2** |
| 9 | TSU:DAT | Data Input Setup Time | 250 | — | ns | |
| | | | 100 | — | ns | I-temp. |
| 10 | TSU:STO | Stop Condition Setup Time | 4000 | — | ns | |
| | | | 600 | — | ns | I-temp. |
| 11 | TAA | Output Valid from Clock | — | 3500 | ns | **Note 2** |
| | | | — | 900 | ns | I-temp. (**Note 2**) |
| 12 | TBUF | Bus Free Time: The time the bus must be free before a new transmission can start | 4700 | — | ns | |
| | | | 1300 | — | ns | I-temp. |
| 13 | TOF | Output Fall Time from VIH Minimum to VIL Maximum, CB ≤ 100 pF | 10 + 0.1CB | 250 | ns | **Note 1** |
| 14 | TSP | Input Filter Spike Suppression (SDA and SCL pins) | — | 50 | ns | **Note 3** |
| 15 | TWC | Write Cycle Time (byte or page) | — | 1.5 | ms | |
| | | | — | 1 | ms | I-temp. |
| 16 | | Endurance | 1,000,000 | — | cycles | +25°C, 5.5V, Page Mode (**Note 4**) |

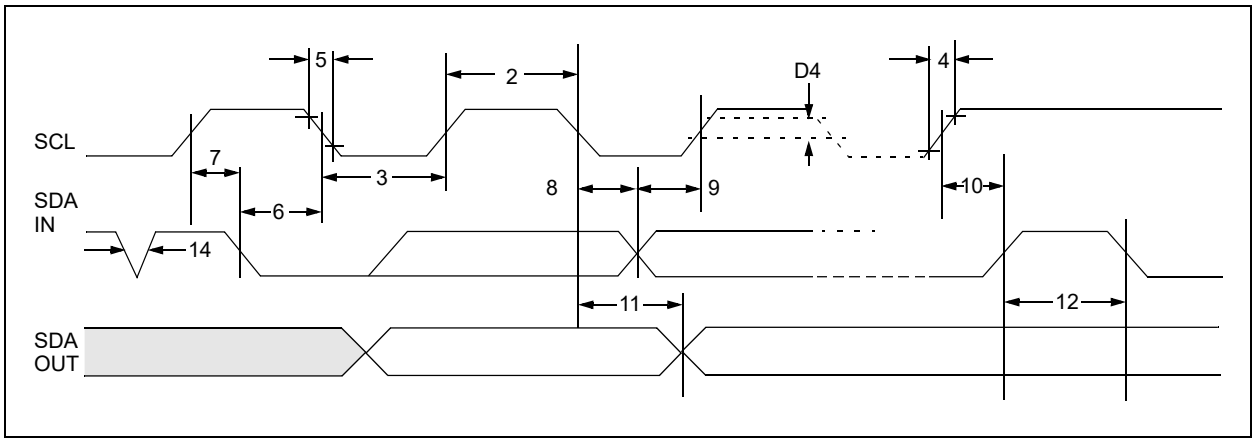
**Note 1:** Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

**4:** This parameter is not tested but ensured by characterization.

**FIGURE 1-1: BUS TIMING DATA**



## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Name | DFN/TDFN[1] | MSOP | PDIP | SOIC | TSSOP | Function |
|---|---|---|---|---|---|---|
| A0 | 1 | 1 | 1 | 1 | 1 | Chip Address Input |
| A1 | 2 | 2 | 2 | 2 | 2 | Chip Address Input |
| A2 | 3 | 3 | 3 | 3 | 3 | Chip Address Input |
| VSS | 4 | 4 | 4 | 4 | 4 | Ground |
| SDA | 5 | 5 | 5 | 5 | 5 | Serial Address/Data I/O |
| SCL | 6 | 6 | 6 | 6 | 6 | Serial Clock |
| WP | 7 | 7 | 7 | 7 | 7 | Write-Protect Input |
| VCC | 8 | 8 | 8 | 8 | 8 | Power Supply |

**Note 1:** The exposed pad on the DFN/TDFN package can be connected to VSS or left floating.

### 2.1 Chip Address Inputs (A0, A1, A2)

The levels on these inputs are compared with the corresponding bits in the client address. The chip is selected if the compare is true.

Up to eight 24C02C devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VCC or VSS.

### 2.2 Serial Address/Data Input/Output (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. Since it is an open-drain terminal, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

### 2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

### 2.4 Write-Protect (WP)

This is the hardware write-protect pin. It must be tied to VCC or VSS. If tied to Vcc, the hardware write protection is enabled and will protect half of the array (80h-FFh). If the WP pin is tied to VSS, the hardware write protection is disabled.

### 2.5 Noise Protection

The 24C02C employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 3.8V at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

## 3.0 FUNCTIONAL DESCRIPTION

The 24C02C supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter while a device receiving data is defined as a receiver. The bus has to be controlled by a host device that generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24C02C works as client. Both host and client can operate as transmitter or receiver, but the host device determines which mode is activated.

## 4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

### 4.1 Bus Not Busy (A)

Both data and clock lines remain high.

### 4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

### 4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

### 4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the host device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a First-In First-Out (FIFO) principle.

### 4.5 Acknowledge

Each receiving device, when addressed, is required to generate an Acknowledge after the reception of each byte. The host device must generate an extra clock pulse, which is associated with this Acknowledge bit.

| **Note:** | The 24C02C does not generate any Acknowledge bits if an internal programming cycle is in progress. |
|---|---|

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. A host must signal an end of data to the client by not generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24C02C) will leave the data line high to enable the host to generate the Stop condition (Figure 4-2).

**FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS**

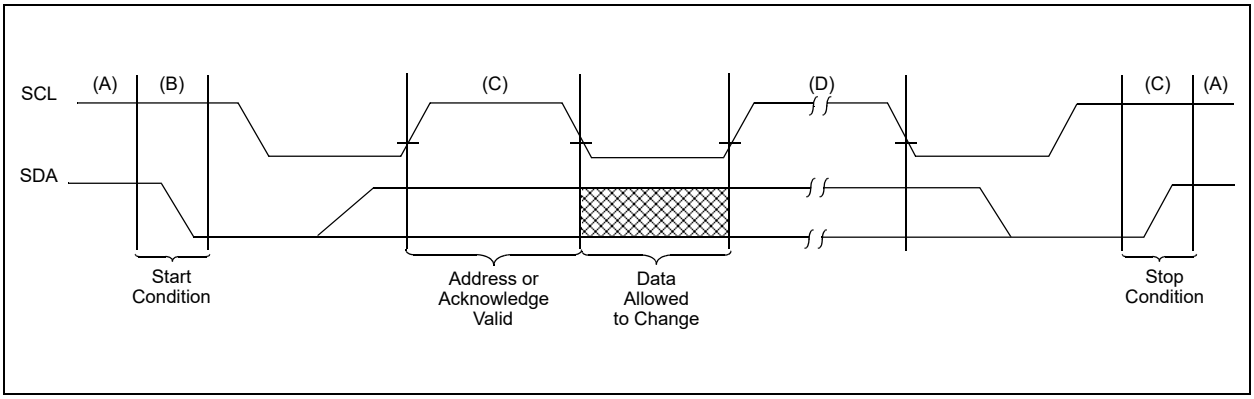
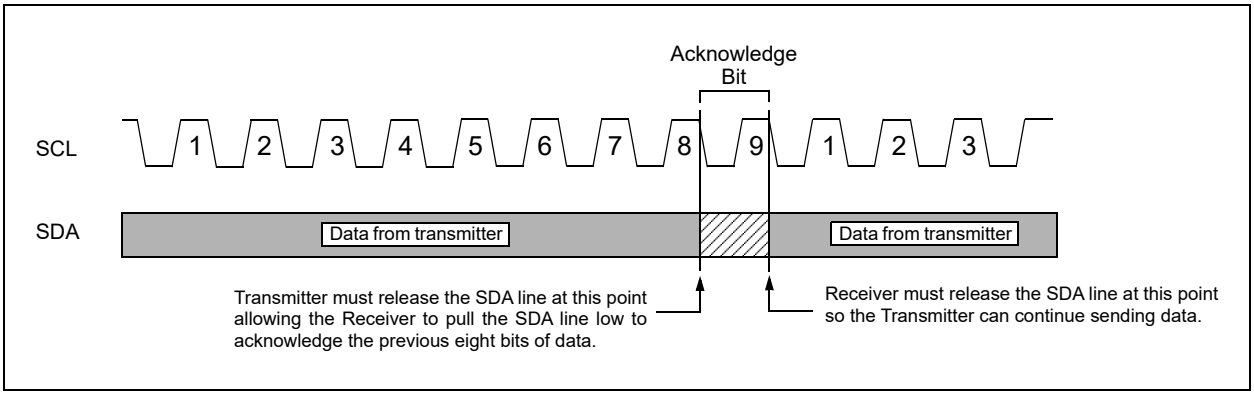



**FIGURE 4-2: ACKNOWLEDGE TIMING**



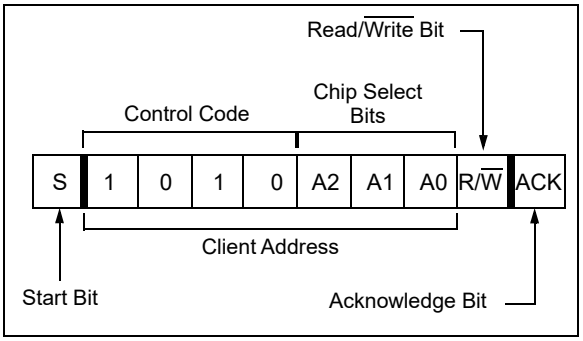
## 5.0 DEVICE ADDRESSING

A control byte is the first byte received following the Start condition from the host device (Figure 5-1). The control byte consists of a 4-bit control code. For the 24C02C, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24C02C devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits are in effect the three Most Significant bits of the word address.

The last bit of the control byte defines the operation to be performed. When set to a '1', a read operation is selected and when set to a '0', a write operation is selected. The next byte received defines the address of the first data byte (Figure 5-2).

Following the Start condition, the 24C02C monitors the SDA bus checking the control byte being transmitted. Upon receiving a '1010' code and appropriate Chip Select bits, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24C02C will select a read or write operation.

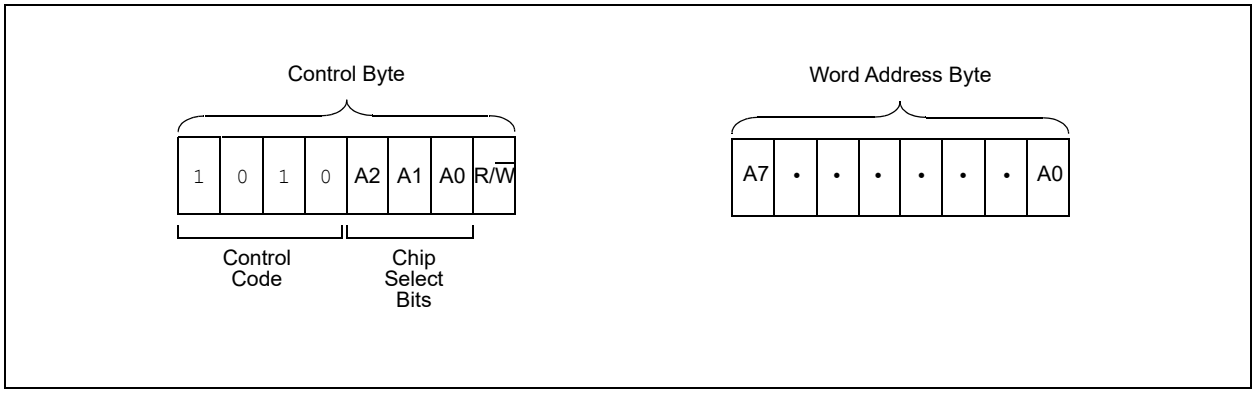
**FIGURE 5-1: CONTROL BYTE FORMAT**




### 5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 16 Kbits by adding up to eight 24C02C devices on the same bus. In this case, software can use A0 of the control byte as address bit A8, A1 as address bit A9 and A2 as address bit A10. It is not possible to write or read across device boundaries.

**FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS**



## 6.0 WRITE OPERATIONS

### 6.1 Byte Write

Following the Start signal from the host, the device code (four bits), the Chip Select bits (three bits) and the R/$\overline{W}$ bit, which is a logic low, is placed onto the bus by the host transmitter. The device will acknowledge this control byte during the ninth clock pulse. The next byte transmitted by the host is the word address and will be written into the Address Pointer of the 24C02C.

After receiving another Acknowledge signal from the 24C02C, the host device will transmit the data word to be written into the addressed memory location. The 24C02C acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and, during this time, the 24C02C will not generate Acknowledge signals (Figure 6-1). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command but no data will be written. The write cycle time must be observed even if the write protection is enabled.

### 6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24C02C in the same way as in a byte write. But instead of generating a Stop condition, the host transmits up to 15 additional data bytes to the 24C02C which are temporarily stored in the on-chip page buffer and will be written into the memory after the host has transmitted a Stop condition. After the receipt of each word, the four lower-order Address Pointer bits are internally incremented by one. The higher-order four bits of the word address remains constant. If the host should transmit more than 16 bytes prior to generating the Stop condition, the Address Pointer will roll over and the previously received data will be overwritten.

As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the protected portion of the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if the write protection is enabled.

| | |
|---|---|
| **Note:** | Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary. |

### 6.3 Write Protection

The WP pin must be tied to VCC or VSS. If tied to VCC, the upper half of the array (080-0FF) will be write-protected. If the WP pin is tied to VSS, then write operations to all address locations are allowed.

**FIGURE 6-1: BYTE WRITE**

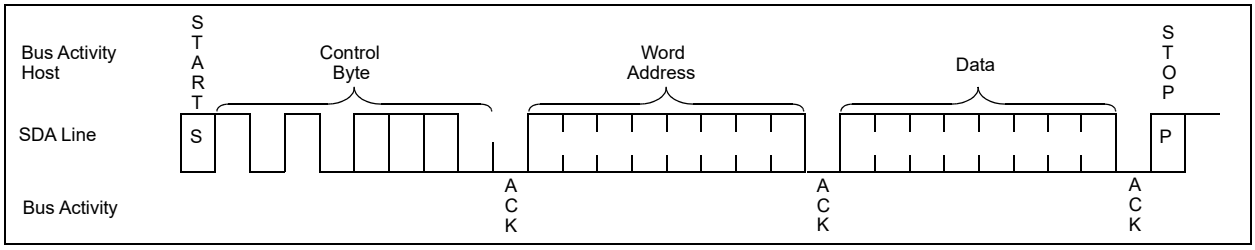
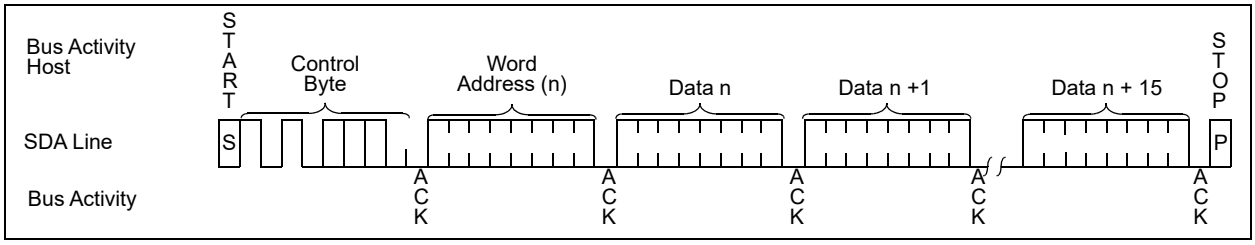


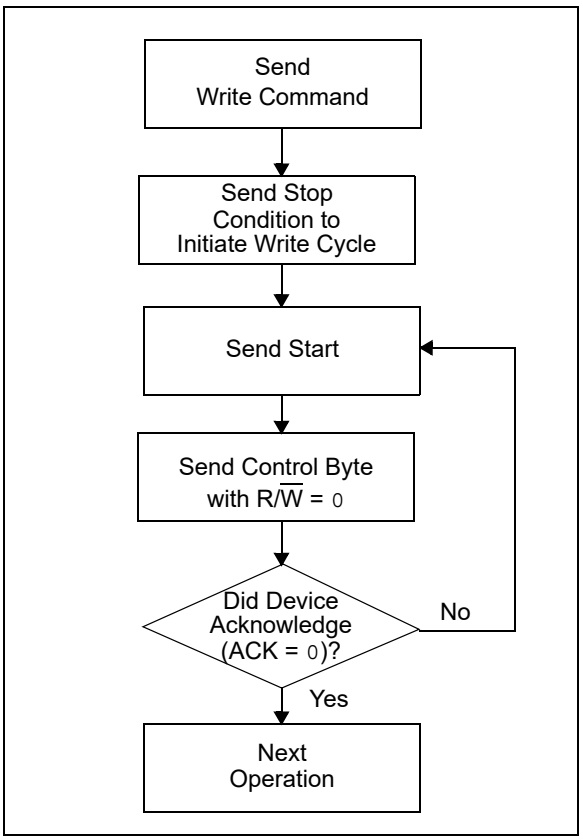

**FIGURE 6-2: PAGE WRITE**



## 7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the host, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the host sending a Start condition followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK and the host can then proceed with the next Read or Write command. See Figure 7-1 for flow diagram.

**FIGURE 7-1: ACKNOWLEDGE POLLING FLOW**



## 8.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the client address is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

### 8.1 Current Address Read

The 24C02C contains an Address Pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address 'n', the next current address read operation would access data from address n + 1. Upon receipt of the client address with the R/$\overline{W}$ bit set to '1', the 24C02C issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24C02C discontinues transmission (Figure 8.1).

### 8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C02C as part of a write operation. After the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again but with the R/$\overline{W}$ bit set to a '1'. The 24C02C will then issue an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24C02C discontinues transmission (Figure 8-2). After this command, the internal Address Pointer will point to the address location following the one that was just read.

### 8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C02C transmits the first data byte, the host issues an Acknowledge as opposed to a Stop condition in a random read. This directs the 24C02C to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 24C02C contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address FF to address 00.

**FIGURE 8-1: CURRENT ADDRESS READ**

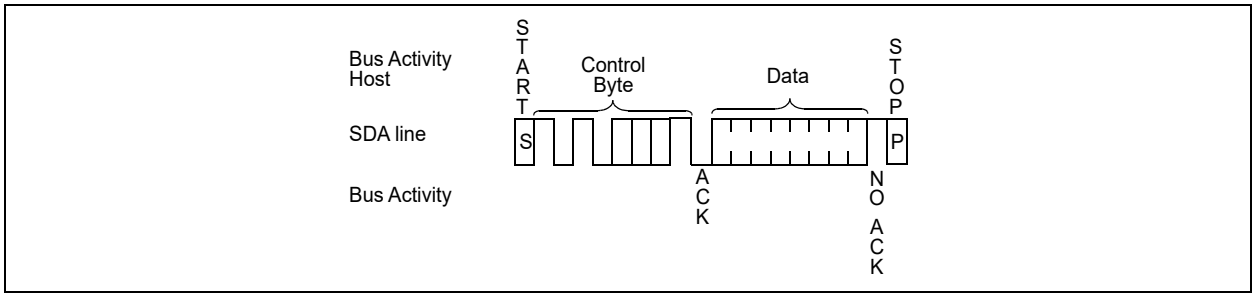


**FIGURE 8-2: RANDOM READ**

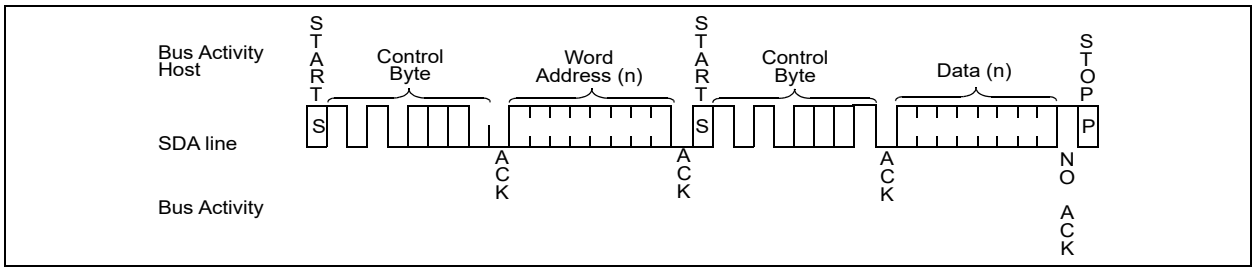
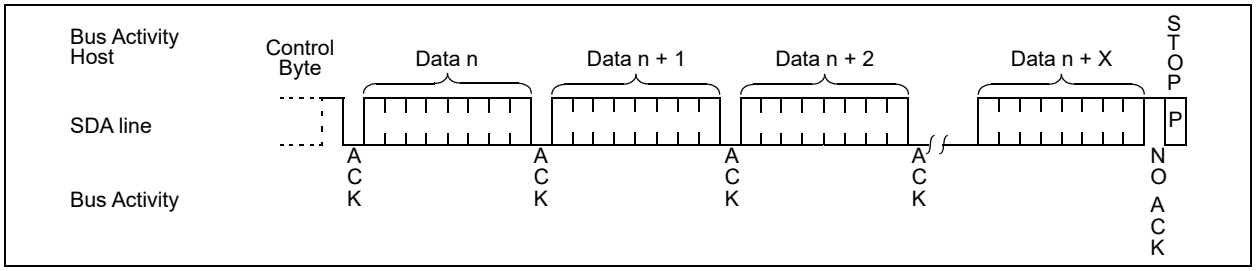



**FIGURE 8-3: SEQUENTIAL READ**

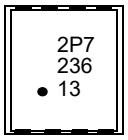


## 9.0 PACKAGING INFORMATION

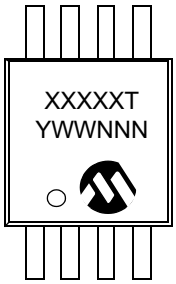
### 9.1 Package Marking Information

8-Lead 2x3 DFN


Example

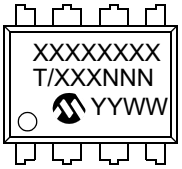



8-Lead MSOP

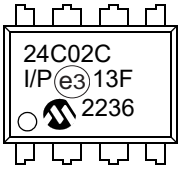



Example

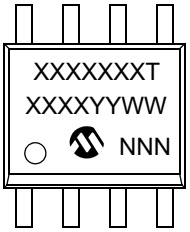

8-Lead PDIP (300 mil)



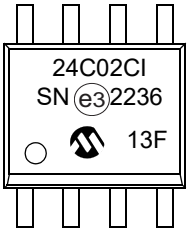

Example



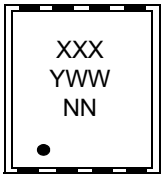

8-Lead SOIC (3.90 mm)



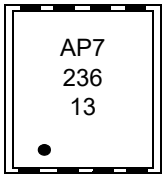

Example



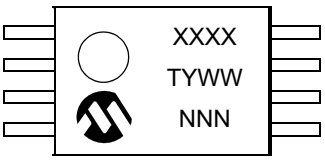

8-Lead 2x3 TDFN



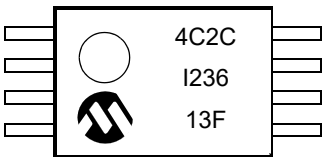

Example




8-Lead TSSOP




Example



| Part Number | 1st Line Marking Codes | | | | | | |
|---|---|---|---|---|---|---|---|
| | DFN | | MSOP | SOIC | TDFN | | TSSOP |
| | I-Temp. | E-Temp. | | | I-Temp. | E-Temp. | |
| 24C02C | 2P7 | 2P8 | 4C2CT | 24C02CT | AP7 | AP8 | 4C2C |

| | | |
|---|---|---|
| **Legend:** | XX...X | Part number or part number code |
| | T | Temperature (I, E) |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code (2 characters for small packages) |
| | (e3) | RoHS-compliant JEDEC® designator for Matte Tin (Sn) |

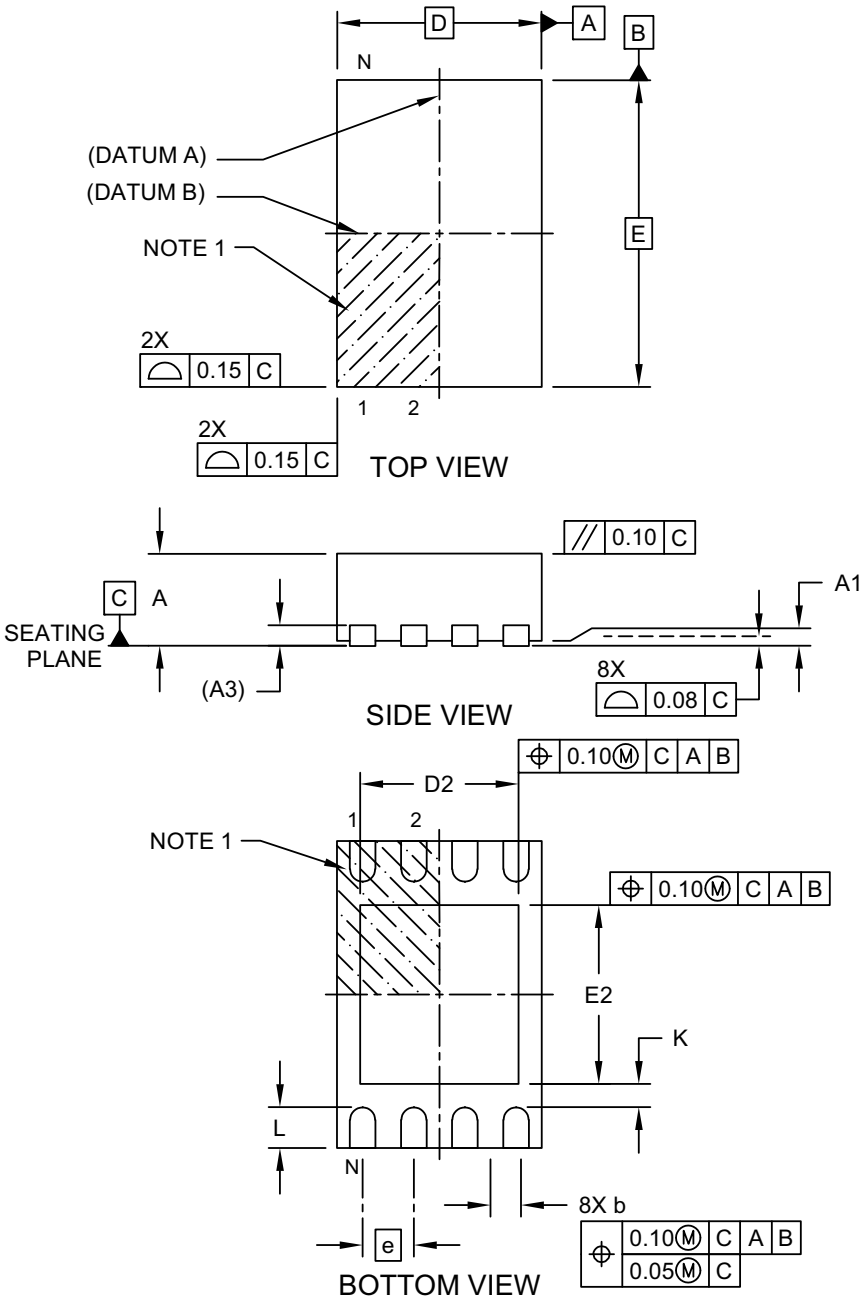
**Note:** Standard OTP marking consists of Microchip part number, year code, week code and traceability code.

**Note:** For very small packages with no room for the RoHS-compliant JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

### 8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

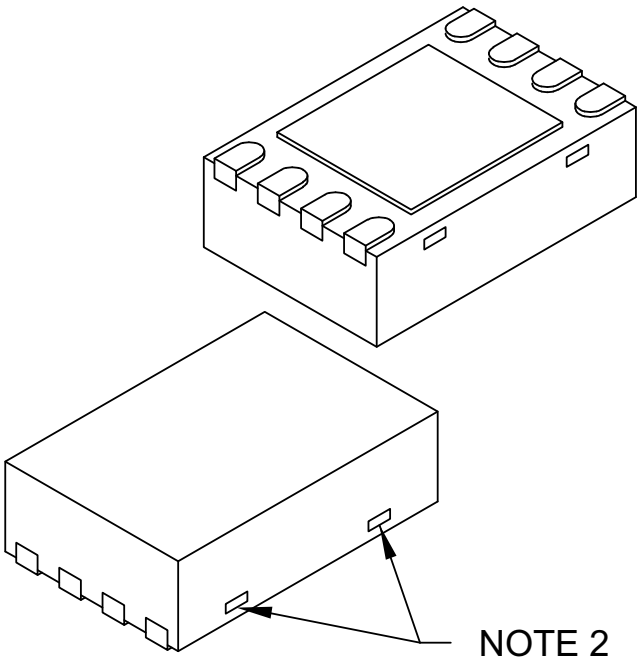
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-123 Rev E Sheet 1 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Exposed Pad Length | D2 | 1.30 | - | 1.55 |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Width | E2 | 1.50 | - | 1.75 |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

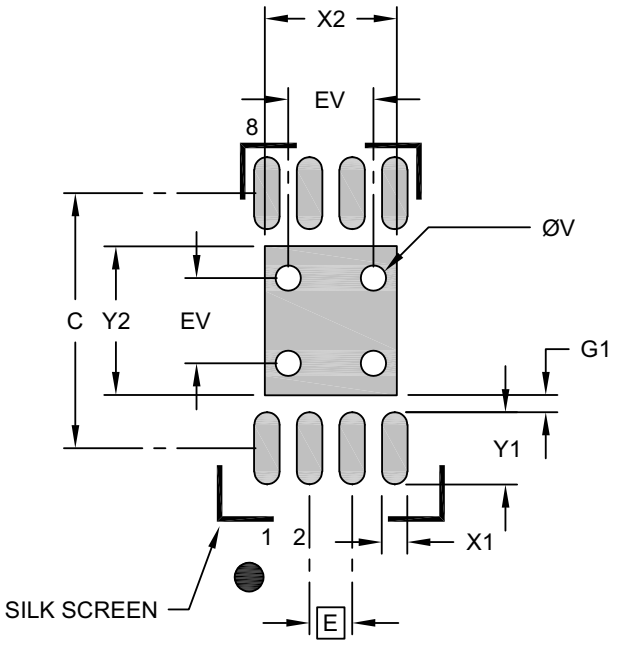
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123 Rev E Sheet 2 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x1 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.55 |
| Optional Center Pad Length | Y2 | | | 1.75 |
| Contact Pad Spacing | C | | 3.00 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Contact Pad to Center Pad (X8) | G1 | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

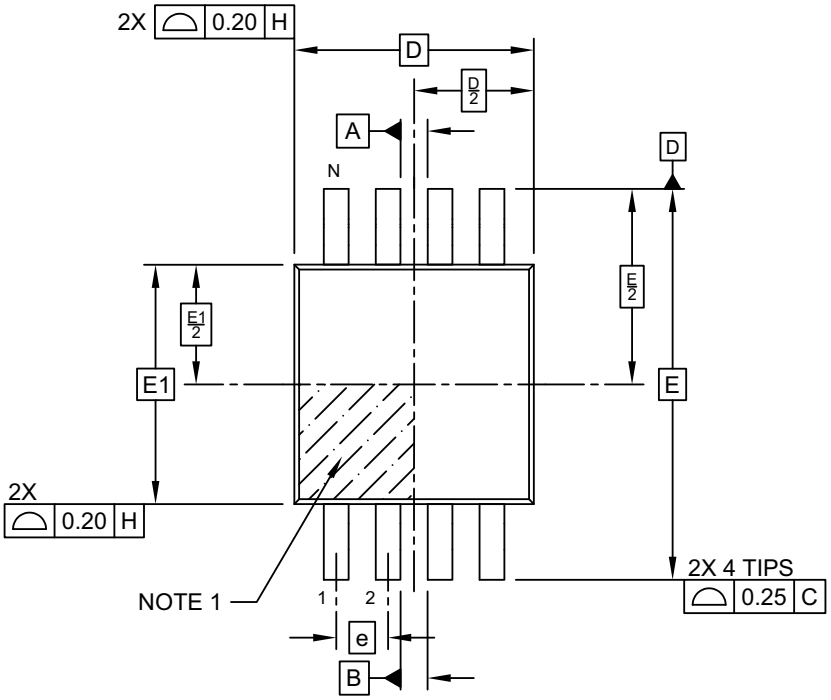
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

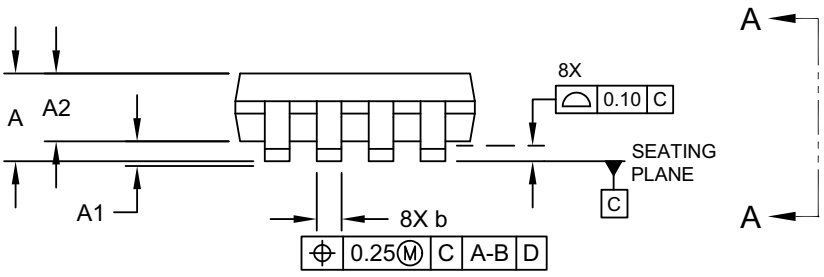
Microchip Technology Drawing C04-2123 Rev E

### 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

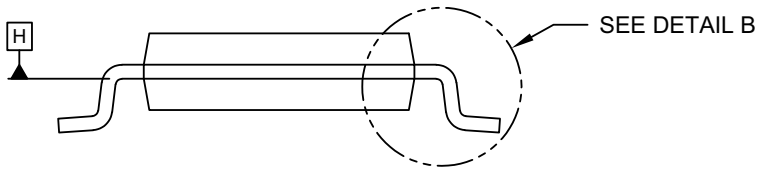
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

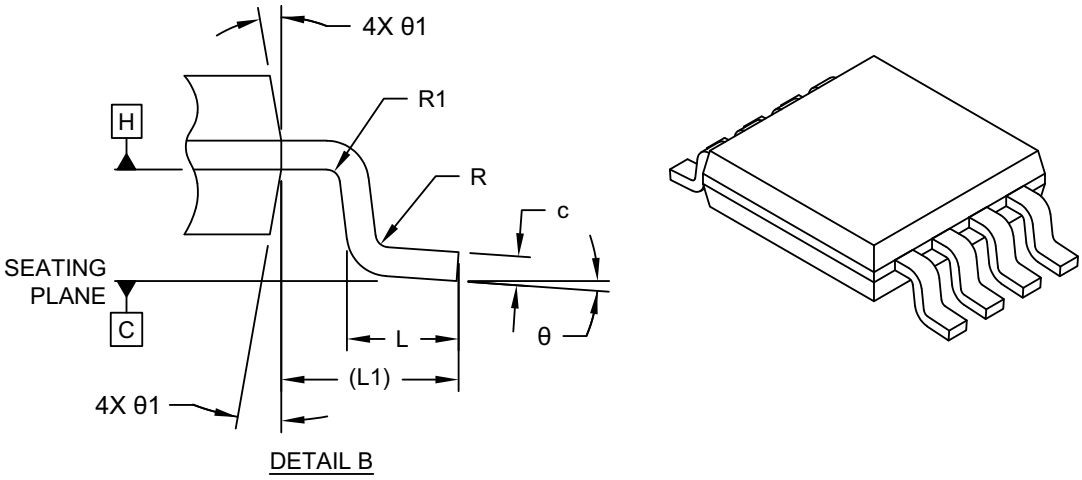



VIEW A–A

Microchip Technology Drawing C04-111-MS Rev D Sheet 1 of 2

## 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Overall Length | D | | 3.00 BSC | |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Terminal Width | b | 0.22 | – | 0.40 |
| Terminal Thickness | c | 0.08 | – | 0.23 |
| Terminal Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |

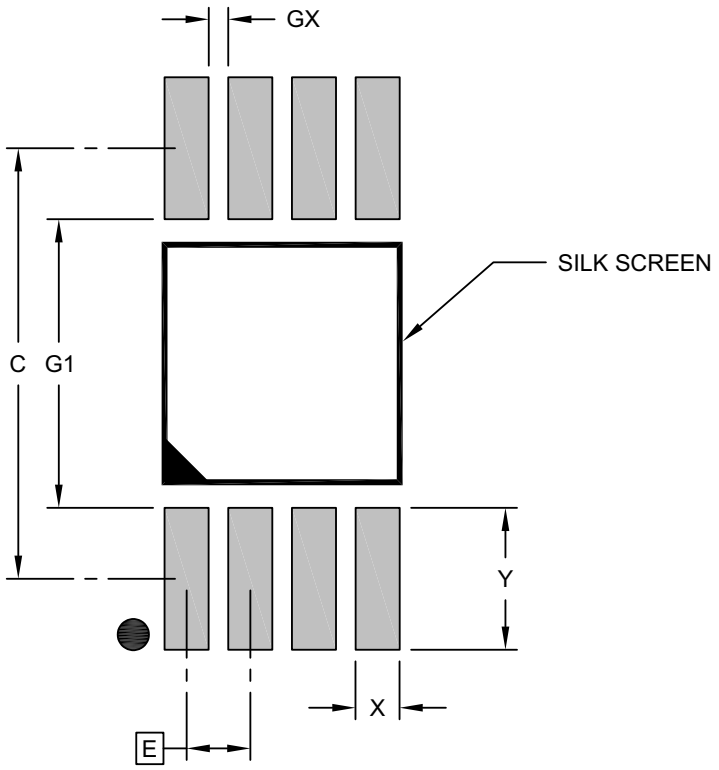
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev D Sheet 2 of 2

### 8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 4.40 | |
| Contact Pad Width (X8) | X | | | 0.45 |
| Contact Pad Length (X8) | Y | | | 1.45 |
| Contact Pad to Contact Pad (X4) | G1 | 2.95 | | |
| Contact Pad to Contact Pad (X6) | GX | 0.20 | | |

Notes:

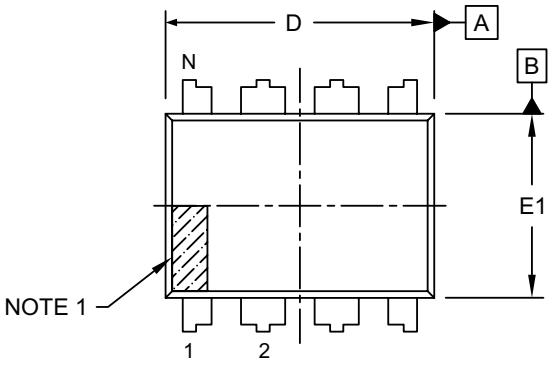
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

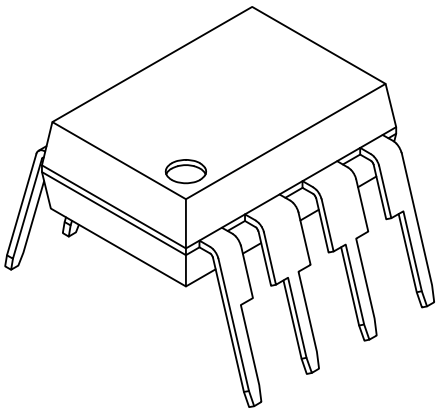
Microchip Technology Drawing C04-2111-MS Rev D

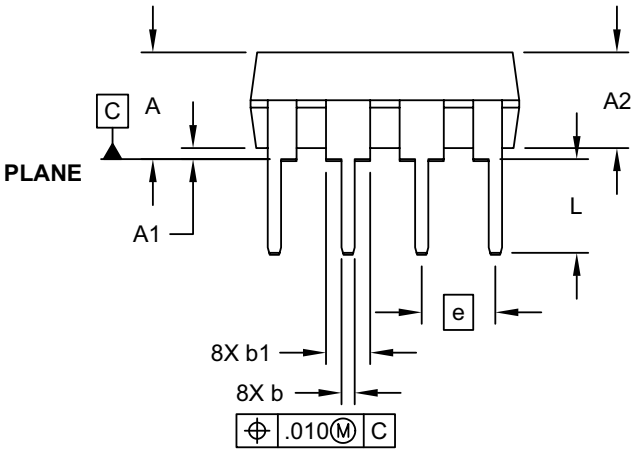
### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

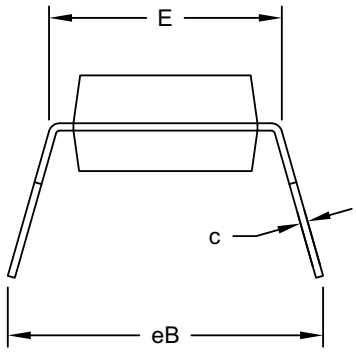



TOP VIEW






SIDE VIEW

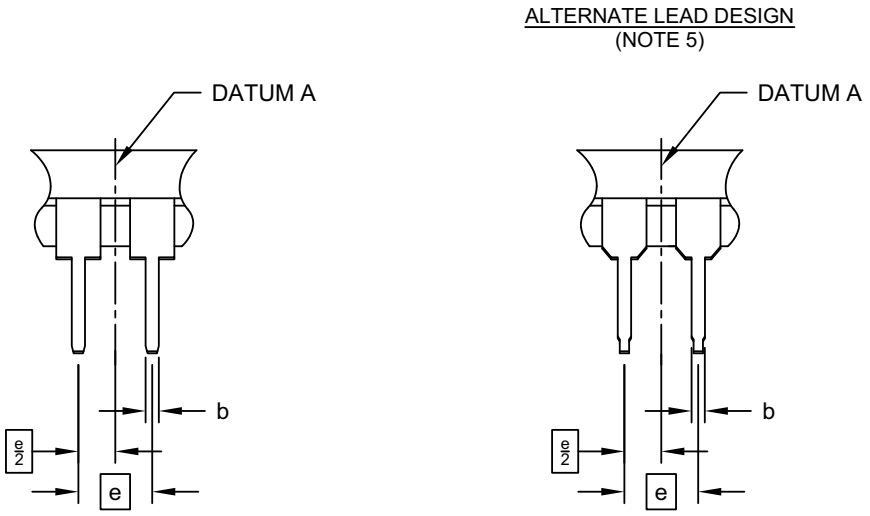



END VIEW

Microchip Technology Drawing No. C04-018-P Rev F Sheet 1 of 2

### 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | - | - | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | - | - |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | - | - | .430 |

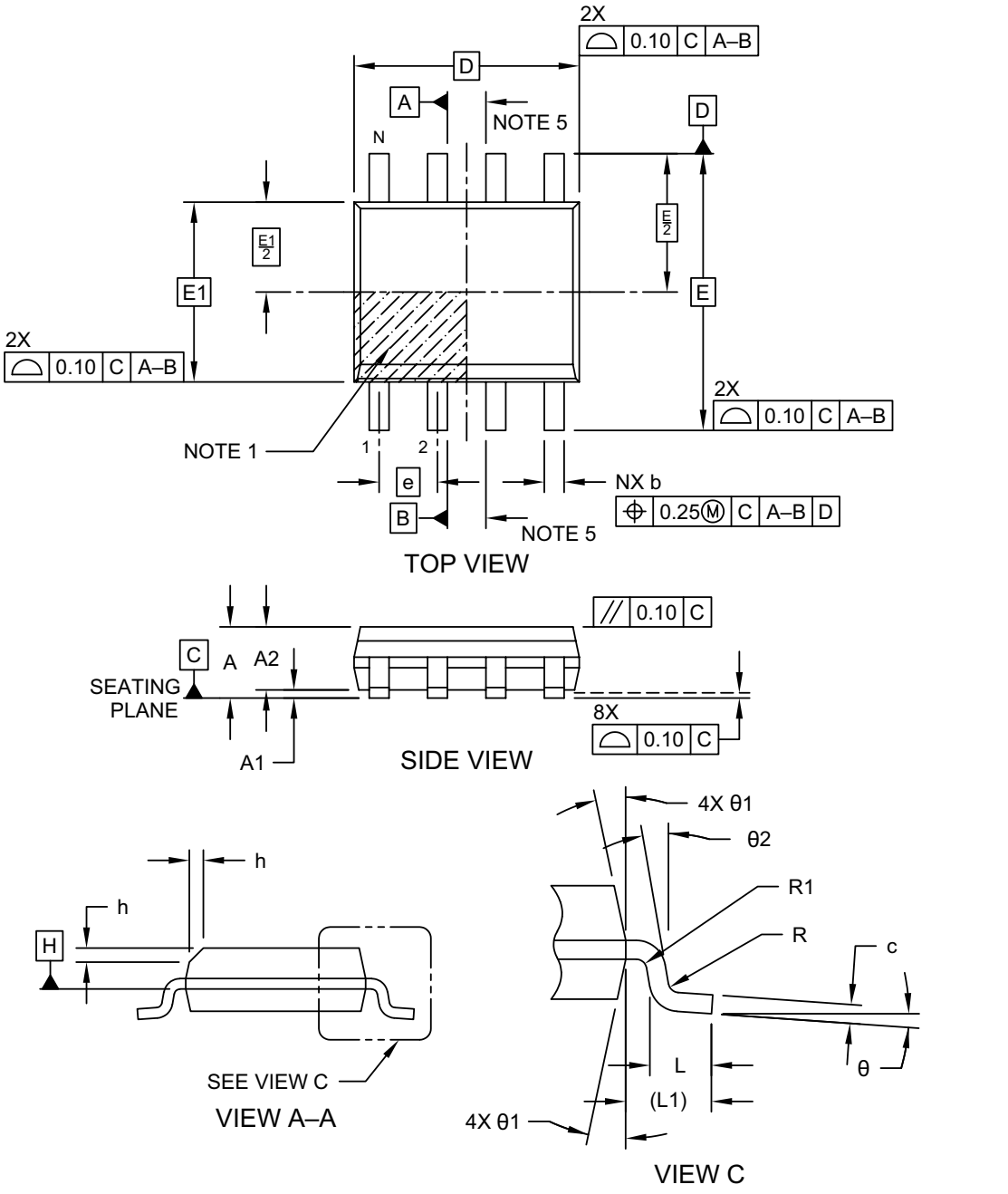
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev F Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

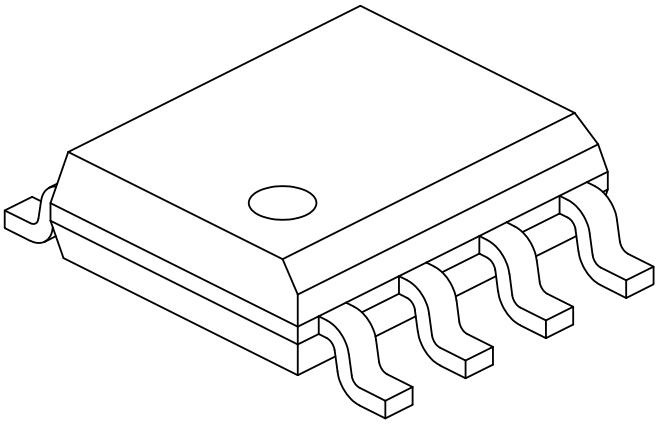
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-057-SN Rev K Sheet 1 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | - |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Lead Bend Radius | R | 0.07 | – | – |
| Lead Bend Radius | R1 | 0.07 | – | – |
| Foot Angle | θ | 0° | – | 8° |
| Mold Draft Angle | θ1 | 5° | – | 15° |
| Lead Angle | θ2 | 0° | – | – |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

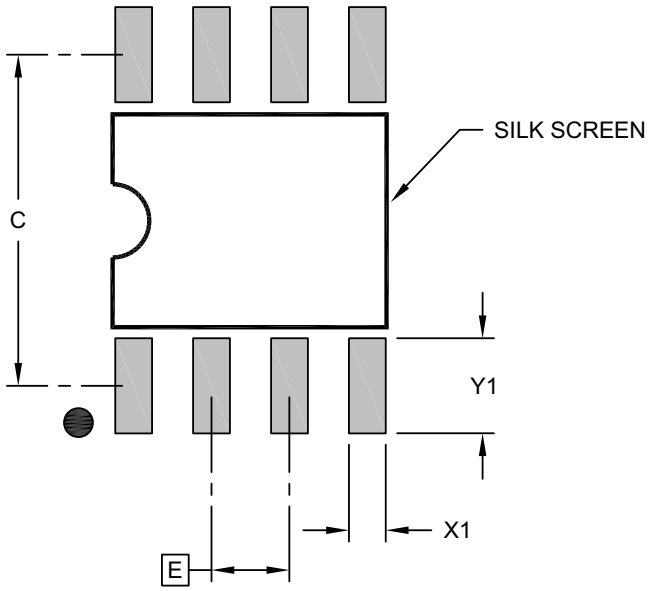
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev K Sheet 2 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

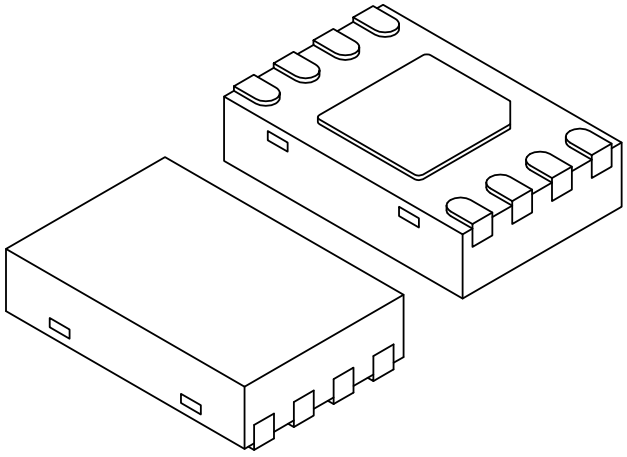
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev K

### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.70 | 0.75 | 0.80 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.35 | 1.40 | 1.45 |
| Exposed Pad Width | E2 | 1.25 | 1.30 | 1.35 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.30 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

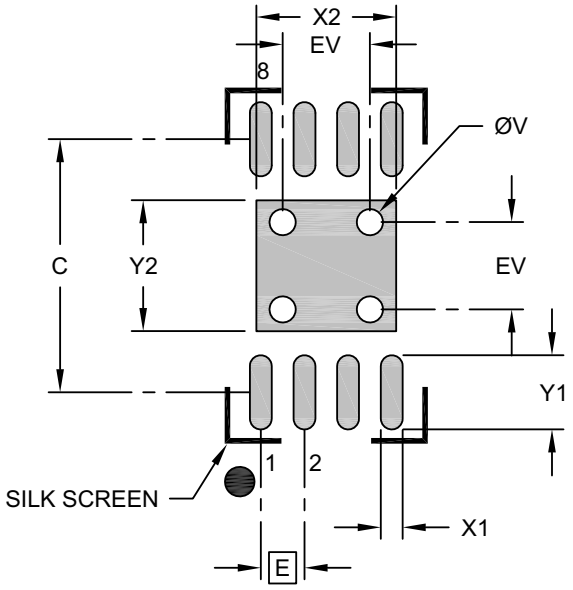
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | X2 | | | 1.60 |
| Optional Center Pad Length | Y2 | | | 1.50 |
| Contact Pad Spacing | C | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.25 |
| Contact Pad Length (X8) | Y1 | | | 0.85 |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

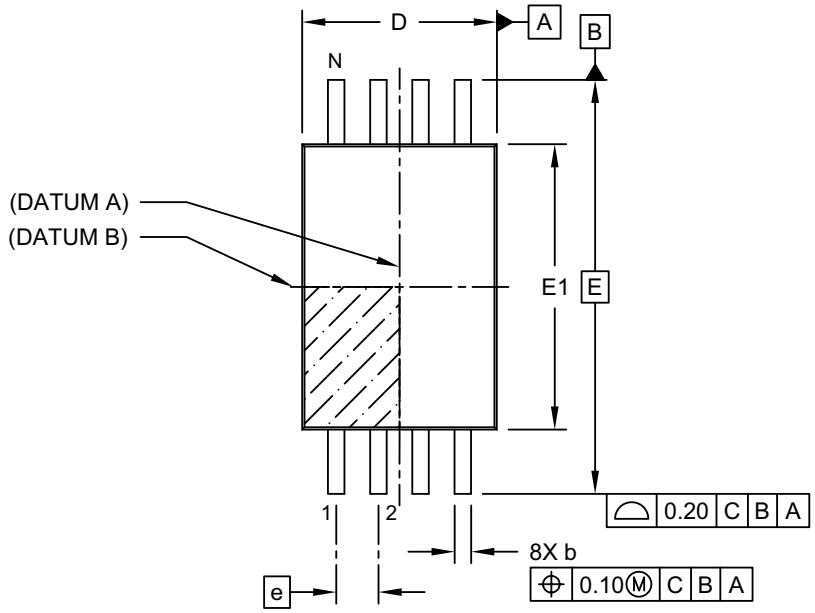
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

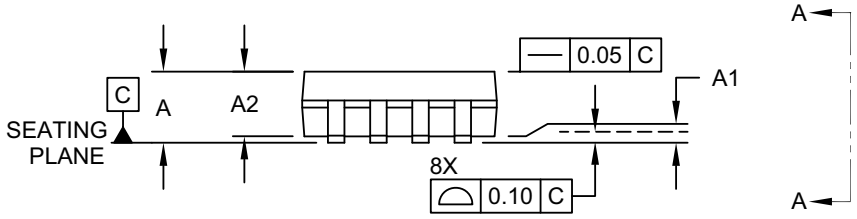
Microchip Technology Drawing No. C04-129-MN Rev. B

### 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

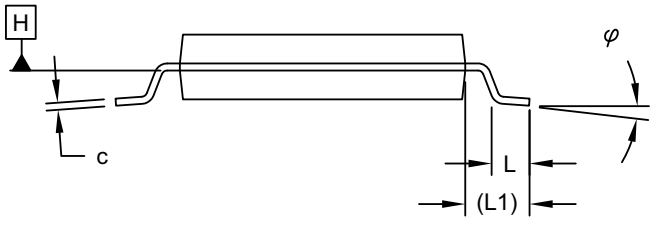
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

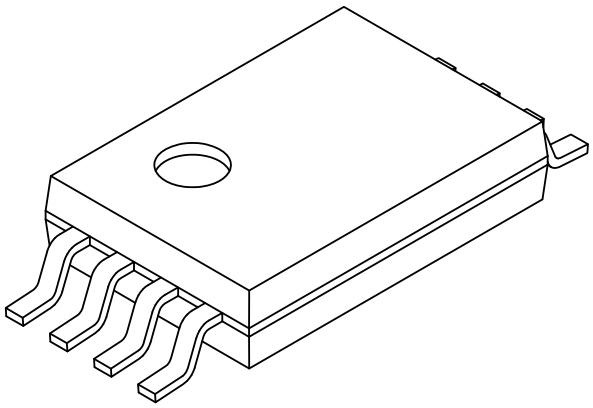



VIEW A-A

Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | - |
| Overall Width | E | | 6.40 BSC | |
| Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
| Overall Length | D | 2.90 | 3.00 | 3.10 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Lead Thickness | c | 0.09 | - | 0.25 |
| Foot Angle | φ | 0° | 4° | 8° |
| Lead Width | b | 0.19 | - | 0.30 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

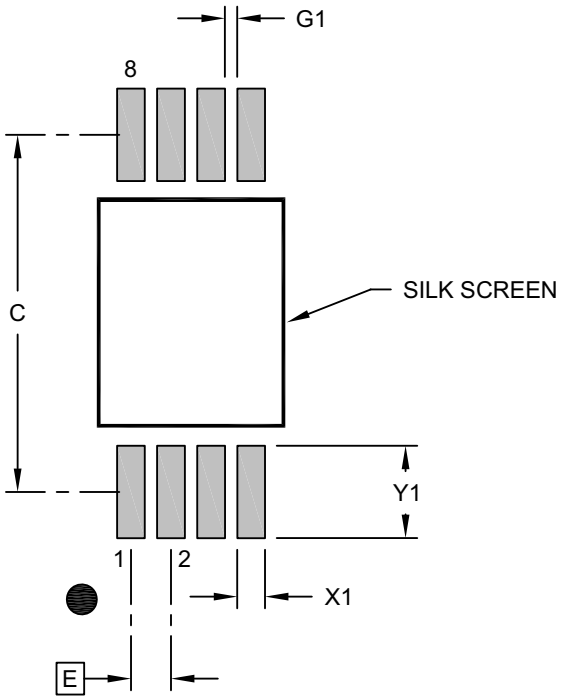
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 5.80 | |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.50 |
| Contact Pad to Center Pad (X6) | G1 | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

# APPENDIX A: REVISION HISTORY

## Revision K (10/2022)

Updated formatting to current template; Updated DFN, MSOP, PDIP, SOIC, TDFN and TSSOP package drawings; Replaced terminology “Master” and “Slave” with “Host” and “Client”, respectively; Replaced “Automotive (E):” designation with “Extended (E):” designation.

## Revision J (08/2008)

Corrections to Table 1-1, DC Characteristics; Updated Table 1-2, AC Characteristics; Revised Figure 1-1; Updated Package Drawings.

## Revision H (04/2008)

Replaced Package Drawings; Added TDFN package; Revised Product ID section.

## Revision G (03/2007)

Replaced Package Drawings (Rev. AM).

## Revision F (02/2007)

Revised Features section; Section 1.0 revised Ambient temperature; Revised Tables 1-1, 1-2, (removed commercial temp); Revised Table 2-1; Replaced On-line Support page; Replaced Package Drawings; Revised Product ID section.

## Revision E

Added DFN package.

## Revision D

Corrections to Section 1.0, Electrical Characteristics.

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| PART NO. | [X](1) | -X | /XX |
|---|---|---|---|
| Device | Tape and Reel Option | Temperature Range | Package |

| | | | |
|---|---|---|---|
| **Device:** | 24C02C | = | 2-Kbit $I^2C$ Serial EEPROM |
| **Tape and Reel Option:** | Blank | = | Standard packaging (tube or tray) |
| | T | = | Tape and Reel(1) |
| **Temperature Range:** | I | = | -40°C to +85°C (Industrial) |
| | E | = | -40°C to +125°C (Extended) |
| **Package:** | MC | = | Plastic Dual Flat, No Lead – 2x3x1 mm Body, 8-Lead (DFN) |
| | MS | = | Plastic Micro Small Outline Package, 8-Lead (MSOP) |
| | P | = | Plastic Dual In-Line – 300 mil Body, 8-Lead (PDIP) |
| | SN | = | Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC) |
| | MNY(2) | = | Plastic Dual Flat, No Lead Package - 2x3x0.75 mm Body, 8-Lead (TDFN) (Tape and Reel only) |
| | ST | = | Plastic Thin Shrink Small Outline – 4.4 mm, 8-Lead (TSSOP) |

**Examples:**

a) 24C02C-I/P: 5.0V Serial EEPROM, Industrial Temperature, PDIP package.

b) 24C02C-E/SN: 5.0V Serial EEPROM, Extended Temperature, SOIC package.

c) 24C02CT-I/MNY: 5.0V Serial EEPROM, Tape and Reel, Industrial Temperature, TDFN package.

d) 24C02CT-E/MS: 5.0V Serial EEPROM, Tape and Reel, Extended Temperature, MSOP package.

e) 24C02C-E/MC: 5.0V Serial EEPROM, Extended Temperature, DFN package.

f) 24C02CT-E/MNY: 5.0V Serial EEPROM, Tape and Reel, Extended Temperature, TDFN package.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**2:** “Y” indicates a Nickel Palladium Gold (NiPdAu) finish.

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