SIEMENS

Standard EEPROM ICs

SLx 24C64

64 Kbit (8192 × 8 bit)
Serial CMOS-EEPROM with
I^2C Synchronous 2-Wire Bus

Data Sheet Preliminary 1998-07-27

SLx 24C64 **Revision History:**		**Current Version: Preliminary 1998-07-27**
Previous Version:		05.98
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
3	3	Text was changed to “Typical programming time 5 ms for up to 32 bytes”.
11, 12	11, 13	The erase/write cycle is finished latest after ~~10~~ 8 ms.
21	21	The write or erase cycle is finished latest after ~~10~~ 4 ms.
24	24	The line “erase/write cycle” was removed.
24	24	Chapter 8.4 “Erase and Write Characteristics” has been added.

I²C Bus

Purchase of Siemens I²C components conveys the license under the Philips I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips.

Edition Preliminary 1998-07-27

Published by Siemens AG,
Bereich Halbleiter, Marketing-
Kommunikation, Balanstraße 73,
81541 München

Attention please!

As far as patents or other rights of third parties are concerned, liability is only assumed for components, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

For questions on technology, delivery and prices please contact the Semiconductor Group Offices in Germany or the Siemens Companies and Representatives worldwide (see address list).

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Siemens Office, Semiconductor Group.

Siemens AG is an approved CECC manufacturer.

Packing

Please use the recycling operators known to you. We can also help you – get in touch with your nearest sales office. By agreement we will take packing material back, if it is sorted. You must bear the costs of transport.

For packing material that is returned to us unsorted or which we are not obliged to accept, we shall have to invoice you for any costs incurred.

Components used in life-support devices or systems must be expressly authorized for such purpose!

Critical components[1] of the Semiconductor Group of Siemens AG, may only be used in life-support devices or systems[2] with the express written approval of the Semiconductor Group of Siemens AG.

1 A critical component is a component used in a life-support device or system whose failure can reasonably be expected to cause the failure of that life-support device or system, or to affect its safety or effectiveness of that device or system.

2 Life support devices or systems are intended (a) to be implanted in the human body, or (b) to support and/or maintain and sustain human life. If they fail, it is reasonable to assume that the health of the user may be endangered.

SIEMENS

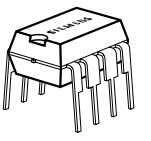
64 Kbit (8192 × 8 bit) Serial CMOS EEPROMs, I²C Synchronous 2-Wire Bus

SLx 24C64

Preliminary

Features

- **Data EEPROM internally organized as 8192 bytes and 256 pages × 32 bytes**
- **Page Protection Mode for protecting the EEPROM against unintended data changes (SLx 24C64.../P types only)**
- **Low power CMOS**
- **V_{CC} = 2.7 to 5.5 V operation**
- **Two wire serial interface bus, I²C-Bus compatible**
- **Three chip select pins to address 8 devices**
- **Filtered inputs for noise suppression with Schmitt trigger**
- **Clock frequency up to 400 kHz**
- **High programming flexibility**
  - Internal programming voltage
  - Self timed programming cycle including erase
  - Byte-write and page-write programming, between 1 and 32 bytes
  - Typical programming time 5 ms for up to 32 bytes
- **High reliability**
  - Endurance 10^6 cycles[1)]
  - Data retention 40 years[1)]
  - ESD protection 4000 V on all pins
- **8 pin DIP/DSO packages**
- **Available for extended temperature ranges**
  - Industrial: – 40 °C to + 85 °C
  - Automotive: – 40 °C to + 125 °C



P-DIP-8-4

P-DSO-8-3

1) Values are temperature dependent, for further information please refer to your Siemens sales office.

Ordering Information

Type	Ordering Code	Package	Temperature	Voltage
SLA 24C64-D SLA 24C64-D/P	Q67100-H3768 Q67100-H3762	P-DIP-8-4	– 40 °C … + 85 °C	4.5 V...5.5 V
SLA 24C64-S SLA 24C64-S/P	Q67100-H3767 Q67100-H3761	P-DSO-8-3	– 40 °C … + 85 °C	4.5 V...5.5 V
SLA 24C64-D-3 SLA 24C64-D-3/P	Q67100-H3766 Q67100-H3760	P-DIP-8-4	– 40 °C … + 85 °C	2.7 V...5.5 V
SLA 24C64-S-3 SLA 24C64-S-3/P	Q67100-H3765 Q67100-H3759	P-DSO-8-3	– 40 °C … + 85 °C	2.7 V...5.5 V
SLE 24C64-D SLE 24C64-D/P	Q67100-H3238 Q67100-H3758	P-DIP-8-4	– 40°C … + 125 °C	4.5 V...5.5 V
SLE 24C64-S SLE 24C64-S/P	Q67100-H3239 Q67100-H3757	P-DSO-8-3	– 40°C … + 125 °C	4.5 V...5.5 V

Other types are available on request:

- Temperature range (– 55 °C … + 150 °C)
- Package (die, wafer delivery)
- 3V types with automotive temperature range (– 40 °C … + 125 °C)

1 Pin Configuration

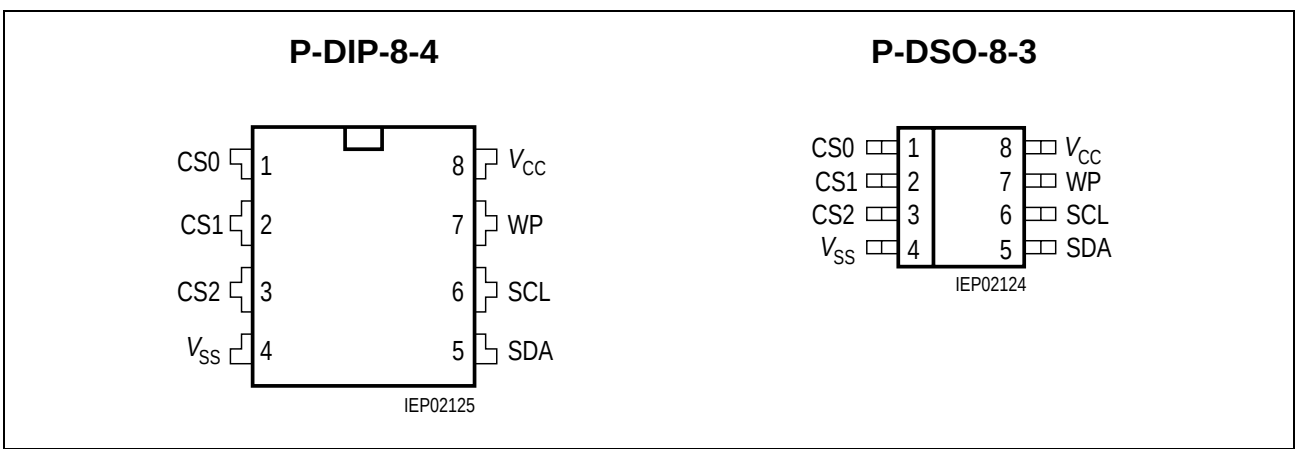


Figure 1
Pin Configuration (top view)

Pin Definitions and Functions

Table 1

Pin No.	Symbol	Function
1, 2, 3	CS0, CS1, CS2	Chip select inputs
4	V_{SS}	Ground
5	SDA	Serial bidirectional data bus
6	SCL	Serial clock input
7	WP	Write protection input
8	V_{CC}	Supply voltage

Pin Description

Serial Clock (SCL)

The SCL input is used to clock data into the device on the rising edge and to clock data out of the device on the falling edge.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer addresses, data or control information into the device or to transfer data out of the device. The output is open drain, performing a wired AND function with any number of other open drain or open collector devices. The SDA bus requires a pull-up resistor to V_{CC}.

Chip Select (CS0, CS1, CS2)

The CS0, CS1 and CS2 pins are chip select inputs either hard wired or actively driven to V_{CC} or V_{SS}. These inputs allow the selection of one of eight possible devices sharing a common bus.

Write Protection (WP)

WP switched to V_{SS} allows normal read/write operations.

WP switched to V_{CC} protects the EEPROM against changes (hardware write protection).

2 Description

The SLx 24C64 device is a serial electrically erasable and programmable read only memory (EEPROM), organized as 8192 × 8 bit. The data memory is divided into 256 pages. The 32 bytes of a page can be programmed simultaneously.

The device conforms to the specification of the 2-wire serial I^2C-Bus. Three chip select pins allow the addressing of 8 devices on the I^2C-Bus. Low voltage design permits operation down to 2.7 V with low active and standby currents. All devices have a minimum endurance of 10^6 erase/write cycles.

The device operates at 5.0 V ± 10% with a maximum clock frequency of 400 kHz and at 2.7 ... 5.5 V with a maximum clock frequency of 100 kHz. The device is available as 5 V type (V_{CC} = 4.5 … 5.5 V) with two temperature ranges for industrial and automotive applications and as 3 V type (V_{CC} = 2.7 … 5.5 V) for industrial applications. The EEPROMs are mounted in eight-pin DIP and DSO packages or are also supplied as chips.

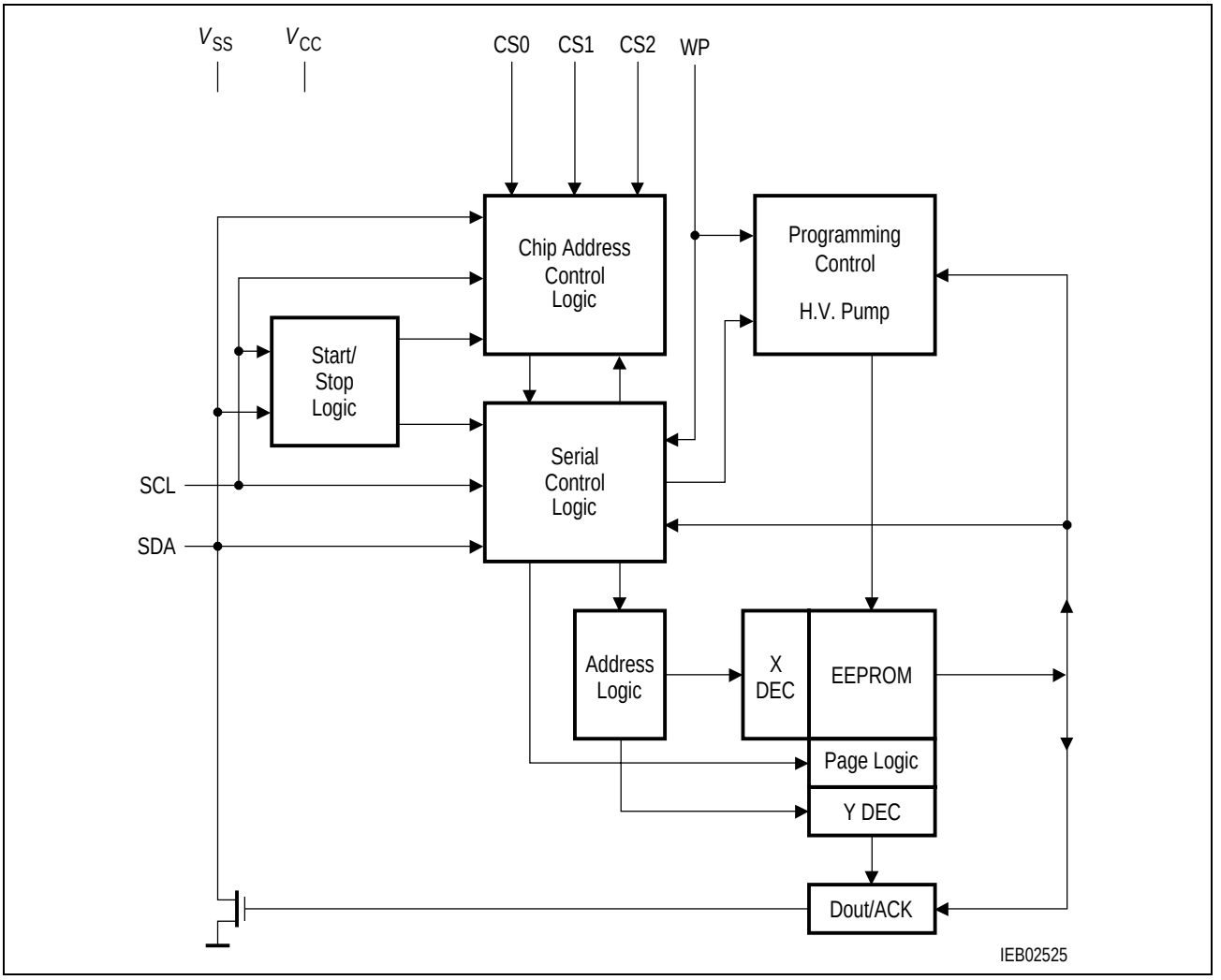


Figure 2
Block Diagram

3 I^2C-Bus Characteristics

Access to the SLx 24C64 device is given via the I^2C bus. This bidirectional bus consists of two wires SCL and SDA for clock and data. The protocol is master/slave oriented, where the serial EEPROM always takes the role of a slave.

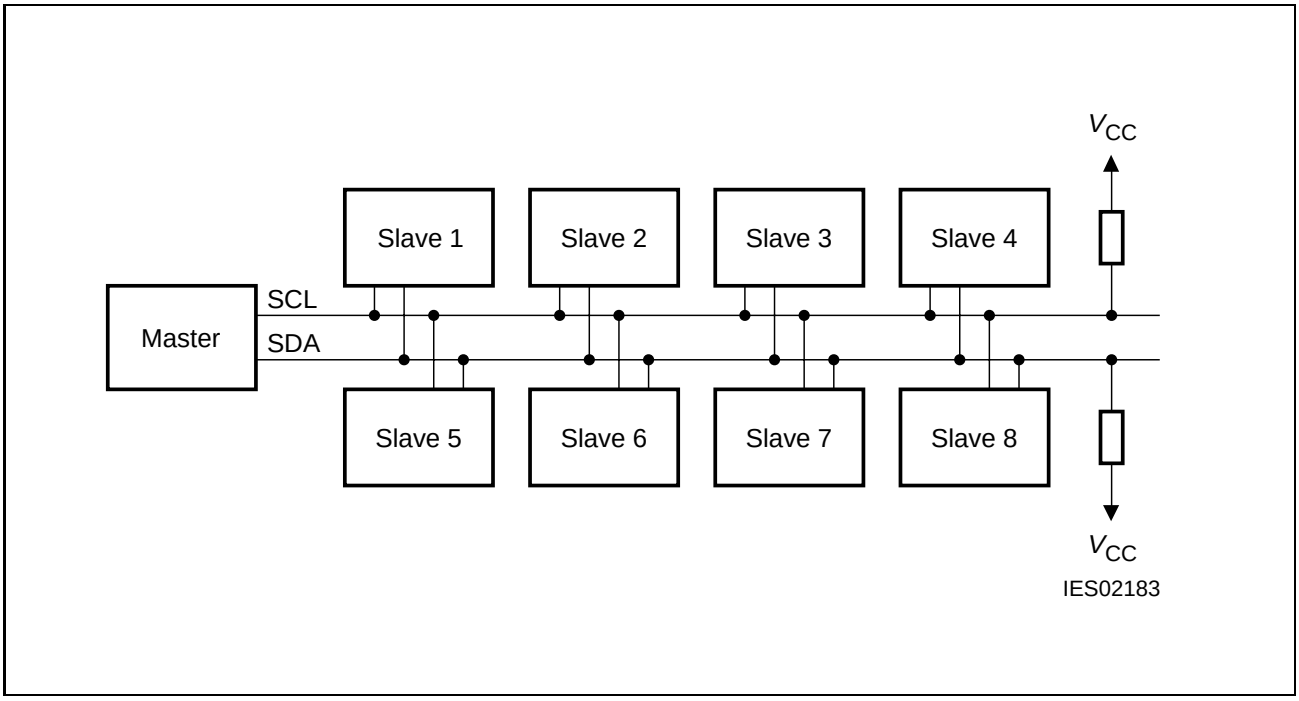


Figure 3
Bus Configuration

Master Device that initiates the transfer of data and provides the clock for transmit and receive operations.

Slave Device addressed by the master, capable of receiving and transmitting data.

Transmitter The device using the SDA as output is defined as the transmitter. Due to the open drain characteristic of the SDA output the device applying a low level wins.

Receiver The device using the SDA as input is defined as the receiver.

The conventions for the serial clock line and the bidirectional data line are shown in **figure 4**.

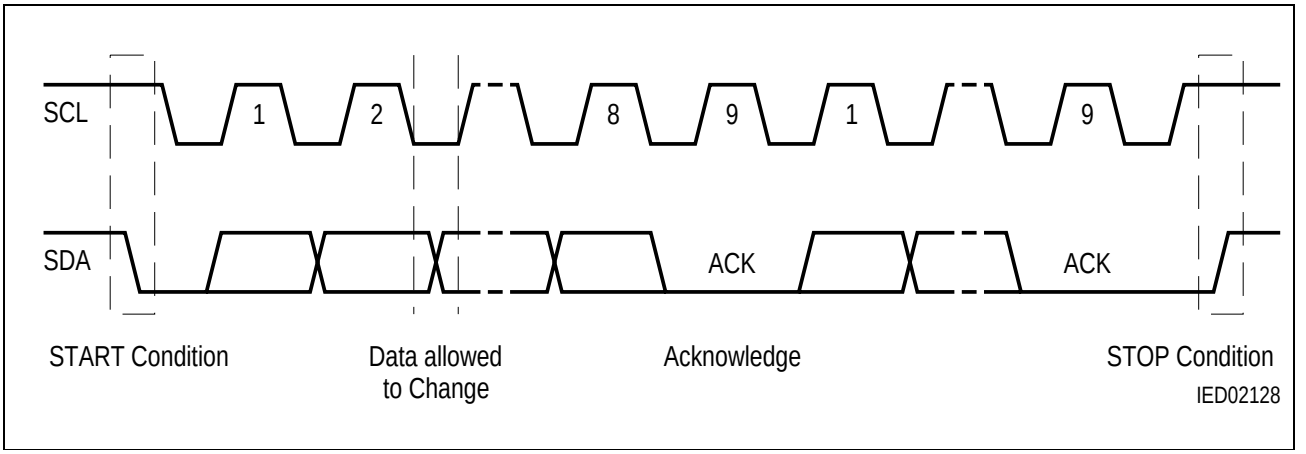


Figure 4
I^2C-Bus Timing Conventions for START Condition, STOP Condition, Data Validation and Transfer of Acknowledge ACK

Standby Mode in which the bus is not busy (no serial transmission, no programming): both clock (SCL) and data line (SDA) are in high state. The device enters the standby mode after a STOP condition or after a programming cycle.

START Condition High to low transition of SDA when SCL is high, preceding all commands.

STOP Condition Low to high transition of SDA when SCL is high, terminating all communications. A STOP condition after writing data initiates an EEPROM programming cycle. A STOP condition after reading data from the EEPROM initiates the standby mode.

Acknowledge A successful reception of eight data bits is indicated by the receiver by pulling down the SDA line during the following clock cycle of SCL (ACK). The transmitter on the other hand has to release the SDA line after the transmission of eight data bits.
The EEPROM as the receiving device responds with an acknowledge, when addressed. The master, on the other side, acknowledges each data byte transmitted by the EEPROM and can at any time end a read operation by releasing the SDA line (no ACK) followed by a STOP condition.

Data Transfer Data must change only during low SCL state, data remains valid on the SDA bus during high SCL state. Nine clock pulses are required to transfer one data byte, the most significant bit (MSB) is transmitted first.

4 Device Addressing and EEPROM Addressing

After a START condition, the master always transmits a command byte CSW or CSR. After the acknowledge of the EEPROM control bytes follow, their contents and the transmitter depend on the previous command byte. The description of the command and control bytes is shown in **table 2**.

Command Byte **Selects one of the 8 addressable slave devices:** The chip select bits CS2, CS1 and CS0 (bit positions b3 to b1) are compared to their corresponding hard wired input pins CS2, CS1 and CS0, respectively.

Selects operation: the least significant bit b0 is low for a write operation (Chip Select Write Command Byte, CSW) or set high for a read operation (Chip Select Read Command Byte, CSR).

Control Bytes **Following CSW (b0 = 0):** The address bytes AHI/ALO containing the address bits A0 to A12 are transmitted by the master.

Following CSR (b0 = 1): The EEPROM transmits the read out data. EEPROM data are read as long as the master pulls down SDA after each byte in order to acknowledge the transfer. The read operation is stopped by the master by releasing SDA (no acknowledge is applied) followed by a STOP condition.

Table 2
Command and Control Byte for I^2C-Bus Addressing of Chip and EEPROM

Command	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
CSW	1	0	1	0	CS2	CS1	CS0	0	chip select for write
CSR	1	0	1	0	CS2	CS1	CS0	1	chip select for read
AHI	0	0	0	A12	A11	A10	A9	A8	high address
ALO	A7	A6	A5	A4	A3	A2	A1	A0	low address
DATA	D7	D6	D5	D4	D3	D2	D1	D0	data byte

The device has an internal address counter which points to the current EEPROM address.

The address counter is incremented
– after a data byte to be written has been acknowledged, during entry of further data byte
– during a byte read, thus the address counter points to the following address after reading a data byte.

The timing conventions for read and write operations are described in **figures 5** and **6**.

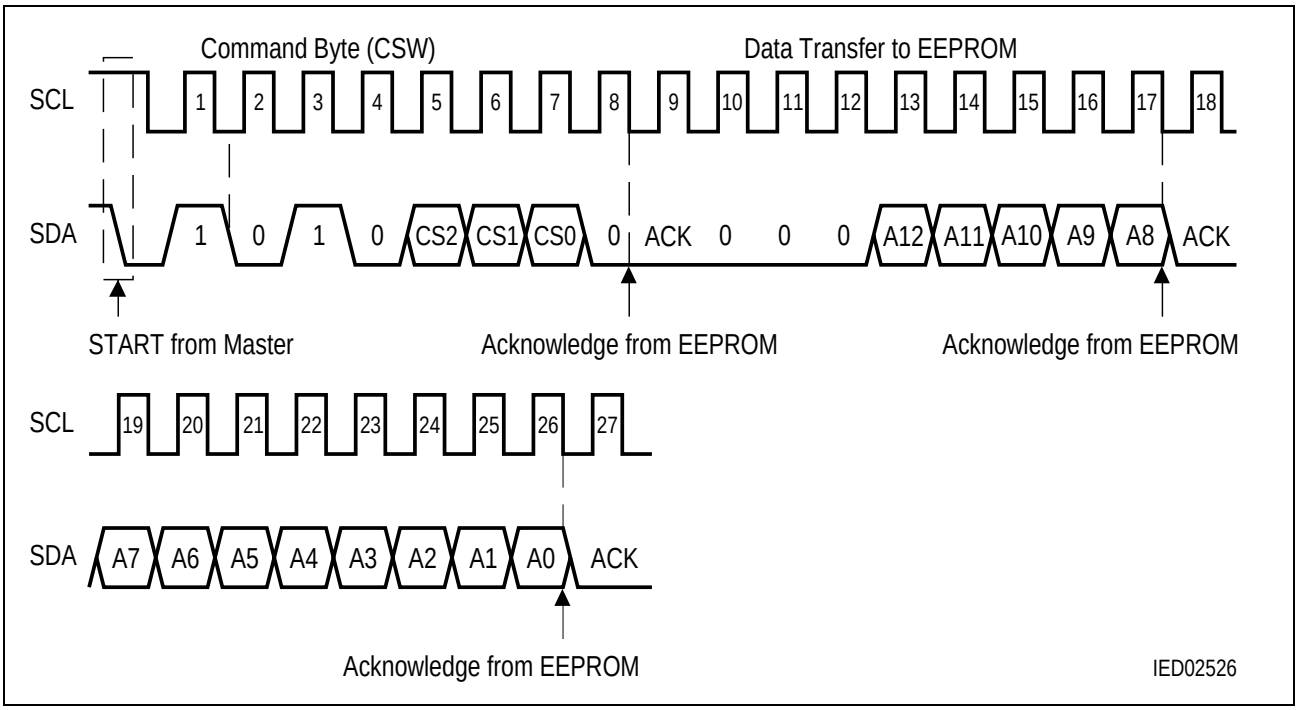


Figure 5
Timing of the Command Byte CSW

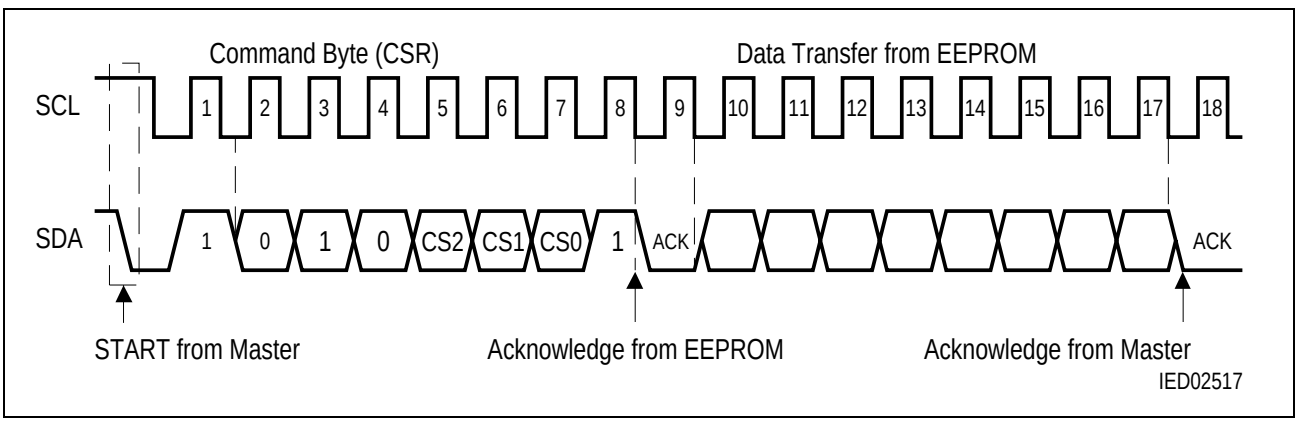


Figure 6
Timing of the Command Byte CSR

5 Write Operations

Changing of the EEPROM data is initiated by the master with the command byte CSW. Either one byte (Byte Write) or up to 32 byte (Page Write) are modified in one programming procedure. Setting the Write Protection pin WP to V_{CC} activates the hardware write protection and therefore any programming is suppressed. For normal operation WP has to be set to V_{SS}.

5.1 Byte Write

Address Setting After a START condition the master transmits the Chip Select Write byte CSW. The EEPROM acknowledges the CSW byte during the ninth clock cycle. The following two bytes AHI/ALO with the EEPROM address (A0 to A12) are loaded into the address counter of the EEPROM and acknowledged by the EEPROM.

Transmission of Data Finally the master transmits the data byte which is also acknowledged by the EEPROM into the internal buffer.

Programming Cycle Then the master applies a STOP condition which starts the internal programming procedure. The data bytes are written in the memory location addressed in the bytes AHI (A8 to A12) and ALO (A0 to A7). The programming procedure consists of an internally timed erase/write cycle. In the first step, the selected byte is erased to “1”. With the next internal step, the addressed byte is written according to the contents of the buffer.

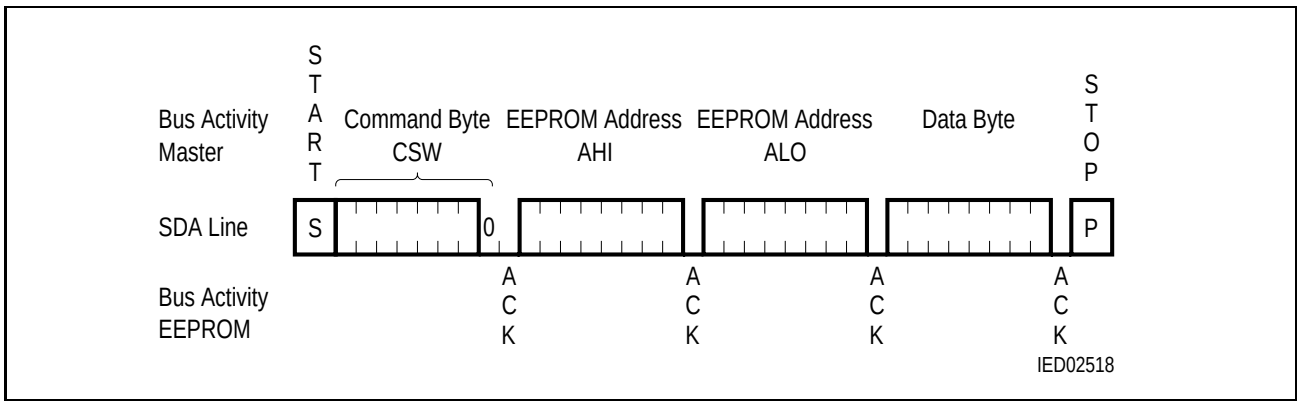


Figure 7
Byte Write Sequence

The erase/write cycle is finished latest after 8 ms. Acknowledge polling can be used for speed enhancement in order to detect the end of the erase/write cycle. Please refer to **chapter 5.3**, Acknowledge Polling for further information.

5.2 Page Write

Address Setting The page write procedure is the same as the byte write procedure up to the first data byte. In a page write instruction however, entry of the EEPROM address bytes AHI/ALO are followed by a sequence of one to a maximum of 32 data bytes with the new data to be programmed. These bytes are transferred to the internal page buffer of the EEPROM.

Transmission of Data The first entered data byte will be stored according to the EEPROM address n given by AHI (A8 to A12) and ALO (A0 to A7). The internal address counter is incremented automatically after the entered data byte has been acknowledged. The next data byte is then stored at the next higher EEPROM address. EEPROM addresses within the same page have common page address bits A5 through A12. Only the respective five least significant address bits A0 through A4 are incremented, as all data bytes to be programmed simultaneously have to be within the same page. Writing over the page border will cause the address counter to roll over to the first address of the page.

Programming Cycle The master stops data entry by applying a STOP condition, which also starts the internally timed erase/write cycle. In the first step, all selected bytes are erased to “1”. With the next internal step, the addressed bytes are written according to the contents of the page buffer.

Those bytes of the page that have not been addressed are not included in the programming.

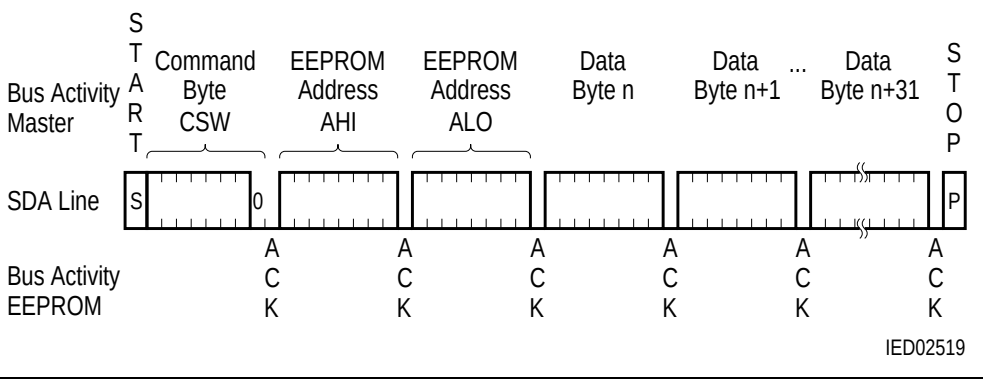


Figure 8
Page Write Sequence

The erase/write cycle is finished latest after 8 ms. Acknowledge polling can be used for speed enhancement in order to detect the end of the erase/write cycle. Please refer to **chapter 5.3**, Acknowledge Polling for further information.

5.3 Acknowledge Polling

During the erase/write cycle the EEPROM will not respond to a new command byte until the internal write procedure is completed. At the end of active programming the chip returns to the standby mode and the last entered EEPROM byte remains addressed by the address counter. To determine the end of the internal erase/write cycle acknowledge polling can be initiated by the master by sending a START condition followed by a command byte CSR or CSW (read with b0 = 1 or write with b0 = 0). If the internal erase/write cycle is not completed, the device will not acknowledge the transmission. If the internal erase/write cycle is completed, the device acknowledges the received command byte and the protocol activities can continue.

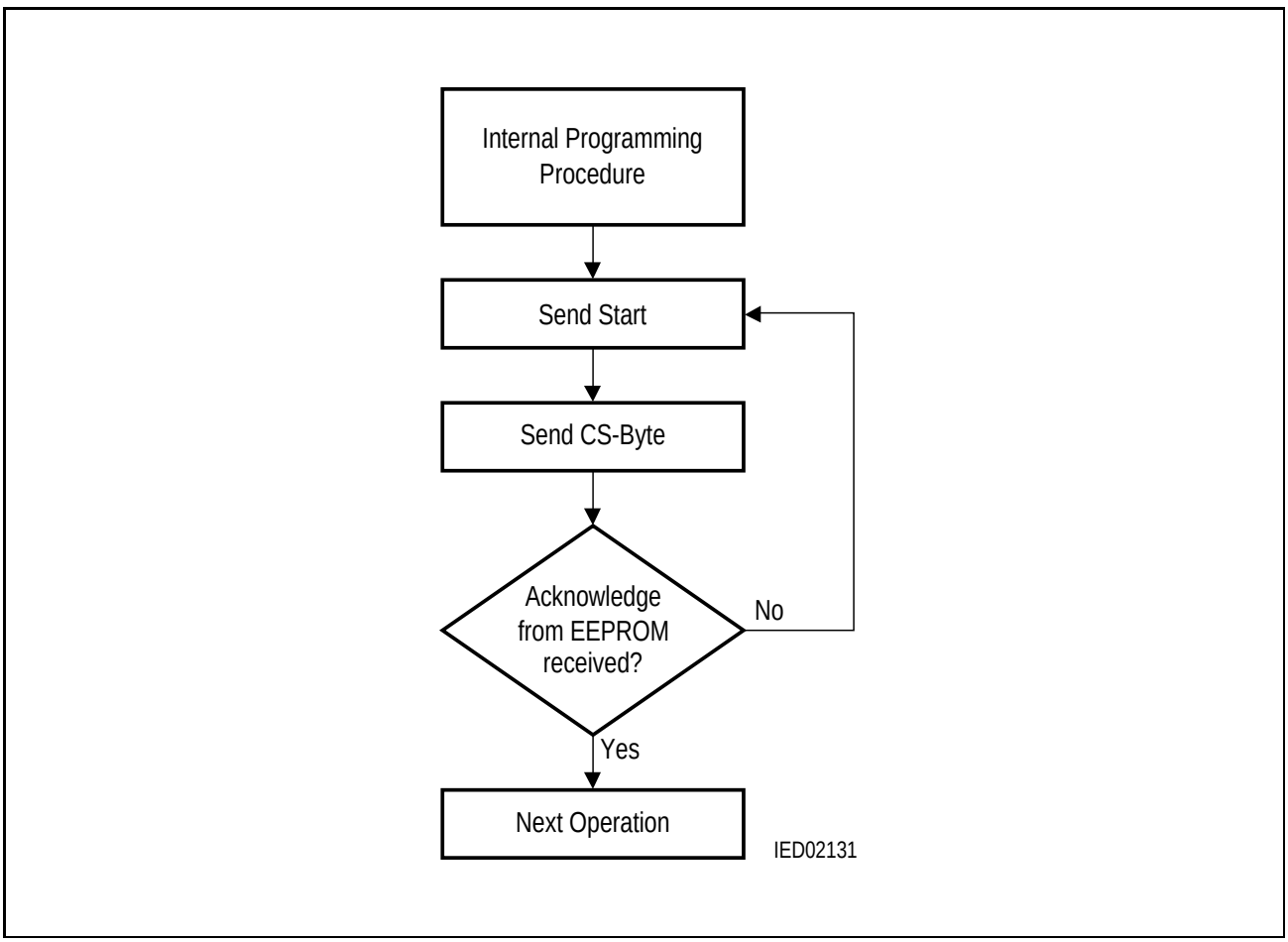


Figure 9
Flow Chart “Acknowledge Polling”

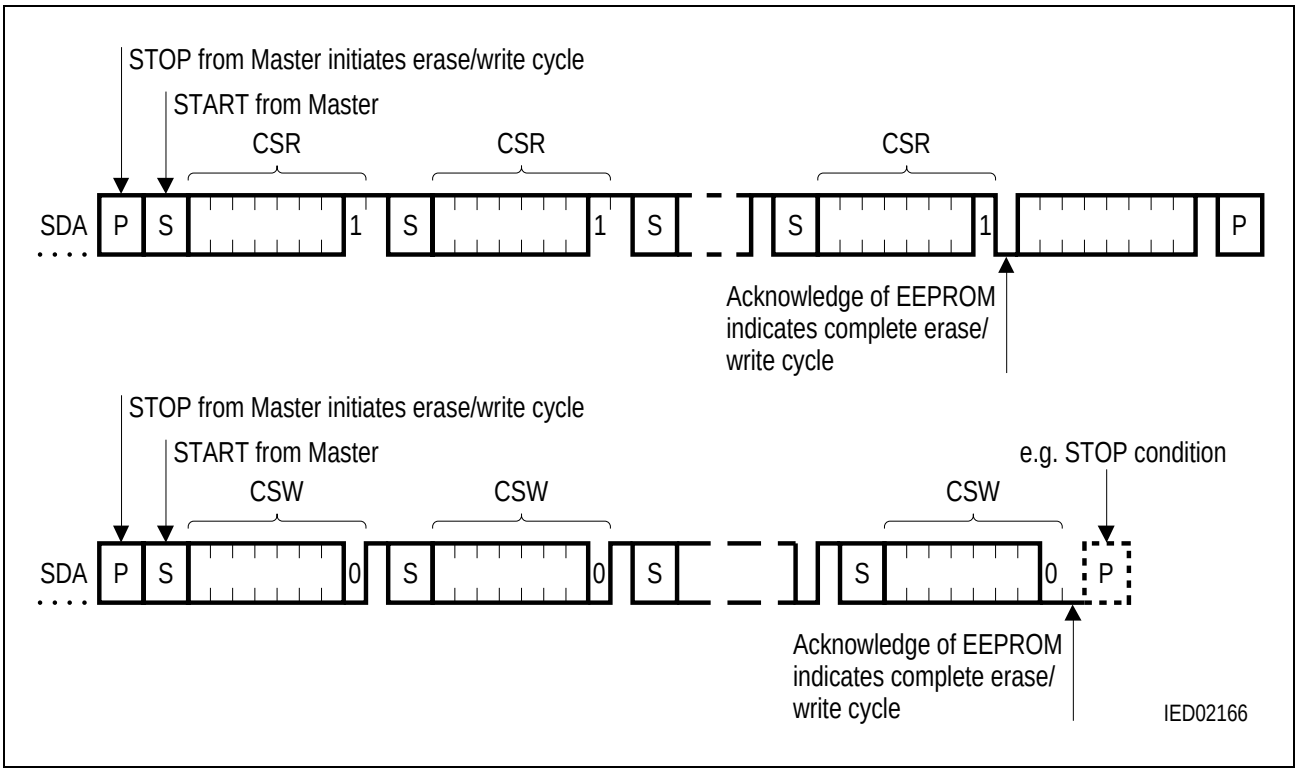


Figure 10
Principle of Acknowledge Polling

6 Read Operations

Reading of the EEPROM data is initiated by the Master with the command byte CSR.

6.1 Random Read

Random read operations allow the master to access any memory location.

Address Setting The master generates a START condition followed by the command byte CSW. The receipt of the CSW-byte is acknowledged by the EEPROM with a low state on the SDA line. Now the master transmits the EEPROM address (AHI/ ALO) to the EEPROM and the internal address counter is loaded with the desired address.

Transmission of CSR After the acknowledge for the EEPROM address is received, the master generates a START condition, which terminates the initiated write operation. Then the master transmits the command byte CSR for read, which is acknowledged by the EEPROM.

Transmission of EEPROM Data During the next eight clock pulses the EEPROM transmits the data byte and increments the internal address counter by one byte.

STOP Condition from Master During the following clock cycle the masters releases the bus and then transmits the STOP condition.

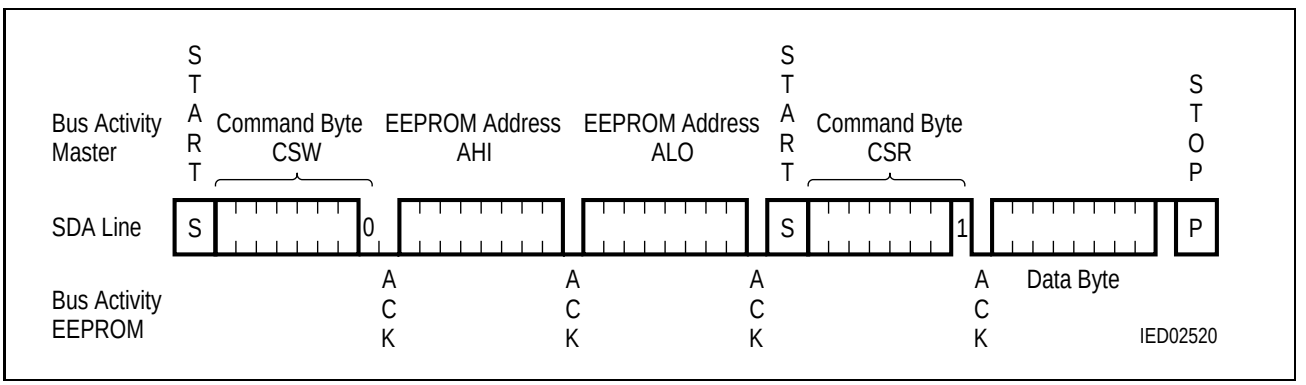


Figure 11
Random Read

6.2 Current Address Read

The EEPROM content is read without setting an EEPROM address, in this case the current content of the address counter will be used (e.g. to continue a previous read operation after the Master has served an interrupt).

Transmission of CSR For a current address read the master generates a START condition, which is followed by the command byte CSR (Chip Select Read). The receipt of the CSR-byte is acknowledged by the EEPROM with a low on the SDA line.

Transmission of EEPROM Data During the next eight clock pulses the EEPROM transmits the data byte and increments the internal address counter by one byte.

STOP Condition from Master During the following clock cycle the masters releases the bus and then transmits the STOP condition.

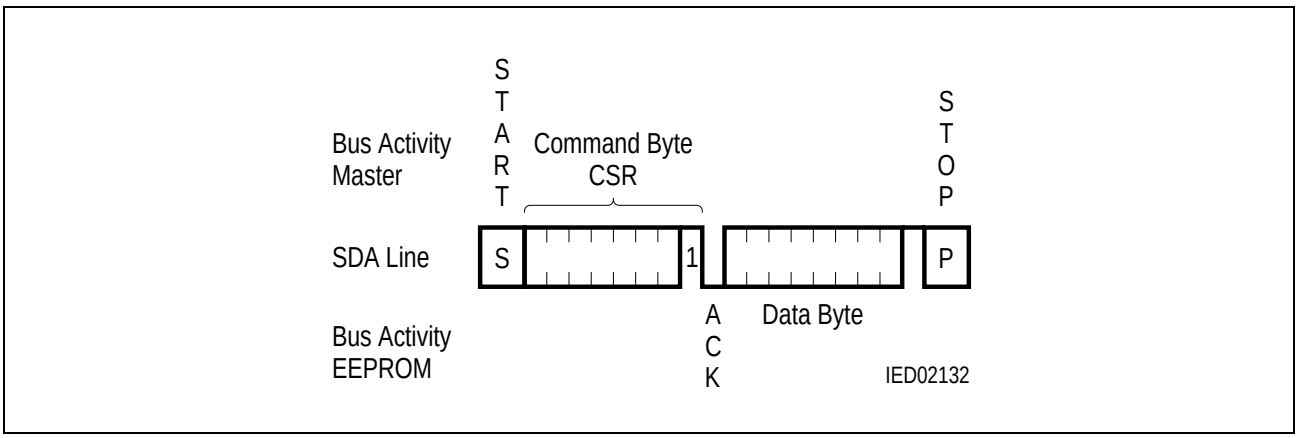


Figure 12
Current Address Read

6.3 Sequential Read

A sequential read is initiated in the same way as a current read or a random read except that the master acknowledges the data byte transmitted by the EEPROM. The EEPROM then continues the data transmission. The internal address counter is incremented by one during each data byte transmission.

A sequential read allows the entire memory to be read during one read operation. After the highest addressable memory location is reached, the internal address pointer “rolls over” to the address 0 and the sequential read continues.

The transmission is terminated by the master by releasing the SDA line (no acknowledge) and generating a STOP condition (see **figure 13**).

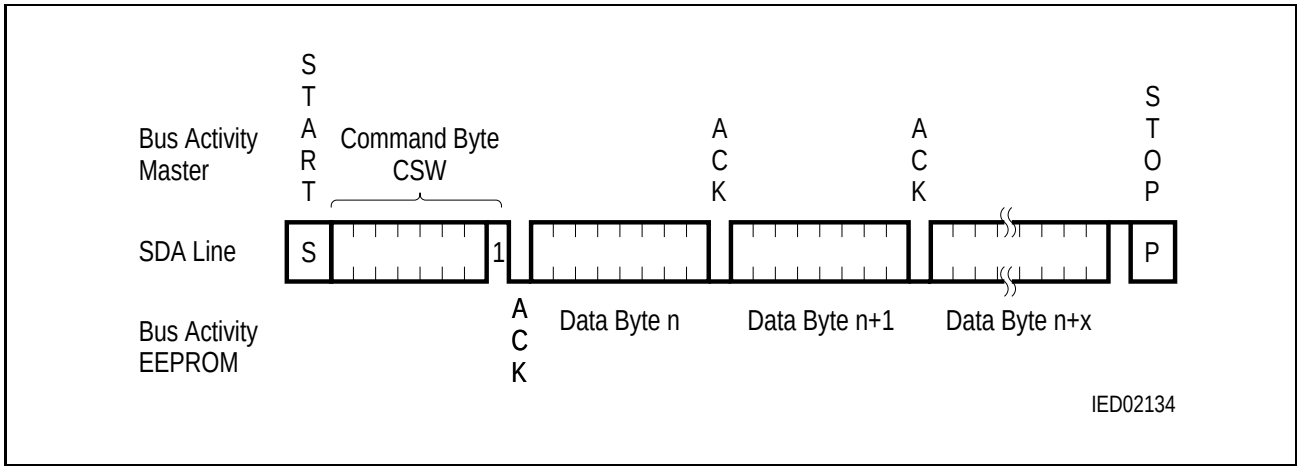


Figure 13
Sequential Read

7 Page Protection Mode™

The page protection mode is supported by the SLx 24C64.../P types only. For example SLA 24C64-D/P has the same functionality as SLA 24C64-D enhanced by page protection mode.

Each page (32 bytes) in the data memory can be protected against unintended data changes by an associated protection bit. The protection bit memory consists of an additional EEPROM of 256 bit (**figure 14**).

Data in the data memory can be modified only if the assigned protection bit is erased (logical state “1”). After writing the data bytes to a page, the protection is achieved by writing the associated protection bit (logical state “0”). Further changes in the data in a protected page is possible only after erasing the protection bit.

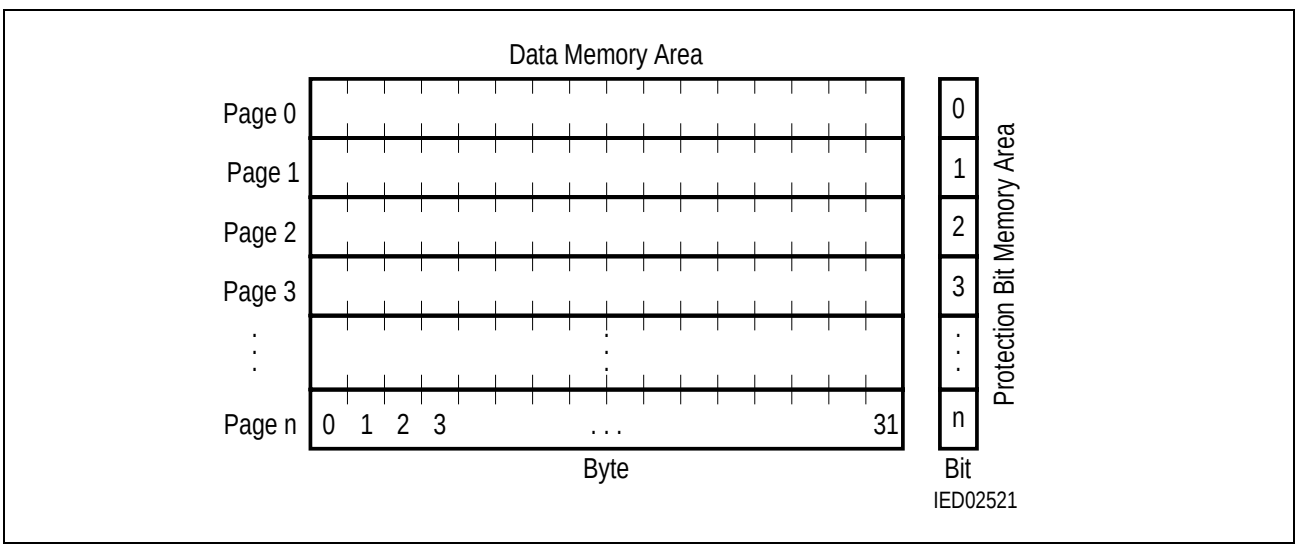


Figure 14
Data Page and Assigned Protection Memory

A special procedure to write or erase a protection bit guarantees proper activation or deactivation of page protection. For protection bit write or erase all 32 data bytes of the respective page have to be entered for verification. The data then are compared internally with the data to be protected. In case of identity the protection bit is written or erased respectively.

7.1 Protection Bit Handling

The bits of the protection memory can be addressed directly for reading or programming. A protection bit address corresponds to the lowest address within the respective page (A5 to A12, A0 to A4 = zero). The status of each protection bit is sensed internally. A written state (“0”) prevents programming in the associated page. If an already protected memory page is accidentally addressed for programming, the programming procedure is suppressed.

The conventional I^2C-Bus protocol allows data bytes to be read and programmed only. Therefore an independent instruction sequence for addressing and manipulation of protection bits is implemented. For protection bit instructions the command byte CSW with its preceding START condition followed by the associated address bytes have to be entered twice (**figures 15** through **17**). The first command byte CSW is followed by the address bytes AHI/ALO with the bit/page address A0 through A4 always at zero. The second CSW is required for entering a control byte CTx for protection bit manipulation. The three control bytes for read, write or erase of a protection bit are listed below (**table 3**):

Table 3
Control Byte for Protection Bit Manipulation

Address Name	Definition								Function
	b7	b6	b5	b4	b3	b2	b1	b0	
CTR	x	x	x	x	x	x	0	0	Protection bit read
CTW	x	x	x	x	x	x	0	1	Protection bit write
CTE	x	x	x	x	x	x	1	1	Protection bit erase

7.2 Protection Bit Write and Erase

For writing or erasing a protection bit the data of the respective page have to be known by the master. The master has to present the page data as a reference for comparison by the EEPROM. A successful comparison is necessary in order to change the value of the protection bit.

The data of the page are not affected by the write or erase procedure of the protection bit. The I^2C-Bus protocol is shown in **figure 15** for protection bit write and **figure 16** for protection bit erase.

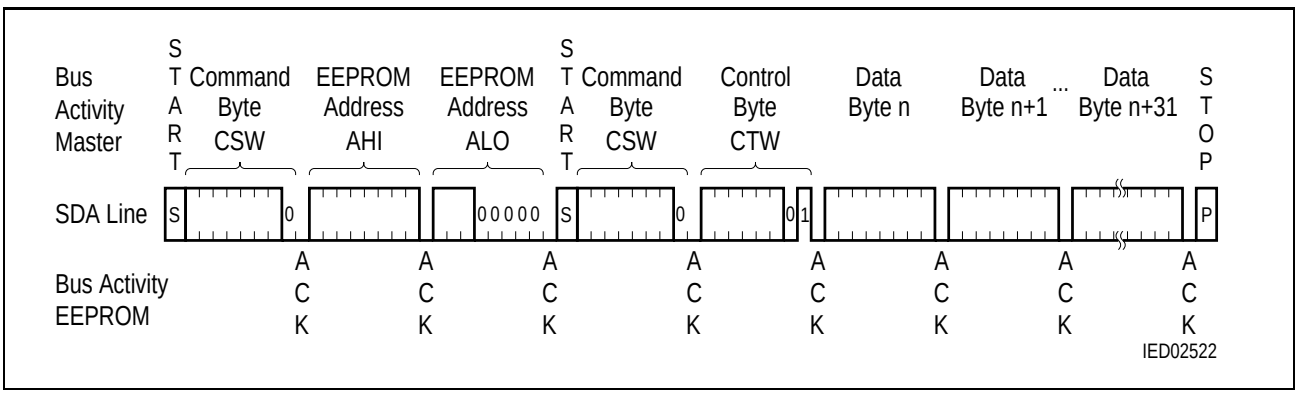


Figure 15
Sequence for Protection Bit Write

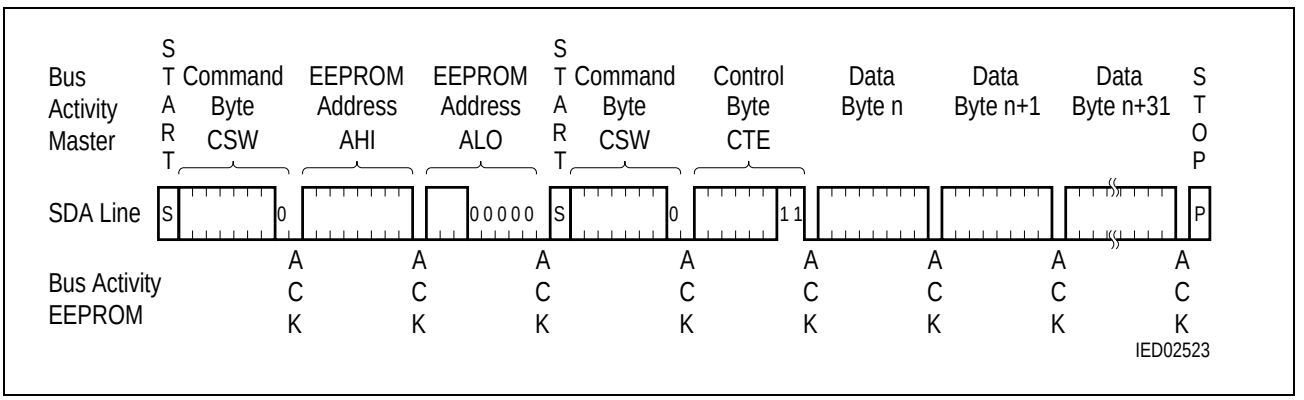


Figure 16
Sequence for Protection Bit Erase

The first command byte CSW followed by the address bytes AHI/ALO determines the page to be protected. The second command byte CSW (identical content of first CSW) is followed by the control byte CTW = 01_H for protection bit write or CTE = 03_H for protection bit erase. Depending on CTx, the addressed protection bit will be either written or erased.

The control byte CTx is followed by 32 parameter bytes identical to the 32 data bytes of the page to be protected or unprotected. The data of the first entered byte must be identical to the data byte stored at the lowest address of the current page. The other

31 bytes have to be identical to the bytes stored in ascending address order within the same page.

A successful verification of each byte is indicated by the EEPROM by pulling the SDA line to low (acknowledge ACK).

The bit programming procedure is initiated by the STOP condition after verification of the last byte. Programming is started only if all 256 bits of a page have been verified successfully. If bit programming has taken place, the address counter points to the uppermost address of the respective page. The write or erase cycle is finished latest after 4 ms. Acknowledge polling can be used for speed enhancement in order to detect the end of the write or erase cycle (refer to **chapter 5.3,** Acknowledge Polling).

7.3 Protection Bit Read

The byte sequence for random bit read is shown in **figure 17**.

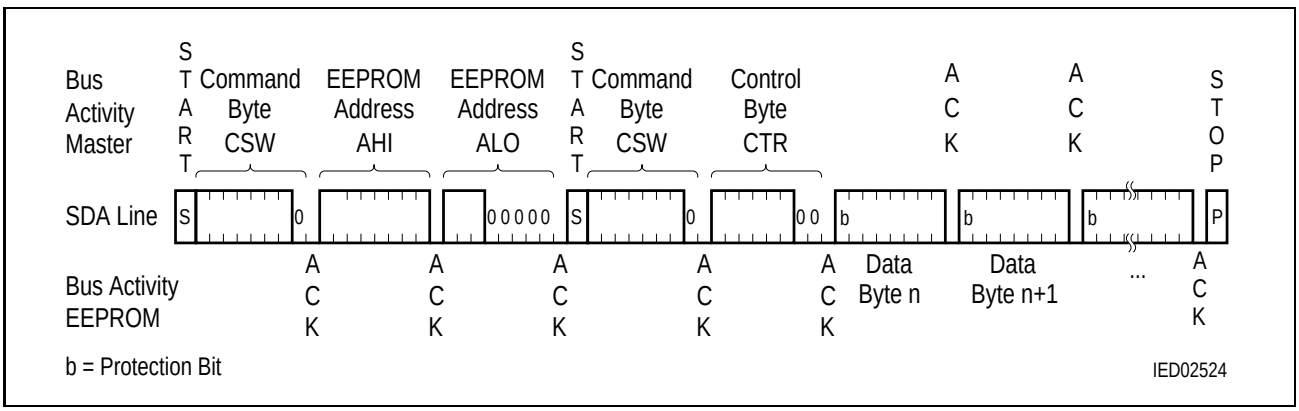


Figure 17
Byte Sequence for Protection Bit Read

The first command byte CSW followed by the address bytes AHI/ALO determine the protection bit to be read. The second command byte CSW is followed by the control byte 00_H for protection bit read. The first bit (MSB) of the transferred byte is the protection bit of the addressed page. The other 7 bits are not valid. The page protection status is indicated as follows:

Protection Bit = 1: A normal write operation changes the data in the associated page
Protection Bit = 0: The data in the associated page are protected against changes.

If the master acknowledges a byte with a low state of the SDA line, the protection bit of the next page can be read as the first bit of the following byte. If the master releases the SDA line, a STOP condition has to complete the read procedure. Any number of bytes with a page protection status at the first bit position can be requested by the master. After the bit of the uppermost page has been addressed an overflow of the address counter occurs and the protection bit of the first page will be read next.

8 Electrical Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

8.1 Absolute Maximum Ratings

Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this data sheet is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter		Limit Values	Units
Operating temperature	range 1 (industrial) range 2 (automotive)	– 40 to + 85 – 40 to + 125	°C °C
Storage temperature		– 65 to + 150	°C
Supply voltage		– 0.3 to + 7.0	V
All inputs and outputs with respect to ground		– 0.3 to V_{CC} + 0.5	V
ESD protection (human body model)		4000	V

8.2 DC Characteristics

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Supply voltage	V_{CC}	4.5		5.5	V	5 V type
	V_{CC}	2.7		5.5	V	3 V type
Supply current[1] (write)	I_{CC}			3	mA	V_{CC} = 5 V; f_c = 100 kHz
Standby current[2]	I_{SB}			1	µA	Inputs at V_{CC} or V_{SS}
Input leakage current	I_{LI}		0.1	1	µA	V_{IN} = V_{CC} or V_{SS}
Output leakage current	I_{LO}		0.1	1	µA	V_{OUT} = V_{CC} or V_{SS}
Input low voltage	V_{IL}	– 0.3		0.3 × V_{CC}	V	

8.2 DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Units	Test Condition
		min.	typ.	max.		
Input high voltage	V_{IH}	$0.7 \times V_{CC}$		V_{CC} + 0.5	V	
Output low voltage	V_{OL}			0.4	V	I_{OL} = 3 mA; V_{CC} = 5 V I_{OL} = 2.1 mA; V_{CC} = 3 V
Input/output capacitance (SDA)	$C_{I/O}$			8[3)]	pF	V_{IN} = 0 V; V_{CC} = 5 V
Input capacitance (other pins)	C_{IN}			6[3)]	pF	V_{IN} = 0 V; V_{CC} = 5 V

1) The values for I_{cc} are maximum peak values

2) Valid over the whole temperature range

3) This parameter is characterized only

8.3 AC Characteristics

Parameter	Symbol	Limit Values V_{CC} = 2.7-5.5 V		Limit Values V_{CC} = 4.5-5.5 V		Units
		min.	max.	min.	max.	
SCL clock frequency	f_{SCL}		100		400	kHz
Clock pulse width low	t_{low}	4.7		1.2		µs
Clock pulse width high	t_{high}	4.0		0.6		µs
SDA and SCL rise time	t_R		1000	[1)]	300	ns
SDA and SCL fall time	t_F		300	[1)]	300	ns
Start set-up time	$t_{SU.STA}$	4.7		0.6		µs
Start hold time	$t_{HD.STA}$	4.0		0.6		µs
Data in set-up time	$t_{SU.DAT}$	200		100		ns
Data in hold time	$t_{HD.DAT}$	0		0		µs
SCL low to SDA data out valid	t_{AA}	0.1	4.5	0.1	0.9	µs
Data out hold time	t_{DH}	100		50		ns
Stop set-up time	$t_{SU.STO}$	4.0		0.6		µs
Time the bus must be free before a new transmission can start	t_{BUF}	4.7		1.2		µs
SDA and SCL spike suppression time at constant inputs	t_I	50	100	50	100	ns

[1)] The minimum rise and fall times can be calculated as follows: (20 + (0.1/pF) × C_b) ns
Example: C_b = 100 pF → t_R = (20 + 0.1 × 100) ns = 30 ns

8.4 Erase and Write Characteristics

Parameter	Symbol	Limit Values V_{cc} = 2.7-5.5 V		Limit Values V_{cc} = 4.5-5.5 V		Units
		typ.	max.	typ.	max.	
Erase + write cycle (per page)	t_{WR}	5	8	5	8	ms
Erase page protection bit		2.5	4	2.5	4	ms
Write page protection bit		2.5	4	2.5	4	ms

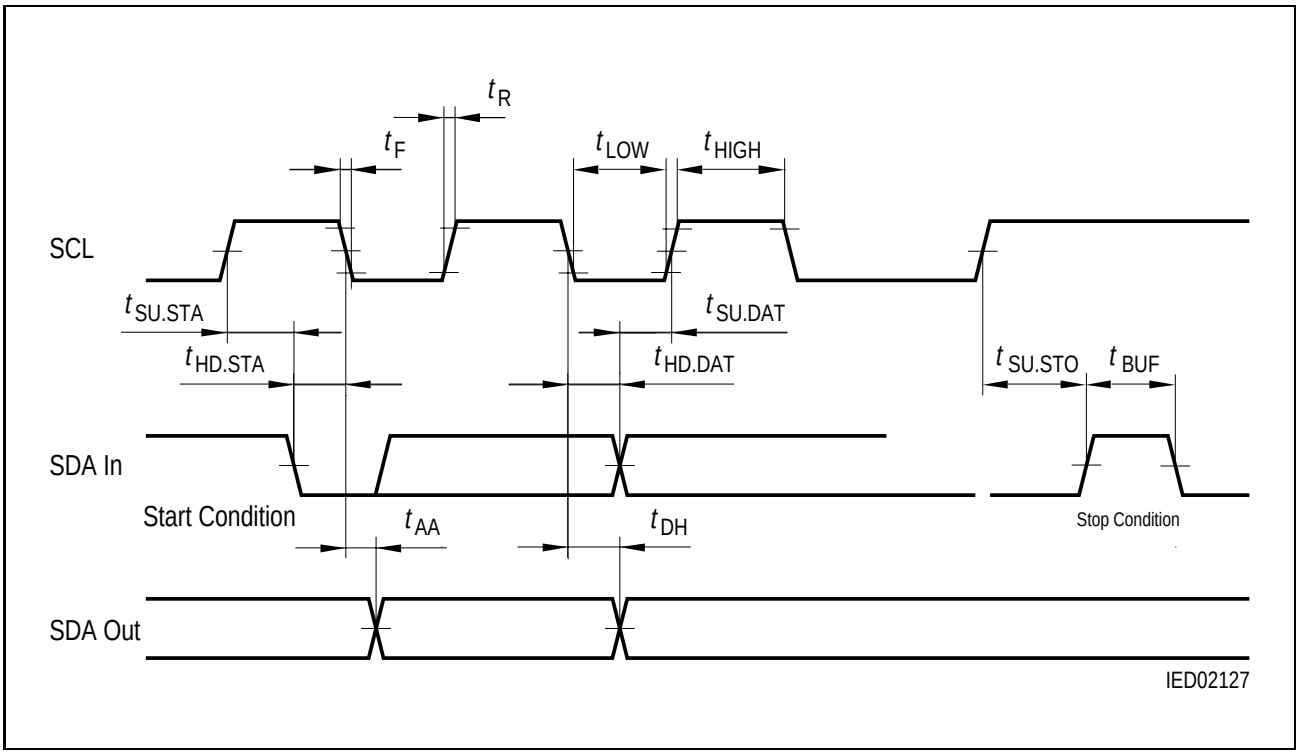
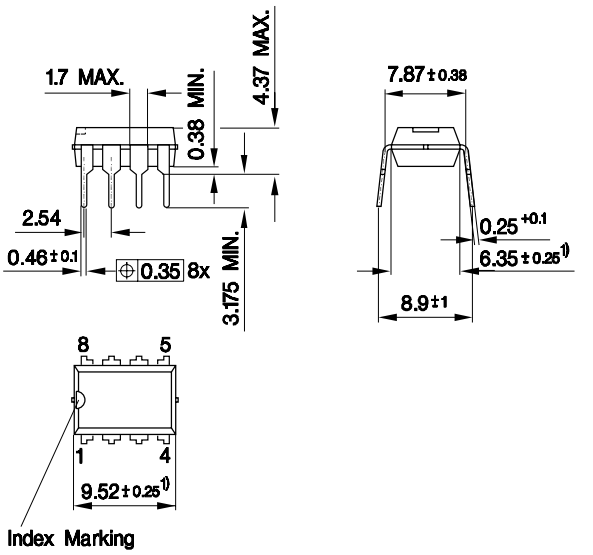


Figure 18
Bus Timing Data

9 Package Outlines

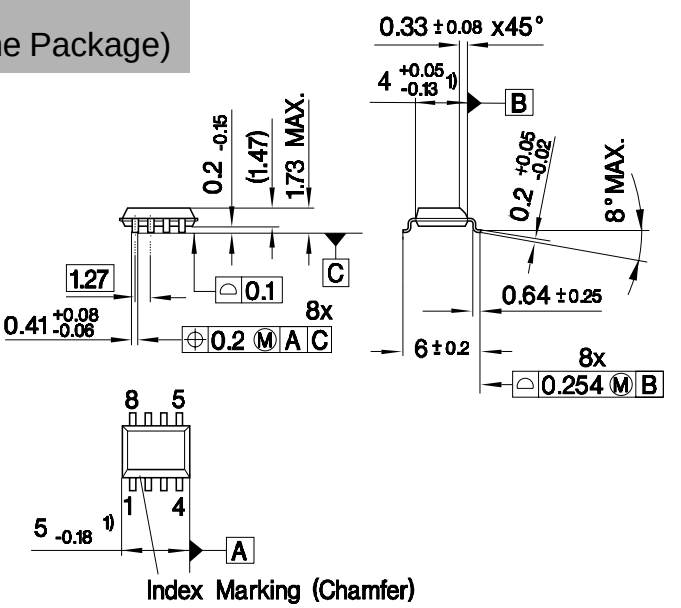
P-DIP-8-4
(Plastic Dual In-line Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05583

P-DSO-8-3
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09032

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm